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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564l54l3cboqr

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double buffered trigger generation unit with as many as 8 independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 120 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows control of ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.5.35 Cyclic Redundancy Checker (CRC) Unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to its input register.

The CRC unit has the following features:

- 3 sets of registers to allow 3 concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores result in internal register.
  The following standard CRC polynomials are implemented:
  - $x^8 + x^4 + x^3 + x^2 + 1$ [8-bit CRC]
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads core from cycle-consuming CRC and helps checking configuration signature for safe start-up or periodic procedures
- CRC unit connected as peripheral bus on internal peripheral bus
- DMA support

1.5.36 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to guarantee highest possible diagnostic coverage (check of checker)
- Multiple times replicated IPs are used as checkers on the SoR outputs

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
83	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
84	JCOMP	—	—	JCOMP
85	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
86	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
87	$V_{DD\_HV\_IO}$	—		
88	$V_{SS\_HV\_IO}$	—		
89	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
90	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
91	$V_{DD\_HV\_REG\_2}$	—		
92	$V_{DD\_LV\_COR}$	—		
93	$V_{SS\_LV\_COR}$	—		
94	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
95	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
96	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
97	FCCU_F[1]	FCCU	F[1]	F[1]
98	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
99	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
100	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1. V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 4. LQFP144 pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
1	NMI	—		
2	A[6]	SIUL	GPIO[6]	GPIO[6]
		DSPI_1	SCK	SCK
		SIUL	—	EIRQ[6]

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
D3	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]
D4	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
D5	$V_{SS\_LV\_CORE\_RING}$	—		
D6	$V_{DD\_LV\_CORE\_RING}$	—		
D7	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
D8	$V_{DD\_HV\_IO\_RING}$	—		
D9	$V_{SS\_HV\_IO\_RING}$	—		
D10	Not connected	—		
D11	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
D12	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
D13	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
D14	$V_{DD\_HV\_IO\_RING}$	—		
D15	V_{PP_TEST}(1)	—		
D16	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
K9	V_{SS_LV}	—		
K10	V_{SS_LV}	—		
K11	V_{SS_LV}	—		
K12	V_{DD_LV}	—		
K14	Not connected	—		
K15	H[8]	SIUL	GPIO[120]	GPIO[120]
		FlexPWM_1	A[1]	A[1]
		DSPI_0	CS6	—
K16	H[7]	SIUL	GPIO[119]	GPIO[119]
		FlexPWM_1	X[1]	X[1]
		eTimer_2	ETC[1]	ETC[1]
K17	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
L1	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	EVTO	—
L2	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	EVTI
L3	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
L4	Not connected	—		
L6	V_{DD_LV}	—		
L7	V_{SS_LV}	—		
L8	V_{SS_LV}	—		
L9	V_{SS_LV}	—		
L10	V_{SS_LV}	—		
L11	V_{SS_LV}	—		
L12	V_{DD_LV}	—		
L14	Not connected	—		
L15	TCK	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
L16	H[4]	SIUL	GPIO[116]	GPIO[116]
		FlexPWM_1	X[0]	X[0]
		eTimer_2	ETC[0]	ETC[0]
L17	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
M1	$V_{DD\_HV\_OSC}$	—		
M2	$V_{DD\_HV\_IO\_RING}$	—		
M3	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
M4	Not connected	—		
M6	V_{DD_LV}	—		
M7	V_{DD_LV}	—		
M8	V_{DD_LV}	—		
M9	V_{DD_LV}	—		
M10	V_{DD_LV}	—		
M11	V_{DD_LV}	—		
M12	V_{DD_LV}	—		
M14	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
M15	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
M16	TMS	—		
M17	H[5]	SIUL	GPIO[117]	GPIO[117]
		FlexPWM_1	A[0]	A[0]
		DSPI_0	CS4	—
N1	XTAL	—		
N2	$V_{SS\_HV\_IO\_RING}$	—		
N3	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
N4	$V_{SS\_LV\_PLL0\_PLL1}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
N14	Not connected	—		
N15	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
N16	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
N17	G[5]	SIUL	GPIO[101]	GPIO[101]
		FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
P1	$V_{SS\_HV\_OSC}$	—		
P2	RESET	—		
P3	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
P4	$V_{DD\_LV\_PLL0\_PLL1}$	—		
P5	$V_{DD\_LV\_CORE\_RING}$	—		
P6	$V_{SS\_LV\_CORE\_RING}$	—		
P7	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
P8	Not connected	—		
P9	$V_{SS\_HV\_IO\_RING}$	—		
P10	$V_{DD\_HV\_IO\_RING}$	—		
P11	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
P12	$V_{DD\_LV\_CORE\_RING}$	—		
P13	$V_{SS\_LV\_CORE\_RING}$	—		
P14	$V_{DD\_HV\_IO\_RING}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
R12	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
R13	BCTRL	—		
R14	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
R15	$V_{SS\_HV\_IO\_RING}$	—		
R16	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
R17	G[9]	SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
		DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
T1	$V_{SS\_HV\_IO\_RING}$	—		
T2	$V_{DD\_HV\_IO\_RING}$	—		
T3	Not connected	—		
T4	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
T5	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
T6	E[7]	SIUL	—	GPIO[71]
		ADC_0	—	AN[6]
T7	$V_{SS\_HV\_ADR0}$	—		
T8	B[11]	SIUL	—	GPIO[27]
		ADC_0 ADC_1	—	AN[13]
T9	$V_{SS\_HV\_ADR1}$	—		
T10	E[9]	SIUL	—	GPIO[73]
		ADC_1	—	AN[7]
T11	E[10]	SIUL	—	GPIO[74]
		ADC_1	—	AN[8]

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
T12	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]
T13	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
T14	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
T15	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
T16	$V_{DD\_HV\_IO\_RING}$	—		
T17	$V_{SS\_HV\_IO\_RING}$	—		
U1	$V_{SS\_HV\_IO\_RING}$	—		
U2	$V_{SS\_HV\_IO\_RING}$	—		
U3	Not connected	—		
U4	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
U5	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
U6	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
U7	B[9]	SIUL	—	GPIO[25]
		ADC_0 ADC_1	—	AN[11]
U8	B[12]	SIUL	—	GPIO[28]
		ADC_0 ADC_1	—	AN[14]
U9	$V_{DD\_HV\_ADV}$	—		
U10	$V_{SS\_HV\_ADV}$	—		
U11	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
U12	Not connected	—		
U13	Not connected	—		
U14	$V_{DD\_HV\_PMU}$	—		

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[4]	PCR[36]	SIUL	GPIO[36]	ALT0	GPIO[36]	—	—	M	S	5	11	H3
		DSPI_0	CS0	ALT1	CS0	—						
		FlexPWM_0	X[1]	ALT2	X[1]	PSMI[28]; PADSEL=0						
		SSCM	DEBUG[4]	ALT3	—	—						
		SIUL	—	—	EIRQ[22]	—						
C[5]	PCR[37]	SIUL	GPIO[37]	ALT0	GPIO[37]	—	—	M	S	7	13	G3
		DSPI_0	SCK	ALT1	SCK	—						
		SSCM	DEBUG[5]	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=0						
		SIUL	—	—	EIRQ[23]	—						
C[6]	PCR[38]	SIUL	GPIO[38]	ALT0	GPIO[38]	—	—	M	S	98	142	D4
		DSPI_0	SOUT	ALT1	—	—						
		FlexPWM_0	B[1]	ALT2	B[1]	PSMI[25]; PADSEL=0						
		SSCM	DEBUG[6]	ALT3	—	—						
		SIUL	—	—	EIRQ[24]	—						
C[7]	PCR[39]	SIUL	GPIO[39]	ALT0	GPIO[39]	—	—	M	S	9	15	K4
		FlexPWM_0	A[1]	ALT2	A[1]	PSMI[21]; PADSEL=0						
		SSCM	DEBUG[7]	ALT3	—	—						
		DSPI_0	—	—	SIN	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[10]	PCR[42]	SIUL	GPIO[42]	ALT0	GPIO[42]	—	—	M	S	78	111	A15
		DSPI_2	CS2	ALT1	—	—						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=0						
C[11]	PCR[43]	SIUL	GPIO[43]	ALT0	GPIO[43]	—	—	M	S	55	80	M14
		eTimer_0	ETC[4]	ALT1	ETC[4]	PSMI[7]; PADSEL=1						
		DSPI_2	CS2	ALT2	—	—						
C[12]	PCR[44]	SIUL	GPIO[44]	ALT0	GPIO[44]	—	—	M	S	56	82	N15
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=0						
		DSPI_2	CS3	ALT2	—	—						
C[13]	PCR[45]	SIUL	GPIO[45]	ALT0	GPIO[45]	—	—	M	S	71	101	F15
		eTimer_1	ETC[1]	ALT1	ETC[1]	PSMI[10]; PADSEL=0						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=0						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=0						
C[14]	PCR[46]	SIUL	GPIO[46]	ALT0	GPIO[46]	—	—	M	S	72	103	E15
		eTimer_1	ETC[2]	ALT1	ETC[2]	PSMI[11]; PADSEL=1						
		CTU_0	EXT_TGR	ALT2	—	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[10]	PCR[58]	SIUL	GPIO[58]	ALT0	GPIO[58]	—	—	M	S	53	76	T15
		FlexPWM_0	A[0]	ALT1	A[0]	PSMI[20]; PADSEL=1						
		eTimer_0	—	—	ETC[0]	PSMI[35]; PADSEL=1						
D[11]	PCR[59]	SIUL	GPIO[59]	ALT0	GPIO[59]	—	—	M	S	54	78	R16
		FlexPWM_0	B[0]	ALT1	B[0]	PSMI[24]; PADSEL=1						
		eTimer_0	—	—	ETC[1]	PSMI[36]; PADSEL=1						
D[12]	PCR[60]	SIUL	GPIO[60]	ALT0	GPIO[60]		—	M	S	70	99	G14
		FlexPWM_0	X[1]	ALT1	X[1]	PSMI[28]; PADSEL=1						
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=1						
D[14]	PCR[62]	SIUL	GPIO[62]	ALT0	GPIO[62]	—	—	M	S	73	105	D16
		FlexPWM_0	B[1]	ALT1	B[1]	PSMI[25]; PADSEL=2						
		eTimer_0	—	—	ETC[3]	PSMI[38]; PADSEL=1						
Port E												
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—	46	68	T13
		ADC_1	—	—	AN[5](3)	—						
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—	32	49	U6
		ADC_0	—	—	AN[5](3)	—						

Table 22. Current consumption characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_HV\_AREF}$[4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_REF}$ = 3.6 V	—	—	3	mA
			T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_REF}$ = 5.5 V	—	—	5	
$I_{DD\_HV\_OSC}$ (oscillator bypass mode)	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	900	µA
$I_{DD\_HV\_OSC}$ (crystal oscillator mode)	D	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	3.5	mA
$I_{DD\_HV\_FLASH}$[5]	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	4	mA
$I_{DD\_HV\_PMU}$	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	10	mA

1. Devices configured for DPM mode, single core only with Core 0 executing typical code at 120 MHz from SRAM and Core 1 in reset. If core execution mode not specified, the device is configured for LSM mode with both cores executing typical code at 120 MHz from SRAM.
2. Enabled Modules in 'Typical mode': FlexPWM0, ETimer0/1/2, CTU, SWG, DMA, FlexCAN0/1, LINFlex, ADC1, DSPI0/1, PIT, CRC, PLL0/1, I/O supply current excluded. If DPM mode is configured, Core_0 is active while Core_1 is in reset during the measurements.
3. Internal structures hold the input voltage less than VDDA + 1.0 V on all pads powered by VDDA supplies, if the maximum injection current specification is met and VDDA is within the operating voltage specifications.
4. This value is the total current for both ADCs.
5. VFLASH is only available in the calibration package.

3.12 Temperature sensor electrical characteristics

Table 23. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Min	Max	Unit
—	P	Accuracy	T_J = –40 °C to 150 °C	–10	10	°C
T_S	D	Minimum sampling period	—	4	—	µs

and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

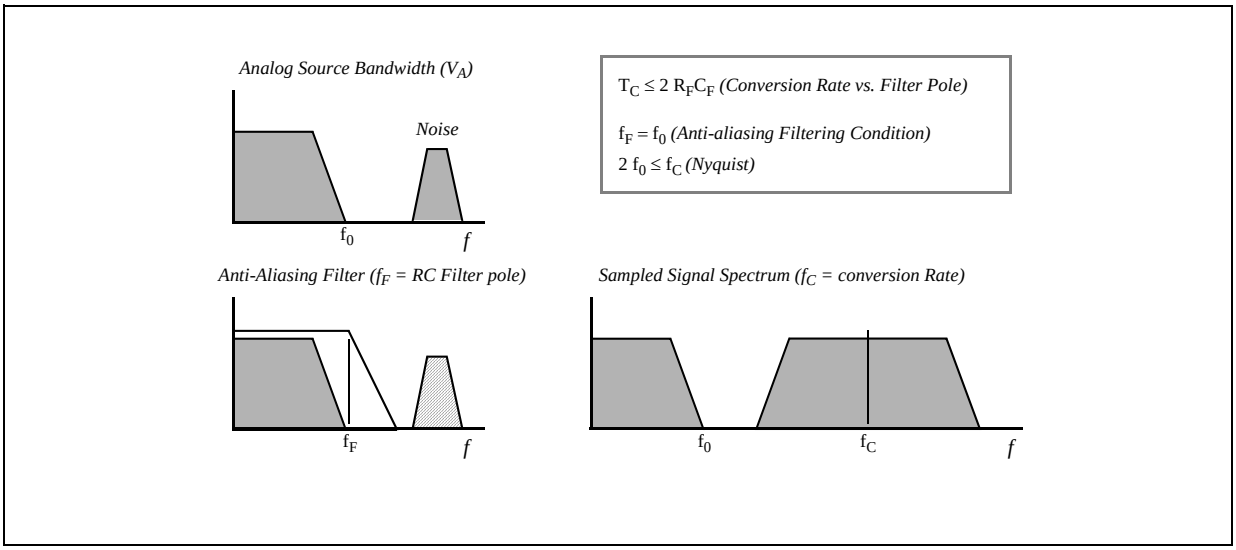
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 12. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to

Table 27. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
IS1WWINJ			(double ADC channel)				
	C	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	Vref = 3.3V	67	—	—	dB
SNR	T	Signal-to-noise ratio	Vref = 5.0V	69	—	—	dB
THD	T	Total harmonic distortion	—	-65	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$	T	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
			With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$	P	Total unadjusted error for IS1WWINJ (double ADC channels)	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1. T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.
4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time Tsample, but only the time for determining the digital result.
6. See *Figure 10*.
7. For the 144-pin package
8. No missing codes

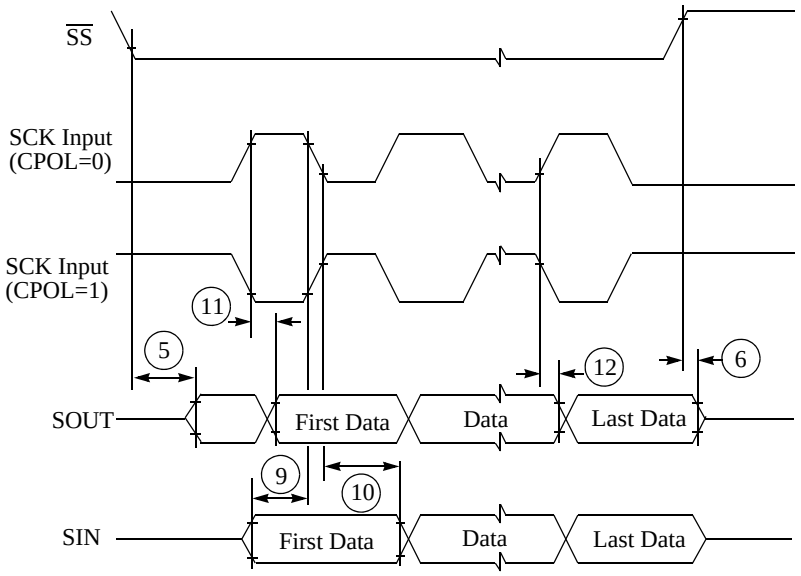
3.17 Flash memory electrical characteristics

Table 28. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Typ (1)	Initial Max (2)	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	*[4]	Double word (64 bits) program time[4]	30	—	500	µs
2	$T_{PPROGRAM}$	*[4]	Page(128 bits) program time[4]	40	160	500	µs
3	$T_{16KPPERASE}$	*[4]	16 KB block pre-program and erase time	250	1000	5000	ms
4	$T_{48KPPERASE}$	*[4]	48 KB block pre-program and erase time	400	1500	5000	ms
5	$T_{64KPPERASE}$	*[4]	64 KB block pre-program and erase time	450	1800	5000	ms
6	$T_{128KPPERASE}$	*[4]	128 KB block pre-program and erase time	800	2600	7500	ms
7	$T_{256KPPERASE}$	*[4]	256 KB block pre-program and erase time	1400	5200	15000	ms

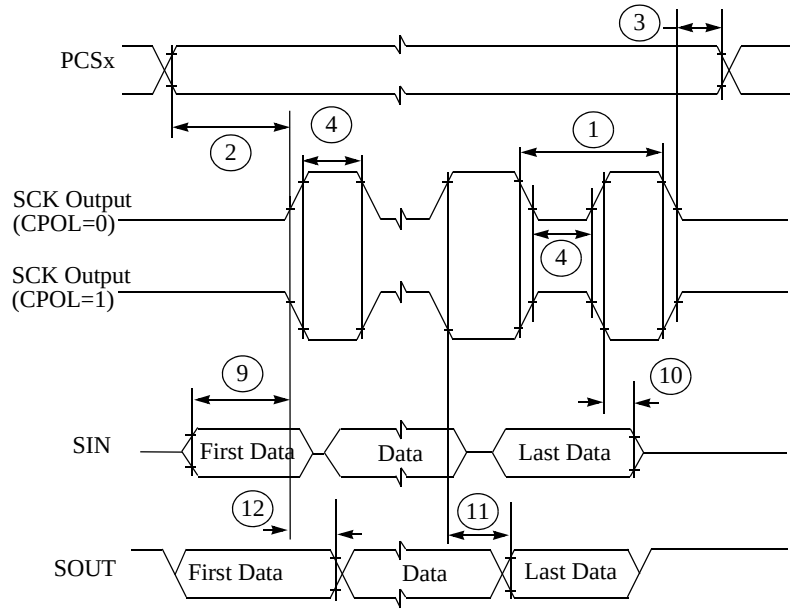
1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25°C. These values are characterized, but not tested.

Figure 35. DSPI classic SPI timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 36. DSPI modified transfer format timing — master, CPHA = 0



Note: The numbers shown are referenced in *Table 41*.

Table 42. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 45. Document revision history

Date	Revision	Changes
23-Mar-2011	6 (continued)	In the “Supply current characteristics (cut2)“ table: – Changed “$I_{DD\_LV\_MAX}$” to “$I_{DD\_LV\_MAX}$“; – Removed all “40-120 MHz” frequency ranges from the “Conditions” column; – Updated the “Max” values column; – Added parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ with “P” classification and special footnote; – Changed all “25°C“ temperature conditions to “ambient”; – Added “T_J = 150 °C“ condition to parameters $I_{DD\_HV\_ADC}$, $I_{DD\_HV\_AREF}$, $I_{DD\_HV\_OSC}$, and $I_{DD\_HV\_FLASH}$. Changed the timing diagram in the “Main oscillator electrical characteristics” section to reference MTRANS assertion instead of V_{DDMIN}. Updated the jitter specs in the “FMPLL electrical characteristics“ table. In the “ADC conversion characteristics“ table, changed all parameters with units of “counts” to units of “LSB” and updated Min/Max values. Changed $I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$ operating current (for both cases) to TBD. In the “Supply current characteristics (cut2)” section, added a footnote that $I_{DD\_HV\_ADC}$ and $I_{DD\_HV\_AREF}$ represent the total current of both ADCs in the “Current consumption characteristics” table. In the “ADC conversion characteristics” table: – Changed DNL min from -2 to -1. – Changed OFS min from -2 to -6. – Changed OFS max from 2 to 6. – Changed GNE min from -2 to -6. – Changed GNE max from 2 to 6. – Changed SNR min from 69 to 67. – Changed TUE min (without current injection) from -6 to -8. – Changed TUE max (without current injection) from 6 to 8. – Changed TUE min (with current injection) from -8 to -10. Changed TUE max (with current injection) from 8 to 10.

Table 45. Document revision history

Date	Revision	Changes
01-Aug-2012	8 (cont.)	– In *Table 20: Voltage regulator electrical specifications*, changed the “Digital supply high voltage detector upper threshold low limit (After a destructive reset initialization phase completion)” from 1.43V to 1.38V. – Added *Table 20: Voltage regulator electrical specifications*. – Updated the IDD values in *Table 22: Current consumption characteristics*. Changed conditions text from “1.2 supplies during LBIST (full LBIST configuration)” to “1.2 V supplies” for all the IDD parameters except $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. Added footnote in “Conditions” for the DPM mode. – Removed Cut references from the whole document. In *Table 27: ADC conversion characteristics*, changed the sampling frequency value from ‘1 MHz’ to ‘983.6 KHz’.
31-Jul-2013	9	– Updated *Table 20: Voltage regulator electrical specifications* (Voltage regulator electrical specifications) – Added Digital supply low voltage detector lower threshold and Digital supply low voltage detector upper threshold – Updated Main High Voltage Power-Low Voltage Detection value to 2.93 V – Replaced IEC with ISO26262 in *Section 1.1: Document overview*, – *Table 1* (SPC56XL60/54 device summary)-removed KGD – *Table 26* (16 MHz RC oscillator electrical characteristics) modified fRC values – Updated*Table 28* (Flash memory program and erase electrical specifications) – Updated *Table 27* (ADC conversion characteristics)-tconv to teval and associated footnote – Updated *Table 21* (DC electrical characteristics) – added VIH footnote – Updated IOL, IOH value for Fast pads – Updated *Table 33* (RESET sequences)-TDRB and TELRB – Updated *Table 20* (Voltage regulator electrical specifications)-combined ESR of external capacitor values – Updated *Section 3.16.1: Input Impedance and ADC Accuracy* -replaced fc by fs – *Table 7* (System pins)s-added footnote to RESET pin about weak pull down – Updated Injection current information in *Table 21* (DC electrical characteristics)-IINJ, *Table 9* (Absolute maximum ratings)-footnote 4 – Updated *Table 22* (Current consumption characteristics) for the following: – specified oscillator bypass mode and crystal oscillator mode – Updated STOP and HALT mode values – Added IDD_HV_PMU – footnote 2, footnote 3 – Added footnote $V_{DD\_HV\_ADRx}$ must always be applied and should be stable before LBIST starts. to *Table 10* (Recommended operating conditions (3.3 V)). – Added footnote to *Section 5: Ordering information* – Edit changes to *Section 3.6: Electromagnetic Interference (EMI) characteristics* – Updated *Equation 11*.