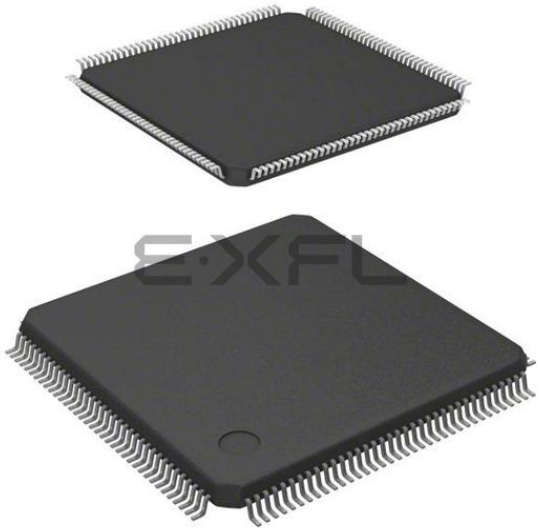

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564l54l5cbfsr

List of tables

1.3 Device comparison

Table 1. SPC56ELx/SPC564Lx device summary

Feature		SPC56EL60	SPC56EL54
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)	
	Architecture	Harvard	
	Execution speed	0–120 MHz (+2% FM)	
	DMIPS intrinsic performance	>240 MIPS	
	SIMD (DSP + FPU)	Yes	
	MMU	16 entry	
	Instruction set PPC	Yes	
	Instruction set VLE	Yes	
	Instruction cache	4 KB, EDC	
	MPU-16 regions	Yes, replicated module	
	Semaphore unit (SEMA4)	Yes	
Buses	Core bus	AHB, 32-bit address, 64-bit data	
	Internal periphery bus	32-bit address, 32-bit data	
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3	
Memory	Flash	1 MB, ECC, RWW	768 KB, ECC, RWW
	Static RAM (SRAM)	128 KB, ECC	96 KB, ECC

Table 1. SPC56ELx/SPC564Lx device summary (continued)

Feature		SPC56EL60	SPC56EL54
Modules	Interrupt Controller (INTC)	16 interrupt levels, replicated module	
	Periodic Interrupt Timer (PIT)	1 × 4 channels	
	System Timer Module (STM)	1 × 4 channels, replicated module	
	Software Watchdog Timer (SWT)	Yes, replicated module	
	eDMA	16 channels, replicated module	
	FlexRay	1 × 64 message buffers, dual channel	
	FlexCAN	2 × 32 message buffers	
	LINFlexD (UART and LIN with DMA support)	2	
	Clock out	Yes	
	Fault Collection and Control Unit (FCCU)	Yes	
	Cross Triggering Unit (CTU)	Yes	
	eTimer	3 × 6 channels(1)	
	FlexPWM	2 Module 4 × (2 + 1) channels(2)	
	Analog-to-Digital Converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)	
	Sine Wave Generator (SWG)	32 point	
Modules (cont.)	Deserial Serial Peripheral Interface (DSPI)	3 × DSPI as many as 8 chip selects	
	Cyclic Redundancy Checker (CRC) unit	Yes	
	Junction temperature sensor (TSENS)	Yes, replicated module	
	Digital I/Os	≥ 16	
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die	
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V	
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4 – 40 MHz	
Debug	Nexus	Level 3+	
Packages	LQFP	100 pins 144 pins	
	LBGA(3)	LBGA257	

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow block for test, censorship device and user option bits
- Wait states:
  - 3 wait states for frequencies =< 120 MHz
  - 2 wait states for frequencies =< 80 MHz
  - 1 wait state for frequencies =< 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The SPC56ELx/SPC564Lx SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

1.5.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Each device has two FMPLLs.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Output divider (ODF) for reduced frequency operation without re-lock
- 3 modes of operation
  - Bypass mode
  - Normal FMPLL mode with crystal reference (default)
  - Normal FMPLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

1.5.15 Main oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

1.5.16 Internal Reference Clock (RC) oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

The SWT module is replicated for each processor.

1.5.21 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ, Functional Reset, Destructive Reset, or Safe mode entered)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.5.22 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.5.23 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

1.5.24 Boot Assist Module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System Status and Configuration Module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification

1.5.37 Junction temperature sensor

The junction temperature sensor provides a value via an ADC channel that can be used by software to calculate the device junction temperature.

The key parameters of the junction temperature sensor include:

- Nominal temperature range from –40 to 150 °C
- Software temperature alarm via analog ADC comparator possible

1.5.38 Nexus Port Controller (NPC)

The NPC module provides real-time development support capabilities for this device in compliance with the IEEE-ISTO 5001-2003. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

The NPC block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2003 Class 3+, including selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the Power Architecture internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Full and reduced port modes
- MCKO (message clock out) pin
- 4 or 12 MDO (message data out) pins[b]
- 2 $\overline{\text{MSEO}}$ (message start/end out) pins
- $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
- $\overline{\text{EVTI}}$ (event in) pin
- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Supports JTAG mode
- Host processor (e200) development support features
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches,

b. 4 MDO pins on LQFP144 package, 12 MDO pins on LFBGA257 package.

Figure 3. SPC56ELx/SPC564Lx LQFP144 pinout (top view)

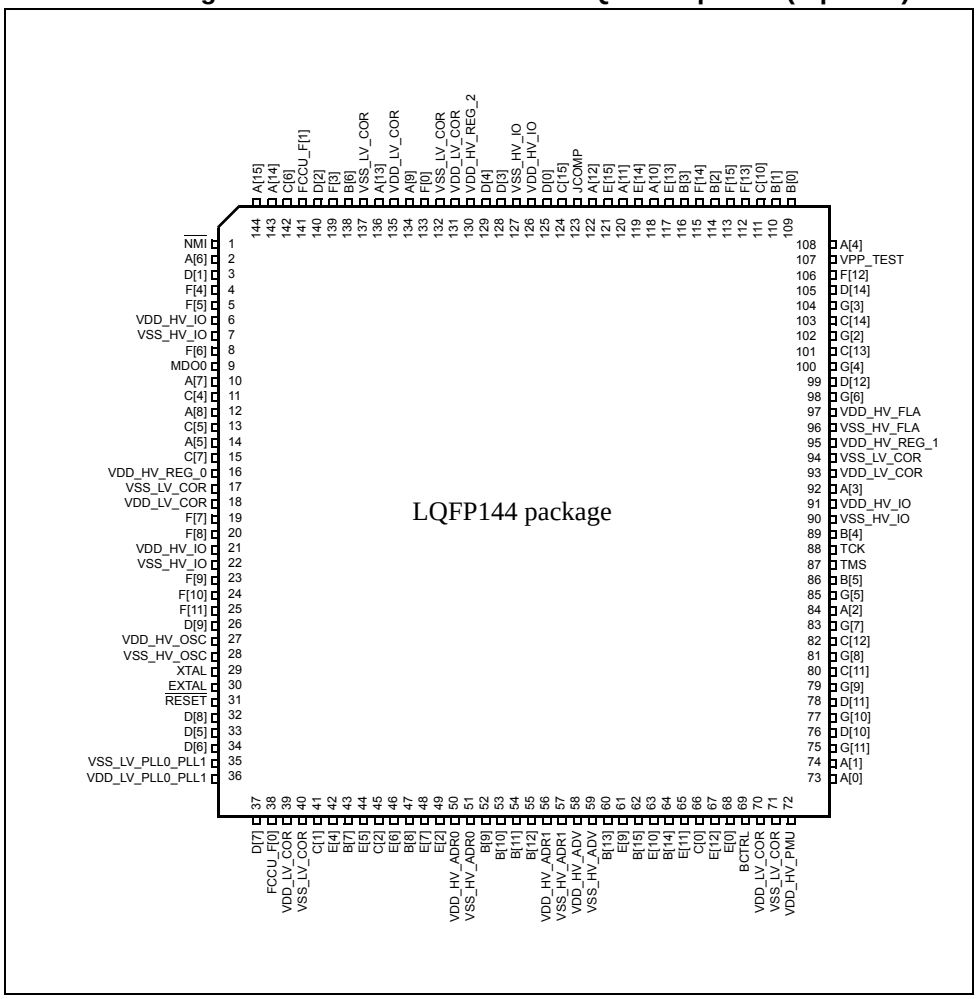


Figure 4 shows the SPC56ELx/SPC564Lx in the LFBGA257 package.

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
62	$V_{SS\_HV\_IO}$	—		
63	$V_{DD\_HV\_IO}$	—		
64	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
65	$V_{DD\_LV\_COR}$	—		
66	$V_{SS\_LV\_COR}$	—		
67	$V_{DD\_HV\_REG\_1}$	—		
68	$V_{SS\_HV\_FLA}$	—		
69	$V_{DD\_HV\_FLA}$	—		
70	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
71	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
72	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
73	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
74	V_{PP_TEST}(1)	—		
75	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
144	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1. V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 5. LFBGA257 pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
A1	$V_{SS\_HV\_IO\_RING}$	—		
A2	$V_{SS\_HV\_IO\_RING}$	—		
A3	$V_{DD\_HV\_IO\_RING}$	—		
A4	H[2]	SIUL	GPIO[114]	GPIO[114]
		NPC	MDO[5]	—

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
B[6]	PCR[22]	SIUL	GPIO[22]	ALT0	GPIO[22]	—	—	F	S	96	138	B3
		MC_CGM	clk_out	ALT1	—	—						
		DSPI_2	CS2	ALT2	—	—						
		SIUL	—		EIRQ[18]	—						
B[7]	PCR[23]	SIUL	—	ALT0	GPI[23]	—	—	—	—	30	43	R5
		LINFlexD_0	—	—	RXD	PSMI[31]; PADSEL=1						
		ADC_0	—	—	AN[0](3)	—						
B[8]	PCR[24]	SIUL	—	ALT0	GPI[24]	—	—	—	—	31	47	P7
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=2						
		ADC_0	—	—	AN[1](3)	—						
B[9]	PCR[25]	SIUL	—	ALT0	GPI[25]	—	—	—	—	35	52	U7
		ADC_0 ADC_1	—	—	AN[11](3)	—						
B[10]	PCR[26]	SIUL	—	ALT0	GPI[26]	—	—	—	—	36	53	R8
		ADC_0 ADC_1	—	—	AN[12](3)	—						
B[11]	PCR[27]	SIUL	—	ALT0	GPI[27]	—	—	—	—	37	54	T8
		ADC_0 ADC_1	—	—	AN[13](3)	—						
B[12]	PCR[28]	SIUL	—	ALT0	GPI[28]	—	—	—	—	38	55	U8
		ADC_0 ADC_1	—	—	AN[14](3)	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	—	M	S	—	140	C5
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0						
		FlexRay	—	—	CB_RX	—						
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	—	SYM	S	89	128	A7
		FlexRay	CB_TX	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2						
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	—	SYM	S	90	129	B7
		FlexRay	CB_TR_EN	ALT1	—	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2						
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	—	M	S	22	33	N3
		DSPI_0	CS3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0						

2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.
3. The max input voltage on the ADC pins is the ADC reference voltage VDD_HV_ADRx.
4. Measured values are applicable to all modes of the pad i.e. IBE = 0/1 and / or APC= 0/1.

3.11 Supply current characteristics

Current consumption data is given in *Table 22*. These specifications are design targets and are subject to change per device characterization.

Table 22. Current consumption characteristics

Symbol		Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{DD\_LV\_FULL}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	50 mA+ 2.18 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	80 mA+ 2.50 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$(2)	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	26 + 2.10 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	41 mA+ 2.30 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies during LBIST (full LBIST configuration) T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	250	mA
			1.2 V supplies during LBIST (full LBIST configuration) T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	290	
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$(2)	P	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	279	mA
			T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	318	mA

Table 22. Current consumption characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_HV\_AREF}$[4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_REF}$ = 3.6 V	—	—	3	mA
			T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_REF}$ = 5.5 V	—	—	5	
$I_{DD\_HV\_OSC}$ (oscillator bypass mode)	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	900	µA
$I_{DD\_HV\_OSC}$ (crystal oscillator mode)	D	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	3.5	mA
$I_{DD\_HV\_FLASH}$[5]	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	4	mA
$I_{DD\_HV\_PMU}$	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	10	mA

1. Devices configured for DPM mode, single core only with Core 0 executing typical code at 120 MHz from SRAM and Core 1 in reset. If core execution mode not specified, the device is configured for LSM mode with both cores executing typical code at 120 MHz from SRAM.
2. Enabled Modules in 'Typical mode': FlexPWM0, ETimer0/1/2, CTU, SWG, DMA, FlexCAN0/1, LINFlex, ADC1, DSPI0/1, PIT, CRC, PLL0/1, I/O supply current excluded. If DPM mode is configured, Core_0 is active while Core_1 is in reset during the measurements.
3. Internal structures hold the input voltage less than VDDA + 1.0 V on all pads powered by VDDA supplies, if the maximum injection current specification is met and VDDA is within the operating voltage specifications.
4. This value is the total current for both ADCs.
5. VFLASH is only available in the calibration package.

3.12 Temperature sensor electrical characteristics

Table 23. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Min	Max	Unit
—	P	Accuracy	T_J = –40 °C to 150 °C	–10	10	°C
T_S	D	Minimum sampling period	—	4	—	µs

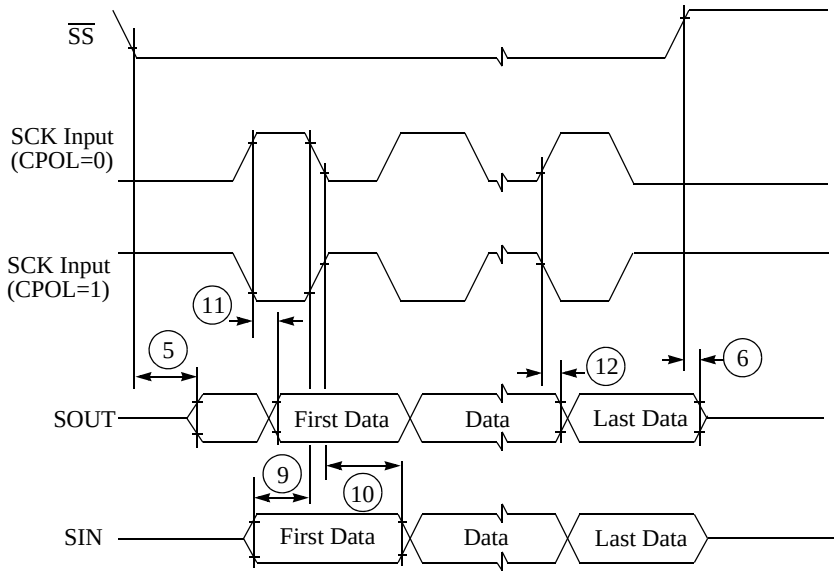
3.14 FMPLL electrical characteristics

Table 25. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range(1)	Crystal reference	4	—	40	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4	—	120(2)	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	20	—	150	MHz
f_{sys}	D	On-chip FMPLL frequency(2)	—	16	—	120	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window(3)	Lower limit	1.6	—	3.7	MHz
			Upper limit	24	—	56	
f_{SCM}	D	Self-clocked mode frequency(4),(5)	—	20	—	150	MHz
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs
t_{lpll}	D	FMPLL lock time (6),(7)	—	—	—	200	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter(8),(9),(10),(11)	Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum	–6	—	6	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 120 MHz, Input clock @ 4 MHz	—	—	175	ps
			PHI @ 100 MHz, Input clock @ 4 MHz	—	—	185	ps
			PHI @ 80 MHz, Input clock @ 4 MHz	—	—	200	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	–6	—	6	% $f_{FMPLLOUT}$
f_{UL}	D	Frequency un-LOCK range	—	–18	—	18	% $f_{FMPLLOUT}$
f_{CS} f_{DS}	D	Modulation depth	Center spread	±0.25	—	±2.0	% $f_{FMPLLOUT}$
			Down spread	–0.5	—	-8.0	
f_{MOD}	D	Modulation frequency(12)	—	—	—	100	kHz

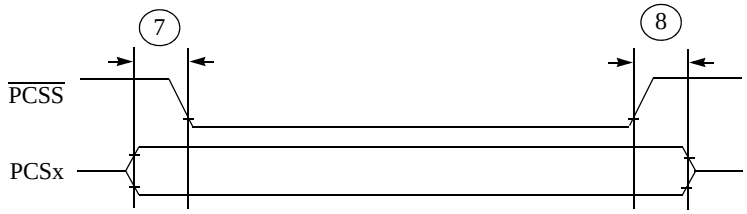
1. Considering operation with FMPLL not bypassed.

Figure 39. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 40. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing



Note: The numbers shown are referenced in *Table 41*.

Figure 42. LQFP144 package mechanical drawing

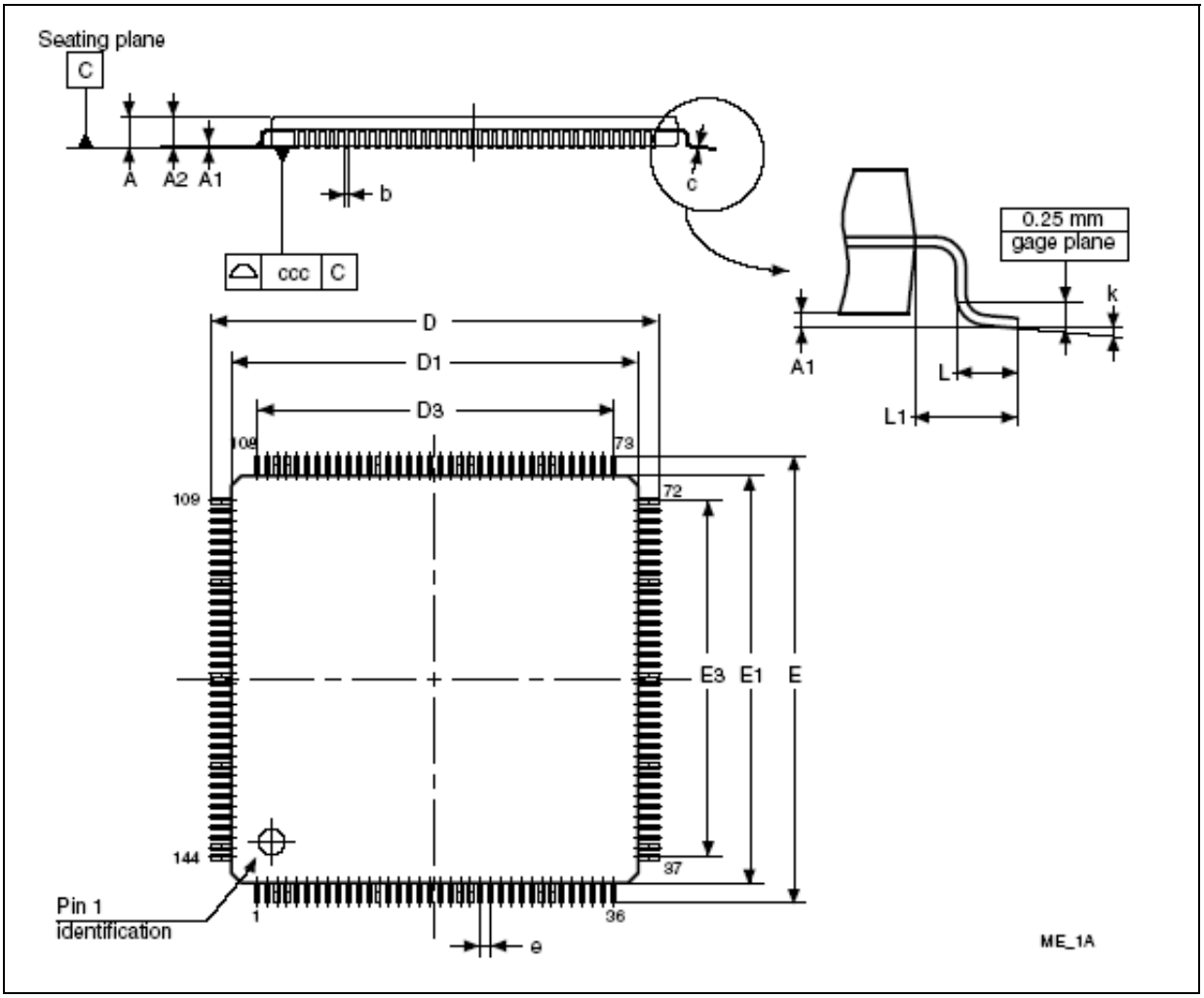


Table 43. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.0630
A1		0.05	0.15		0.0020	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	22	21.8	22.2	0.8661	0.8583	0.8740
D1	20	19.8	20.2	0.7874	0.7795	0.7953
D3	17.5			0.6890		
E	22	21.8	22.2	0.8661	0.8583	0.8740
E1	20	19.8	20.2	0.7874	0.7795	0.7953

Table 45. Document revision history

Date	Revision	Changes
23-Mar-2011	6 (continued)	Added symbol “CC” to the description in the “Introduction” section. Updated “Input leakage current” specs in the “DC electrical characteristics” table. Changed T_{ADC_S} to T_{sample} and T_{ADC_C} toT_{conv} in the “ADC conversion characteristics” table and footnotes. Removed “IINJ” from the “ADC conversion characteristics” table as this is included in IS1WIKNJ and IS1WWiNJ. Changed RESET_B to $\overline{\text{RESET}}$ in the "Reset sequence" section. Added the “Flash memory timing” table. Added cut2 specs for T_{DRB} and T_{ERLB} to the “Reset sequences” table. Added “WKUP/NMI Timing” subsection and “WKUP/NMI Glitch Filter” table to the “AC timing characteristics” section. Added “Nexus DDR Mode output timing” table to the “Nexus timing” section. Removed the “CLKOUT” diagram from the “External interrupt timing (IRQ pin)” section as it is not relevant. Corrected an error in the IRQ timing in the “External interrupt timing” figure. Updated the t_{SDC} parameters in the “DSPI timing” table. Renamed the “Electromagnetic Interference (EMI) characteristics” section (is “Electromagnetic Interference (EMI) characteristics (cut1)”) and revised all information in that section. In the “Voltage regulator electrical characteristics” section, added the BCX68 from Infineon to the list of supported transistors. Revised the “Voltage regulator electrical specifications” table to include cut1 and cut2 information. Renamed the “Supply current characteristics” section (is “Supply current characteristics (cut2)”) and revised it to show meaningful data. In the footnotes of the “Main oscillator electrical characteristics” table, changed SELMARGIN to XOSC_MARGIN. In the “ADC conversion characteristics” table: – Changed “LSB” to “Counts”. – Created separate rows for the TUE specifications. Removed the BGA row from the “Temperature” table entry. Added bullet regarding HALT and STOP in the “Clock, reset, power, mode and test control modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)” subsection of the “Features” section. In the “Analog-to-Digital Converter module “subsection of the “Feature Details” section, changed “Motor control mode” to “CTU mode” to be consistent with the nomenclature used in the Reference Manual. Updated the JCOMP entries in the “Pin function summary” table. Added footnotes regarding pad pull devices to NMI, TMS, TCK, and JCOMP in the “System pins” table. Added “Time constant of RC filter at LVD input” parameters to the “Main supply LVD (LVD Main) specifications” table.

Table 45. Document revision history

Date	Revision	Changes
23-Mar-2011	6 (continued)	In the “Supply current characteristics (cut2)“ table: – Changed “$I_{DD\_LV\_MAX}$” to “$I_{DD\_LV\_MAX}$“; – Removed all “40-120 MHz” frequency ranges from the “Conditions” column; – Updated the “Max” values column; – Added parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ with “P” classification and special footnote; – Changed all “25°C“ temperature conditions to “ambient”; – Added “T_J = 150 °C“ condition to parameters $I_{DD\_HV\_ADC}$, $I_{DD\_HV\_AREF}$, $I_{DD\_HV\_OSC}$, and $I_{DD\_HV\_FLASH}$. Changed the timing diagram in the “Main oscillator electrical characteristics” section to reference MTRANS assertion instead of V_{DDMIN}. Updated the jitter specs in the “FMPLL electrical characteristics“ table. In the “ADC conversion characteristics“ table, changed all parameters with units of “counts” to units of “LSB” and updated Min/Max values. Changed $I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$ operating current (for both cases) to TBD. In the “Supply current characteristics (cut2)” section, added a footnote that $I_{DD\_HV\_ADC}$ and $I_{DD\_HV\_AREF}$ represent the total current of both ADCs in the “Current consumption characteristics” table. In the “ADC conversion characteristics” table: – Changed DNL min from -2 to -1. – Changed OFS min from -2 to -6. – Changed OFS max from 2 to 6. – Changed GNE min from -2 to -6. – Changed GNE max from 2 to 6. – Changed SNR min from 69 to 67. – Changed TUE min (without current injection) from -6 to -8. – Changed TUE max (without current injection) from 6 to 8. – Changed TUE min (with current injection) from -8 to -10. Changed TUE max (with current injection) from 8 to 10.