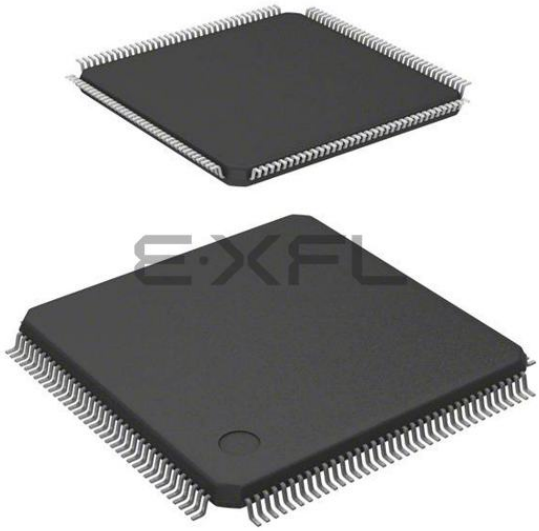

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564l54l5cbfsy

Figure 3. SPC56ELx/SPC564Lx LQFP144 pinout (top view)

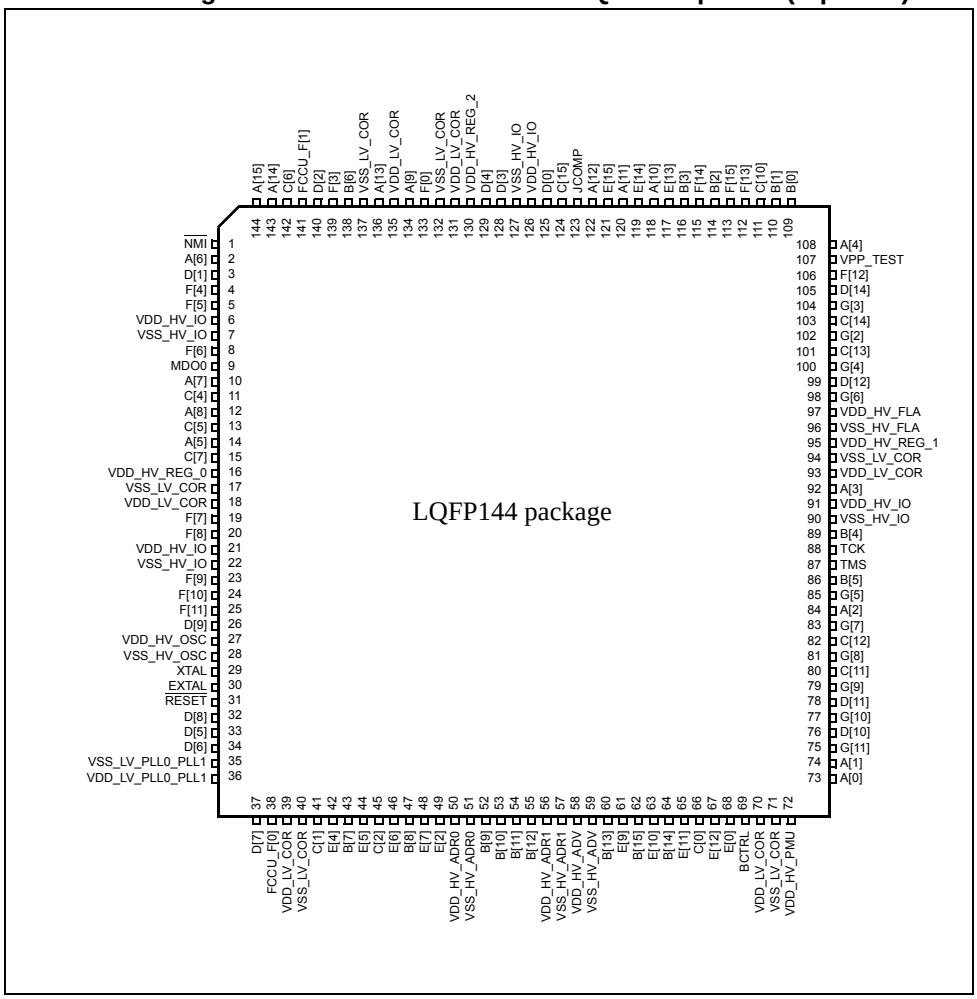


Figure 4 shows the SPC56ELx/SPC564Lx in the LFBGA257 package.

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
31	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
32	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
33	$V_{DD\_HV\_ADR0}$	—		
34	$V_{SS\_HV\_ADR0}$	—		
35	B[9]	SIUL	—	GPIO[25]
		ADC_0	—	AN[11]
		ADC_1		
36	B[10]	SIUL	—	GPIO[26]
		ADC_0	—	AN[12]
		ADC_1		
37	B[11]	SIUL	—	GPIO[27]
		ADC_0	—	AN[13]
		ADC_1		
38	B[12]	SIUL	—	GPIO[28]
		ADC_0	—	AN[14]
		ADC_1		
39	$V_{DD\_HV\_ADR1}$	—		
40	$V_{SS\_HV\_ADR1}$	—		
41	$V_{DD\_HV\_ADV}$	—		
42	$V_{SS\_HV\_ADV}$	—		
43	B[13]	SIUL	—	GPIO[29]
		LINFlexD_1	—	RXD
		ADC_1	—	AN[0]
44	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
45	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
46	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
47	BCTRL	—		

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
95	$V_{DD\_HV\_REG\_1}$	—		
96	$V_{SS\_HV\_FLA}$	—		
97	$V_{DD\_HV\_FLA}$	—		
98	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
99	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
100	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]
101	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
102	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
103	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
104	G[3]	SIUL	GPIO[99]	GPIO[99]
		FlexPWM_0	A[2]	A[2]
		eTimer_0	—	ETC[4]
105	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
106	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
107	V_{PP_TEST}(1)	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C9	I[0]	SIUL	GPIO[128]	GPIO[128]
		eTimer_2	ETC[0]	ETC[0]
		DSPI_0	CS4	—
		FlexPWM_1	—	FAULT[0]
C10	JCOMP	—	—	JCOMP
C11	H[11]	SIUL	GPIO[123]	GPIO[123]
		FlexPWM_1	A[2]	A[2]
C12	I[1]	SIUL	GPIO[129]	GPIO[129]
		eTimer_2	ETC[1]	ETC[1]
		DSPI_0	CS5	—
		FlexPWM_1	—	FAULT[1]
C13	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
C14	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
C15	$V_{SS\_HV\_IO\_RING}$	—		
C16	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
C17	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
D1	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
D2	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
D3	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]
D4	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
D5	$V_{SS\_LV\_CORE\_RING}$	—		
D6	$V_{DD\_LV\_CORE\_RING}$	—		
D7	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
D8	$V_{DD\_HV\_IO\_RING}$	—		
D9	$V_{SS\_HV\_IO\_RING}$	—		
D10	Not connected	—		
D11	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
D12	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
D13	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
D14	$V_{DD\_HV\_IO\_RING}$	—		
D15	V_{PP_TEST}(1)	—		
D16	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[6]	PCR[6]	SIUL	GPIO[6]	ALT0	GPIO[6]	—	—	M	S	2	2	G4
		DSPI_1	SCK	ALT1	SCK	—						
		SIUL	—	—	EIRQ[6]	—						
A[7]	PCR[7]	SIUL	GPIO[7]	ALT0	GPIO[7]	—	—	M	S	4	10	F3
		DSPI_1	SOUT	ALT1	—	—						
		SIUL	—	—	EIRQ[7]	—						
A[8]	PCR[8]	SIUL	GPIO[8]	ALT0	GPIO[8]	—	—	M	S	6	12	F4
		DSPI_1	—	—	SIN	—						
		SIUL	—	—	EIRQ[8]	—						
A[9]	PCR[9]	SIUL	GPIO[9]	ALT0	GPIO[9]	—	—	M	S	94	134	B6
		DSPI_2	CS1	ALT1	—	—						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=0						
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	—	M	S	81	118	A13
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1						
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0						
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0						
		SIUL	—	—	EIRQ[9]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S	82	120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S	83	122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	—	M	S	95	136	C6
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1						
		SIUL	—	—	EIRQ[12]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—	43	60	R10
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=0						
		ADC_1	—	—	AN[0](3)	—						
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—	44	64	P11
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2						
		SIUL	—	—	EIRQ[19]	—						
		ADC_1	—	—	AN[1](3)	—						
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—	—	62	R11
		SIUL	—	—	EIRQ[20]	—						
		ADC_1	—	—	AN[2](3)	—						
Port C												
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—	45	66	R12
		ADC_1	—	—	AN[3](3)	—						
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—	—	41	T4
		ADC_0	—	—	AN[2](3)	—						
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—	—	45	U5
		ADC_0	—	—	AN[3](3)	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
H[11]	PCR[123]	SIUL	GPIO[123]	ALT0	GPIO[123]	—	—	M	S	—	—	C11
		FlexPWM_1	A[2]	ALT1	A[2]	—						
H[12]	PCR[124]	SIUL	GPIO[124]	ALT0	GPIO[124]	—	—	M	S	—	—	B10
		FlexPWM_1	B[2]	ALT1	B[2]	—						
H[13]	PCR[125]	SIUL	GPIO[125]	ALT0	GPIO[125]	—	—	M	S	—	—	G15
		FlexPWM_1	X[3]	ALT1	X[3]	—						
		eTimer_2	ETC[3]	ALT2	ETC[3]	PSMI[42]; PADSEL=0						
H[14]	PCR[126]	SIUL	GPIO[126]	ALT0	GPIO[126]	—	—	M	S	—	—	A12
		FlexPWM_1	A[3]	ALT1	A[3]	—						
		eTimer_2	ETC[4]	ALT2	ETC[4]	—						
H[15]	PCR[127]	SIUL	GPIO[127]	ALT0	GPIO[127]	—	—	M	S	—	—	J17
		FlexPWM_1	B[3]	ALT1	B[3]	—						
		eTimer_2	ETC[5]	ALT2	ETC[5]	—						
Port I												
I[0]	PCR[128]	SIUL	GPIO[128]	ALT0	GPIO[128]	—	—	M	S	—	—	C9
		eTimer_2	ETC[0]	ALT1	ETC[0]	PSMI[39]; PADSEL=1						
		DSPI_0	CS4	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[0]	—						

Table 11. Decoupling capacitors (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
C_{PMU1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		µF
C_{PMU2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{REG}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		20		µF
C_{IO1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{IO2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		470		pF
C_{FLA1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{FLA2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{OSC1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{OSC2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{PLL1}	SR	External decoupling / stability capacitor		22		100	nF
C_{ADR1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADR2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADR3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF
C_{ADV1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADV2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADV3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF

1. Capacitors shall be placed as close as possible to the respective pads.
2. Total ESR considering all decoupling capacitor close to the $V_{DD}/V_{SS\_LV\_CORy}$ pairs shall be between 1 mΩ and 100 mΩ.

Table 20. Voltage regulator electrical specifications (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
—		Main High Voltage Power - Low Voltage Detection, upper threshold	—	—	—	2.93	V
—	D	Main supply low voltage detector, lower threshold	—	2.6	—	—	V
—	D	Digital supply high voltage detector upper threshold	Before a destructive reset initialization phase completion	1.355	—	1.495	V
			After a destructive reset initialization phase completion	1.39	—	1.47	
—	D	Digital supply high voltage detector lower threshold	Before a destructive reset initialization phase completion	1.315	—	1.455	V
			After a destructive reset initialization phase completion	1.35	—	1.38	
—	D	Digital supply low voltage detector lower threshold	After a destructive reset initialization phase completion	1.080	—	1.140	V
—	D	Digital supply low voltage detector upper threshold	After a destructive reset initialization phase completion	1.16	—	1.22	V
—	D	Digital supply low voltage detector lower threshold	Before a destructive reset initialization phase	1.080	—	1.226	V
—	D	Digital supply low voltage detector upper threshold	Before a destructive reset initialization phase	1.160	—	1.306	V
—	D	POR rising/ falling supply threshold voltage	—	1.6	—	2.6	V
—	SR	Supply ramp rate	—	3 V/s	—	0.5 V/µs	—
—	D	LVD_MAIN: Time constant of RC filter at LVD input	3.3V noise rejection at the input of LVD comparator	1.1	—	—	µs
—	D	HVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs
—	D	LVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs

Table 27. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
IS1WWINJ			(double ADC channel)				
	C	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	Vref = 3.3V	67	—	—	dB
SNR	T	Signal-to-noise ratio	Vref = 5.0V	69	—	—	dB
THD	T	Total harmonic distortion	—	-65	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$	T	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
			With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$	P	Total unadjusted error for IS1WWINJ (double ADC channels)	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1. T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.
4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time Tsample, but only the time for determining the digital result.
6. See *Figure 10*.
7. For the 144-pin package
8. No missing codes

3.17 Flash memory electrical characteristics

Table 28. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Typ (1)	Initial Max (2)	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	*[4]	Double word (64 bits) program time[4]	30	—	500	µs
2	$T_{PPROGRAM}$	*[4]	Page(128 bits) program time[4]	40	160	500	µs
3	$T_{16KPPERASE}$	*[4]	16 KB block pre-program and erase time	250	1000	5000	ms
4	$T_{48KPPERASE}$	*[4]	48 KB block pre-program and erase time	400	1500	5000	ms
5	$T_{64KPPERASE}$	*[4]	64 KB block pre-program and erase time	450	1800	5000	ms
6	$T_{128KPPERASE}$	*[4]	128 KB block pre-program and erase time	800	2600	7500	ms
7	$T_{256KPPERASE}$	*[4]	256 KB block pre-program and erase time	1400	5200	15000	ms

1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25°C. These values are characterized, but not tested.

Figure 15. Destructive Reset Sequence, BIST disabled

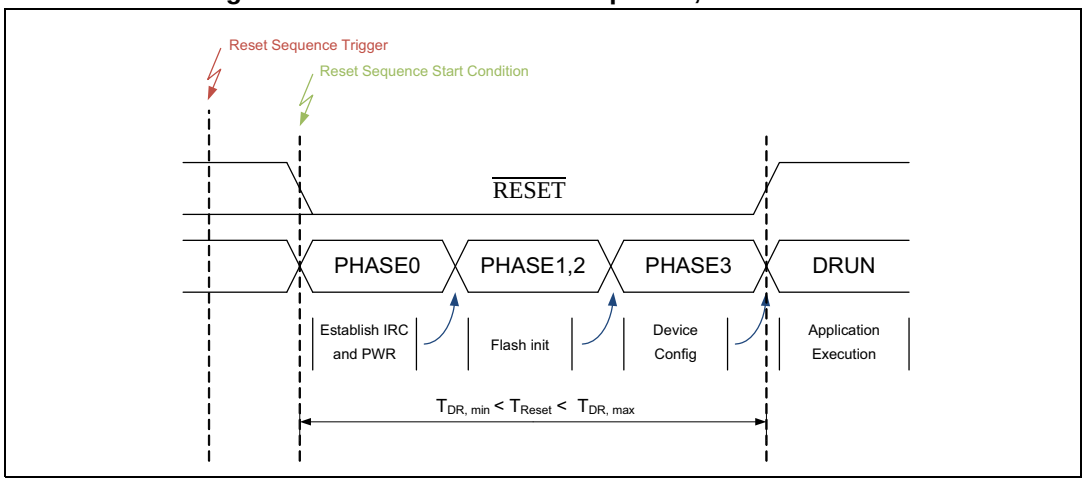


Figure 16. External Reset Sequence Long, BIST enabled

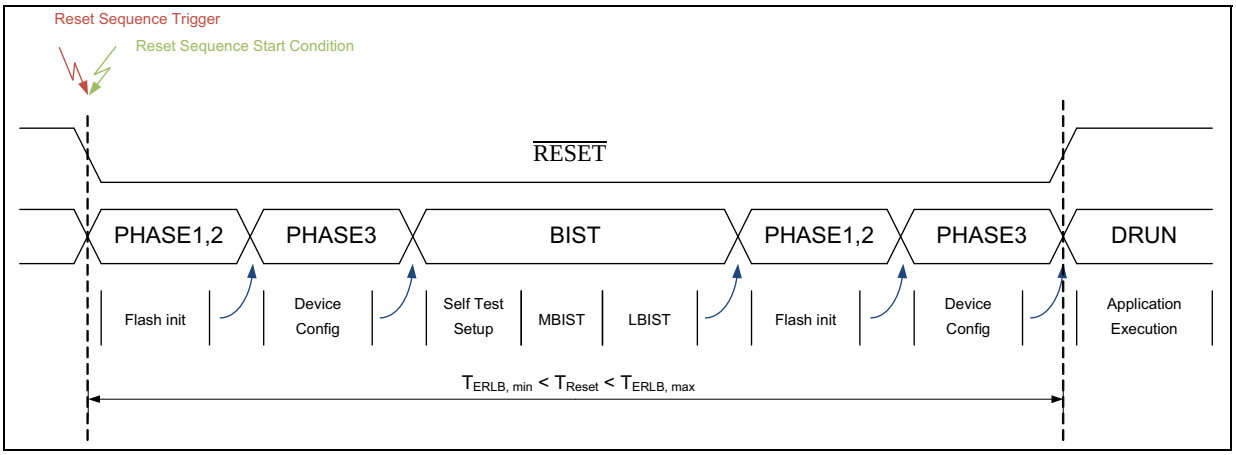


Figure 17. Functional Reset Sequence Long

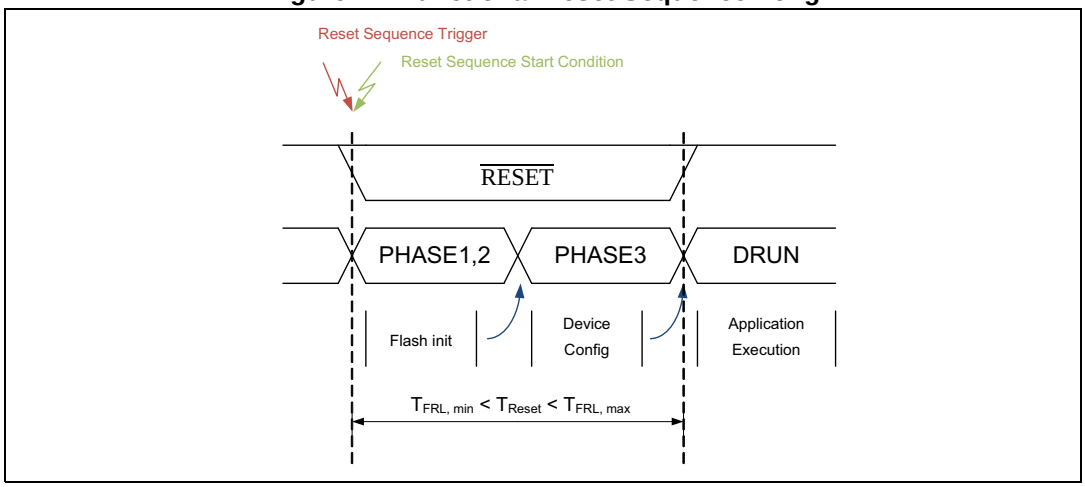


Table 39. Nexus debug port timing(1) (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	D	TDI, TMS Data Hold Time		5	—	ns
10	t_{JOV}	D	TCK Low to TDO/RDY Data Valid		0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

Figure 27. Nexus output timing

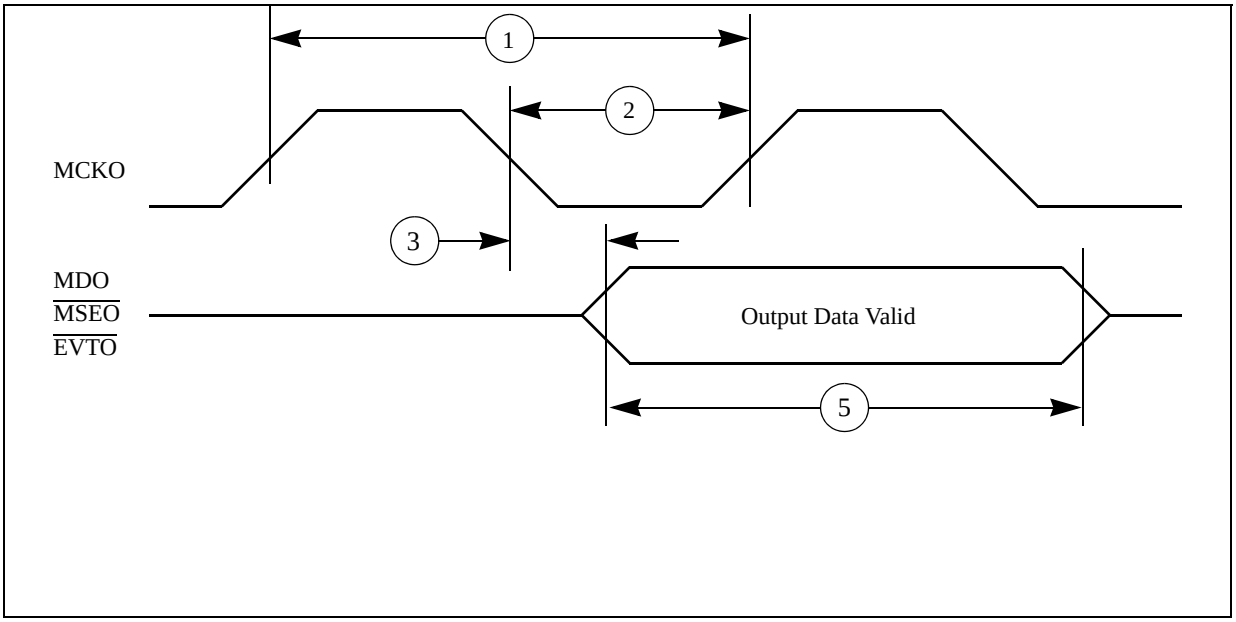


Figure 28. Nexus EVTI Input Pulse Width

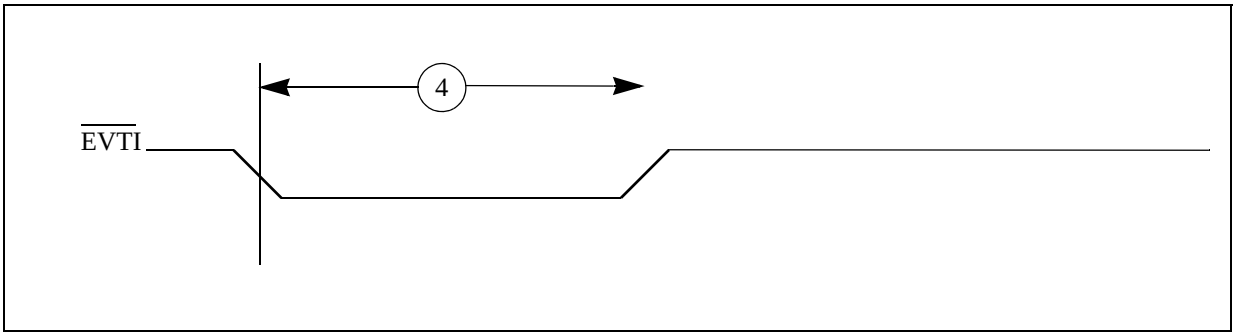
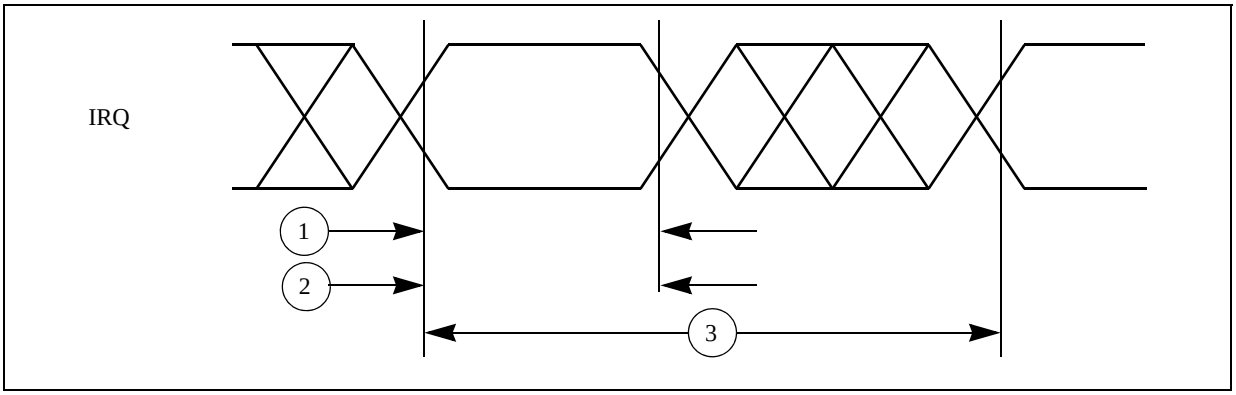


Figure 31. External interrupt timing

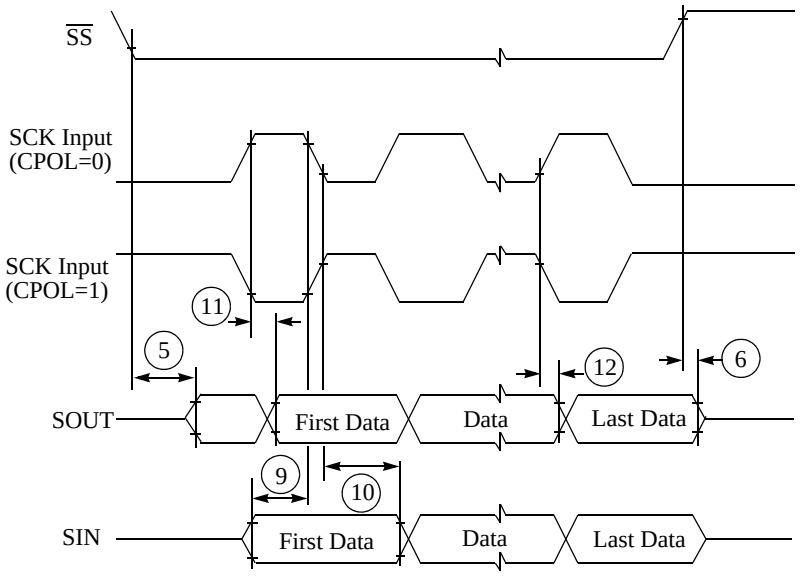


3.21.6 DSPI timing

Table 41. DSPI timing

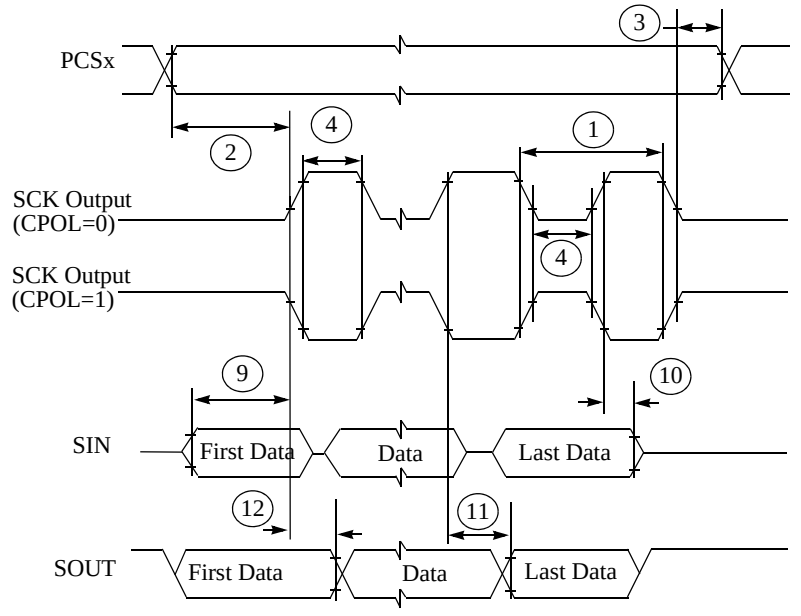
No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		D		Slave (MTFE = 0)	62	—	
		D		Slave Receive Only Mode(1)	16	—	
2	t_{CSC}	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	D	After SCK delay	—	16	—	ns
4	t_{SDC}	D	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	ns
5	t_A	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	12	
				Master (MTFE = 1, CPHA = 1)	—	4	

Figure 35. DSPI classic SPI timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 36. DSPI modified transfer format timing — master, CPHA = 0



Note: The numbers shown are referenced in *Table 41*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

Figure 41. LQFP100 package mechanical drawing

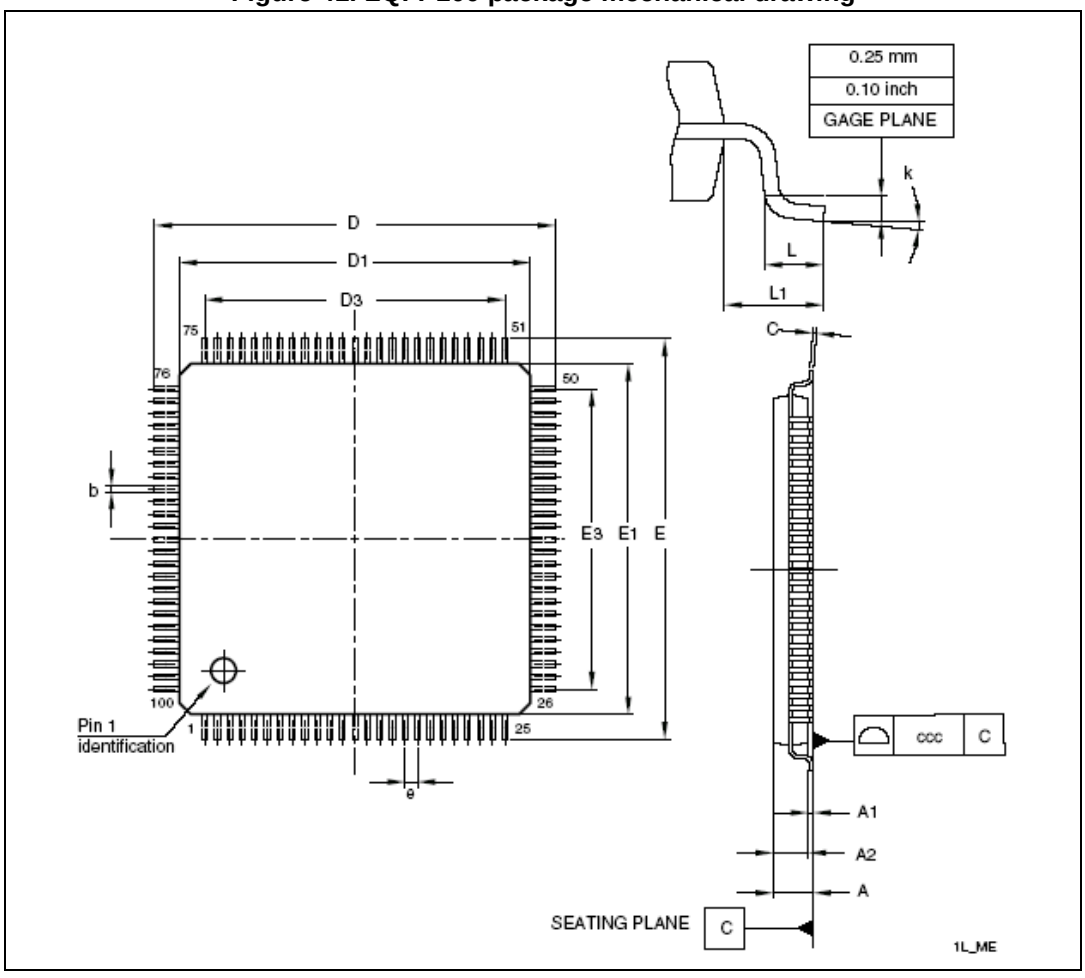


Table 45. Document revision history

Date	Revision	Changes
23-Mar-2011	6 (continued)	In the “Supply current characteristics (cut2)“ table: – Changed “$I_{DD\_LV\_MAX}$” to “$I_{DD\_LV\_MAX}$“; – Removed all “40-120 MHz” frequency ranges from the “Conditions” column; – Updated the “Max” values column; – Added parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ with “P” classification and special footnote; – Changed all “25°C“ temperature conditions to “ambient”; – Added “T_J = 150 °C“ condition to parameters $I_{DD\_HV\_ADC}$, $I_{DD\_HV\_AREF}$, $I_{DD\_HV\_OSC}$, and $I_{DD\_HV\_FLASH}$. Changed the timing diagram in the “Main oscillator electrical characteristics” section to reference MTRANS assertion instead of V_{DDMIN}. Updated the jitter specs in the “FMPLL electrical characteristics“ table. In the “ADC conversion characteristics“ table, changed all parameters with units of “counts” to units of “LSB” and updated Min/Max values. Changed $I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$ operating current (for both cases) to TBD. In the “Supply current characteristics (cut2)” section, added a footnote that $I_{DD\_HV\_ADC}$ and $I_{DD\_HV\_AREF}$ represent the total current of both ADCs in the “Current consumption characteristics” table. In the “ADC conversion characteristics” table: – Changed DNL min from -2 to -1. – Changed OFS min from -2 to -6. – Changed OFS max from 2 to 6. – Changed GNE min from -2 to -6. – Changed GNE max from 2 to 6. – Changed SNR min from 69 to 67. – Changed TUE min (without current injection) from -6 to -8. – Changed TUE max (without current injection) from 6 to 8. – Changed TUE min (with current injection) from -8 to -10. Changed TUE max (with current injection) from 8 to 10.

Table 45. Document revision history

Date	Revision	Changes
01-Aug-2012	8 (cont.)	– In *Section 1.5.31: eTimer module*" changed text from "The MPC5643L provides three eTimer modules on the 257 MAPBGA device, and two eTimer modules on the 144 LQFP package" to "The MPC5643L provides three eTimer modules (on the LQFP package eTimer_2 is available internally only without any external I/O access)". – In *Section 3.6: Electromagnetic Interference (EMI) characteristics*",added additional information at the end of this section. – In *Section 3.9: Voltage regulator electrical characteristics*, added text related to external ballast transistor. – In *Table 4: LQFP144 pin function summary* and *Table 5: LFBGA257 pin function summary*, moved EVTI from output function to input function. – In *Table 7: System pins*, changed the direction for EXTAL from "Output Only" to "Input/Output". – In*Table 7: System pins*, added table footnote for symbol "EXTAL". – Changed the row (TVdd) in *Table 9: Absolute maximum ratings*. – In *Table 9: Absolute maximum ratings*, Maximum value for "$V_{DD\_HV\_IOX}$" and "$V_{DD\_HV\_FLA}$" changed from "3.6" to "4.0". – In *Table 22: Current consumption characteristics*, added max value 250 and 290 mA for symbol $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. – Added five additional RunIDD parameters in *Table 22: Current consumption characteristics*. – In *Table 23: Temperature sensor electrical characteristics*, changed condition for parameter "Accuracy" from "-40°C to 25°C" to "-40°C to 150°C" – In *Table 25: FMPLL electrical characteristics*,added '150' to the max value for 'f_{SCM}' In *Table 26: 16 MHz RC oscillator electrical characteristics*,changes done are: f_{RC} symbol- Added min value '15.04' and max value '16.96'.Removed condition "T_J=25°C" Removed row containing Δ_{RCMVAR} symbol. – In *Figure 10: Input Equivalent Circuit*, added the name 'C_S' to the capacitor in the internal circuit scheme. – Removed references to Cut1 and Cut2: Renamed Section "Electromagnetic Interference (EMI) characteristics (cut1)" to "Electromagnetic Interference (EMI) characteristics". In *Table 27: ADC conversion characteristics*, removed reference to cut2 only for symbol 'IS1WINJ' and '$TUE_{IS1WWINJ}$'. In *Section 1.1: Document overview*, modified text to remove references to 'Cut1'. – In *Table 27: ADC conversion characteristics*, for t_{CONV} added '60 MHz' to 'conditions' and '600' to the 'Min' value. Separated SNR into two specifications with conditions Vref 3.3 V and 5.0 V respectively.