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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l3ccfqy

1.5.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Each device has two FMPLLs.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Output divider (ODF) for reduced frequency operation without re-lock
- 3 modes of operation
  - Bypass mode
  - Normal FMPLL mode with crystal reference (default)
  - Normal FMPLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

1.5.15 Main oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

1.5.16 Internal Reference Clock (RC) oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
52	B[9]	SIUL	—	GPIO[25]
		ADC_0 ADC_1	—	AN[11]
53	B[10]	SIUL	—	GPIO[26]
		ADC_0 ADC_1	—	AN[12]
54	B[11]	SIUL	—	GPIO[27]
		ADC_0 ADC_1	—	AN[13]
55	B[12]	SIUL	—	GPIO[28]
		ADC_0 ADC_1	—	AN[14]
56	$V_{DD\_HV\_ADR1}$	—		
57	$V_{SS\_HV\_ADR1}$	—		
58	$V_{DD\_HV\_ADV}$	—		
59	$V_{SS\_HV\_ADV}$	—		
60	B[13]	SIUL	—	GPIO[29]
		LINFlexD_1	—	RXD
		ADC_1	—	AN[0]
61	E[9]	SIUL	—	GPIO[73]
		ADC_1	—	AN[7]
62	B[15]	SIUL	—	GPIO[31]
		SIUL	—	EIRQ[20]
		ADC_1	—	AN[2]
63	E[10]	SIUL	—	GPIO[74]
		ADC_1	—	AN[8]
64	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
65	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
66	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
67	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
68	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
69	BCTRL	—		
70	$V_{DD\_LV\_COR}$	—		
71	$V_{SS\_LV\_COR}$	—		
72	$V_{DD\_HV\_PMU}$	—		
73	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
74	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
75	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
76	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
77	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]
78	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
79	G[9]	SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
		DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
80	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
K9	V_{SS_LV}	—		
K10	V_{SS_LV}	—		
K11	V_{SS_LV}	—		
K12	V_{DD_LV}	—		
K14	Not connected	—		
K15	H[8]	SIUL	GPIO[120]	GPIO[120]
		FlexPWM_1	A[1]	A[1]
		DSPI_0	CS6	—
K16	H[7]	SIUL	GPIO[119]	GPIO[119]
		FlexPWM_1	X[1]	X[1]
		eTimer_2	ETC[1]	ETC[1]
K17	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
L1	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	EVTO	—
L2	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	EVTI
L3	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
L4	Not connected	—		
L6	V_{DD_LV}	—		
L7	V_{SS_LV}	—		
L8	V_{SS_LV}	—		
L9	V_{SS_LV}	—		
L10	V_{SS_LV}	—		
L11	V_{SS_LV}	—		
L12	V_{DD_LV}	—		
L14	Not connected	—		
L15	TCK	—		

Table 6. Supply pins (continued)

Supply		Pin #		
Symbol	Description	100 pkg	144 pkg	257 pkg
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132	VSS_LV(2)
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	135	VDD_LV(1)
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	137	VSS_LV(2)

1. VDD_LV balls are tied together on the LFBGA257 substrate.
2. VSS_LV balls are tied together on the LFBGA257 substrate.
3. VDD_HV balls are tied together on the LFBGA257 substrate.
4. VSS_HV balls are tied together on the LFBGA257 substrate.

2.3 System pins

Table 7. System pins

Symbol	Description	Direction	Pin #		
			100 pkg	144 pkg	257 pkg
Dedicated pins					
MDO0(1)	Nexus Message Data Output — line	Output only	—	9	E1
NMI(2)	Non Maskable Interrupt	Input only	1	1	E4
XTAL	Input for oscillator amplifier circuit and internal clock generator	Input only	18	29	N1
EXTAL(3)	Oscillator amplifier output	Input/Output (4)	19	30	R1
TMS(2)	JTAG state machine control	Input only	59	87	M16
TCK(2)	JTAG clock	Input only	60	88	L15
JCOMP(5)	JTAG compliance select	Input only	84	123	C10
Reset pin					
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength. Output drive is open drain and must be terminated by an external resistor of value 1KOhm.(6)	Bidirectional	20	31	P2
Test pin					
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.		74	107	D15

1. This pad is configured for Fast (F) pad speed.

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[10]	PCR[42]	SIUL	GPIO[42]	ALT0	GPIO[42]	—	—	M	S	78	111	A15
		DSPI_2	CS2	ALT1	—	—						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=0						
C[11]	PCR[43]	SIUL	GPIO[43]	ALT0	GPIO[43]	—	—	M	S	55	80	M14
		eTimer_0	ETC[4]	ALT1	ETC[4]	PSMI[7]; PADSEL=1						
		DSPI_2	CS2	ALT2	—	—						
C[12]	PCR[44]	SIUL	GPIO[44]	ALT0	GPIO[44]	—	—	M	S	56	82	N15
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=0						
		DSPI_2	CS3	ALT2	—	—						
C[13]	PCR[45]	SIUL	GPIO[45]	ALT0	GPIO[45]	—	—	M	S	71	101	F15
		eTimer_1	ETC[1]	ALT1	ETC[1]	PSMI[10]; PADSEL=0						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=0						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=0						
C[14]	PCR[46]	SIUL	GPIO[46]	ALT0	GPIO[46]	—	—	M	S	72	103	E15
		eTimer_1	ETC[2]	ALT1	ETC[2]	PSMI[11]; PADSEL=1						
		CTU_0	EXT_TGR	ALT2	—	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	—	M	S	—	140	C5
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0						
		FlexRay	—	—	CB_RX	—						
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	—	SYM	S	89	128	A7
		FlexRay	CB_TX	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2						
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	—	SYM	S	90	129	B7
		FlexRay	CB_TR_EN	ALT1	—	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2						
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	—	M	S	22	33	N3
		DSPI_0	CS3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
E[4]	PCR[68]	SIUL	—	ALT0	GPI[68]	—	—	—	—	—	42	U4
		ADC_0	—	—	AN[7](3)	—						
E[5]	PCR[69]	SIUL	—	ALT0	GPI[69]	—	—	—	—	—	44	T5
		ADC_0	—	—	AN[8](3)	—						
E[6]	PCR[70]	SIUL	—	ALT0	GPI[70]	—	—	—	—	—	46	R6
		ADC_0	—	—	AN[4](3)	—						
E[7]	PCR[71]	SIUL	—	ALT0	GPI[71]	—	—	—	—	—	48	T6
		ADC_0	—	—	AN[6](3)	—						
E[9]	PCR[73]	SIUL	—	ALT0	GPI[73]	—	—	—	—	—	61	T10
		ADC_1	—	—	AN[7](3)	—						
E[10]	PCR[74]	SIUL	—	ALT0	GPI[74]	—	—	—	—	—	63	T11
		ADC_1	—	—	AN[8](3)	—						
E[11]	PCR[75]	SIUL	—	ALT0	GPI[75]	—	—	—	—	—	65	U11
		ADC_1	—	—	AN[4](3)	—						
E[12]	PCR[76]	SIUL	—	ALT0	GPI[76]	—	—	—	—	—	67	T12
		ADC_1	—	—	AN[6](3)	—						
E[13]	PCR[77]	SIUL	GPIO[77]	ALT0	GPIO[77]	—	—	M	S	—	117	D12
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=1						
		DSPI_2	CS3	ALT2	—	—						
		SIUL	—	—	EIRQ[25]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	—	M	S	—	—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	—	M	S	—	—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	—	M	S	—	—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	—	F	S	—	—	K3
		NPC	RDY	ALT2	—	—						

1. Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)
2. The default function of this pin out of reset is ALT1 (TDO).
3. Analog

Note: Open Drain can be configured by the PCRn for all pins used as output (except FCCU_F[0] and FCCU_F[1]).

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	4.5(2), (3)	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	4.5 (2), (3)	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	4.5 (2), (3)	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.5 (2), (3)	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADR0}$ (2)(3) $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.4 (2)	V

Table 10. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_AD0}$ $V_{SS\_HV\_AD1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD\_LV\_REGCOR}$(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(5)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_PLL}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	$f_{CPU} \leq 120$ MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. $V_{DD\_HV\_ADR0}$ and $V_{DD\_HV\_ADR1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.
3. $V_{DD\_HV\_ADRx}$ must always be applied and should be stable before LBIST starts. If this supply is not above its absolute minimum level, LBIST operations can fail.
4. Can be connected to emitter of external NPN. Low voltage supplies are not under user control. They are produced by an on-chip voltage regulator.
5. For the device to function properly, the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter, if one is used.

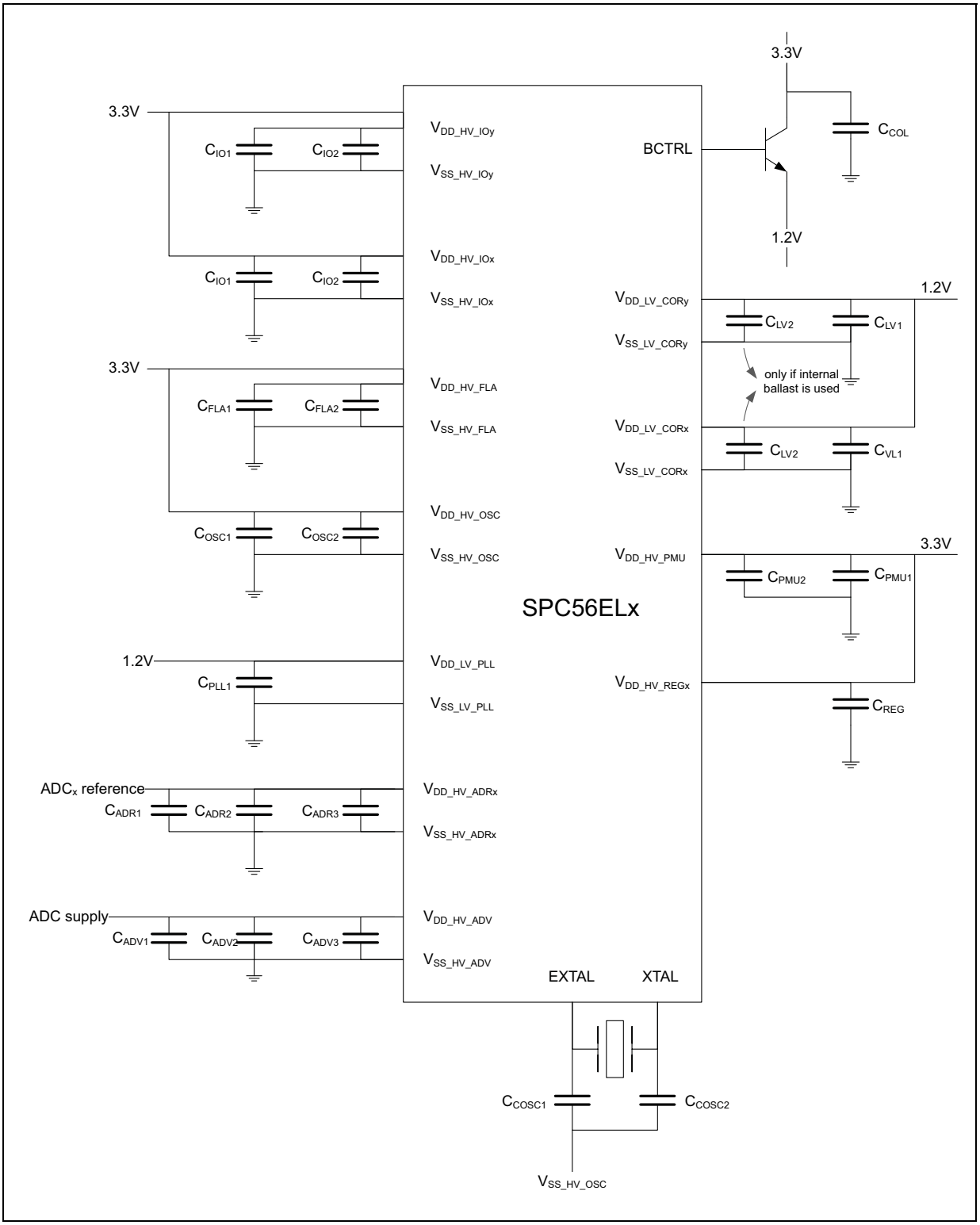
3.4 Decoupling capacitors

The internal voltage regulator requires an external NPN ballast and some additional decoupling capacitors. These capacitors shall be placed on the board as close as possible to the associated pin.

Table 11. Decoupling capacitors

Symbol		Parameter	Conditions(1)	Value			Unit
				Min	Typ	Max	
C_{COL}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Max ESR = 100 mΩ.		20		µF
C_{LV1}	SR	External decoupling / stability capacitor	Sum of C_{LV1} placed close to $V_{DD}/V_{SS\_LV\_CORy}$ pairs(2).	12µF		40µF	µF
C_{LV2}	SR	External decoupling / stability capacitor	Sum of C_{LV2} placed close to $V_{DD}/V_{SS\_LV\_CORy}$ pairs shall be between 300 nF and 900 nF.		100(2)		nF

Figure 5. Decoupling capacitors



Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$= junction to case thermal resistance (°C/W)

$R_{\theta CA}$= case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T= thermocouple temperature on top of the package (°C)

Ψ_{JT}= thermal characterization parameter (°C/W)

P_D= power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.5.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB on JEDEC site.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

2. With FM; the value does not include a possible +2% modulation
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the FMPLL is in self clocked mode.
4. Self clocked mode frequency is the frequency that the FMPLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} is the frequency at the output of the VCO; its range is 256–512 MHz.
   f_{SCM} is the self-clocked mode frequency (free running frequency); its range is 20–150 MHz.
   $f_{SYS} = f_{VCO} \div ODF$
6. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this FMPLL, load capacitors should not exceed these limits.
7. This specification applies to the period required for the FMPLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
8. This value is determined by the crystal manufacturer and board design.
9. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FMPLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
10. Proper PC board layout procedures must be followed to achieve specifications.
11. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
12. Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.15 16 MHz RC oscillator electrical characteristics

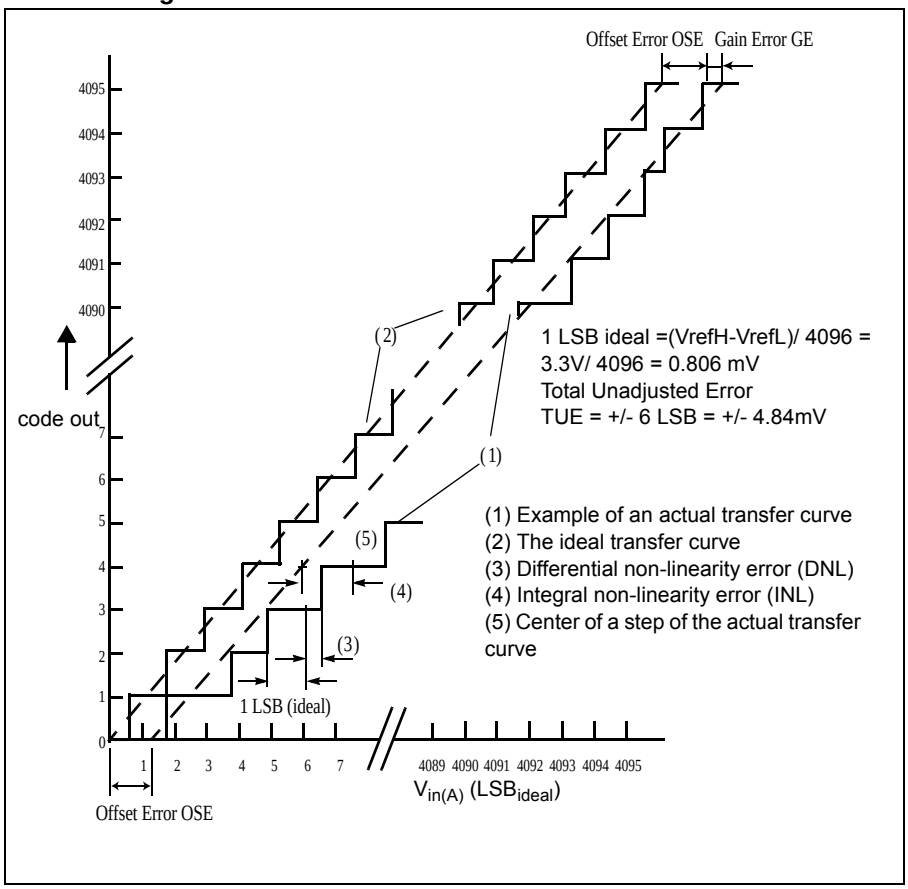
Table 26. 16 MHz RC oscillator electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%

3.16 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Figure 9. ADC characteristics and error definitions



3.16.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the *Equation 4*:

Table 27. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
IS1WWINJ			(double ADC channel)				
	C	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	Vref = 3.3V	67	—	—	dB
SNR	T	Signal-to-noise ratio	Vref = 5.0V	69	—	—	dB
THD	T	Total harmonic distortion	—	-65	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$	T	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
			With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$	P	Total unadjusted error for IS1WWINJ (double ADC channels)	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1. T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.
4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time Tsample, but only the time for determining the digital result.
6. See *Figure 10*.
7. For the 144-pin package
8. No missing codes

3.17 Flash memory electrical characteristics

Table 28. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Typ (1)	Initial Max (2)	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	*[4]	Double word (64 bits) program time[4]	30	—	500	µs
2	$T_{PPROGRAM}$	*[4]	Page(128 bits) program time[4]	40	160	500	µs
3	$T_{16KPPERASE}$	*[4]	16 KB block pre-program and erase time	250	1000	5000	ms
4	$T_{48KPPERASE}$	*[4]	48 KB block pre-program and erase time	400	1500	5000	ms
5	$T_{64KPPERASE}$	*[4]	64 KB block pre-program and erase time	450	1800	5000	ms
6	$T_{128KPPERASE}$	*[4]	128 KB block pre-program and erase time	800	2600	7500	ms
7	$T_{256KPPERASE}$	*[4]	256 KB block pre-program and erase time	1400	5200	15000	ms

1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25°C. These values are characterized, but not tested.

Figure 19. Reset sequence start for Destructive Resets

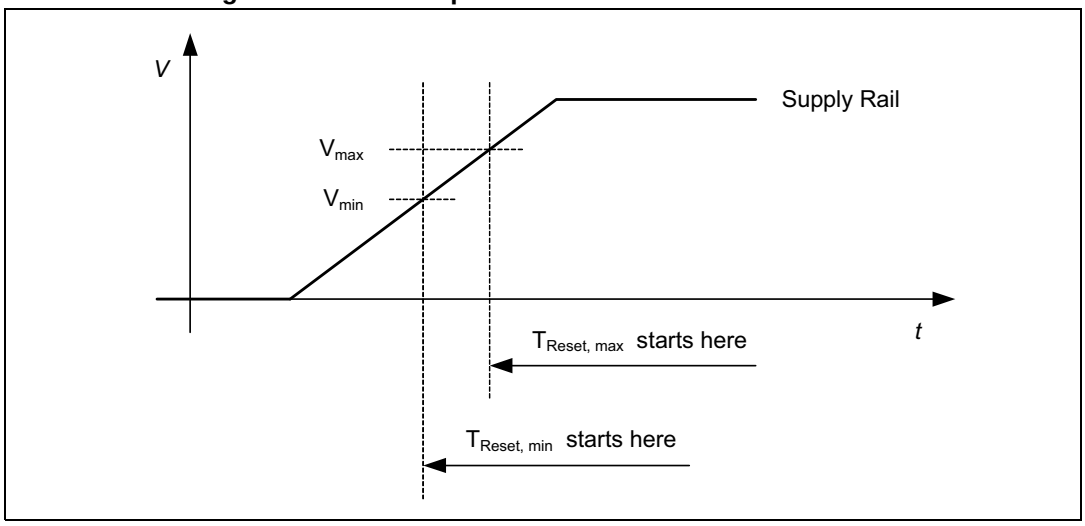


Table 35. Voltage Thresholds

Variable name	Value
V_{min}	Refer to *Table 20*
V_{max}	Refer to *Table 20*
Supply Rail	VDD_HV_PMU

3.20.4.2 External reset via $\overline{\text{RESET}}$

Figure 20 shows the voltage thresholds that determine the start of the reset sequences initiated by the assertion of $\overline{\text{RESET}}$ as specified in *Table 34*.

Figure 20. Reset sequence start via $\overline{\text{RESET}}$ assertion

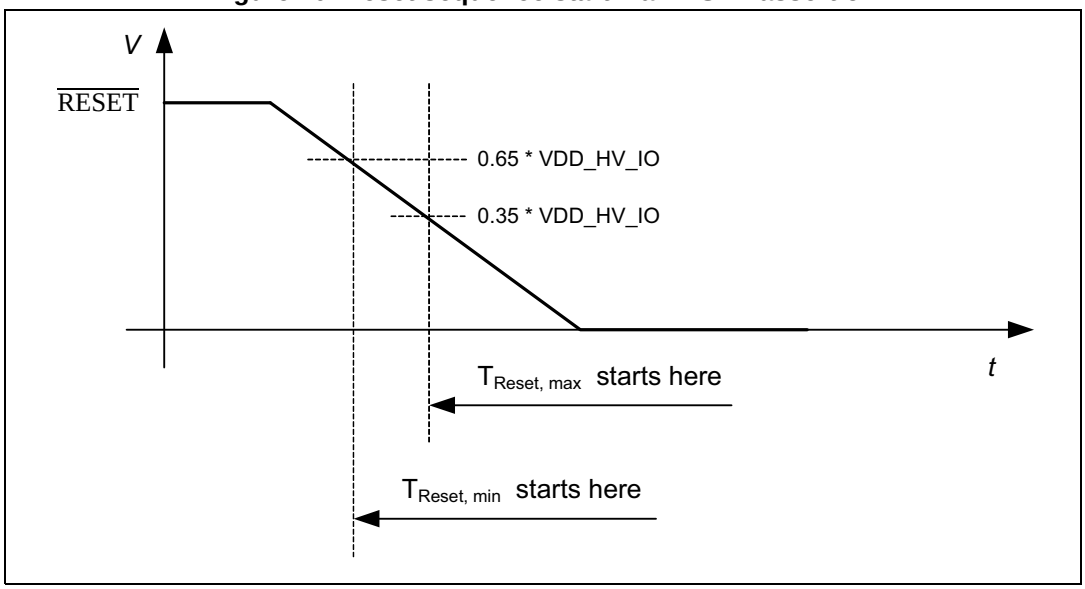


Figure 22. Start-up reset requirements

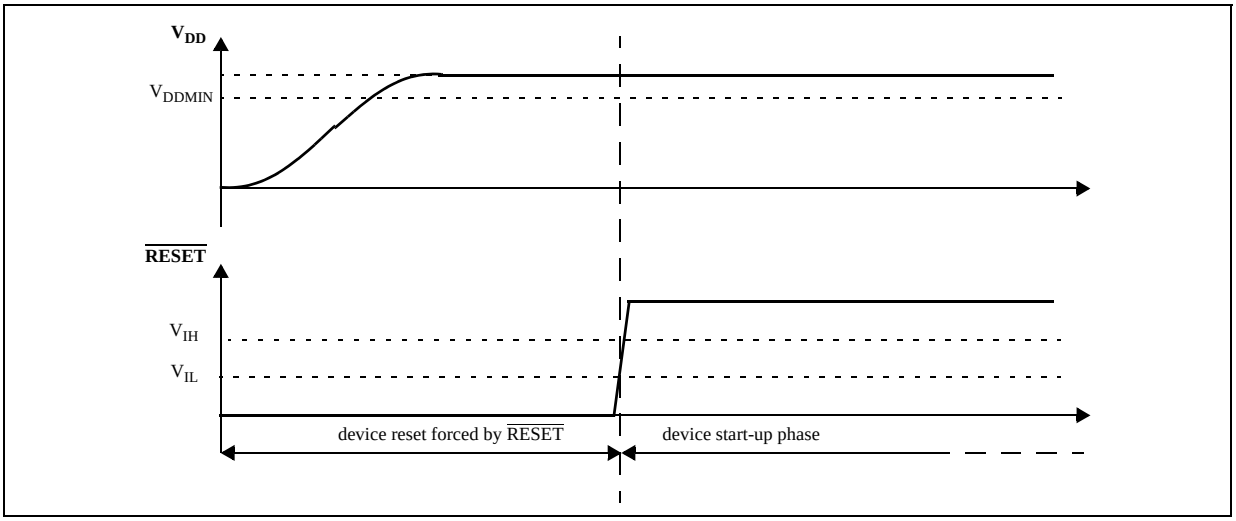


Figure 23. Noise filtering on reset signal

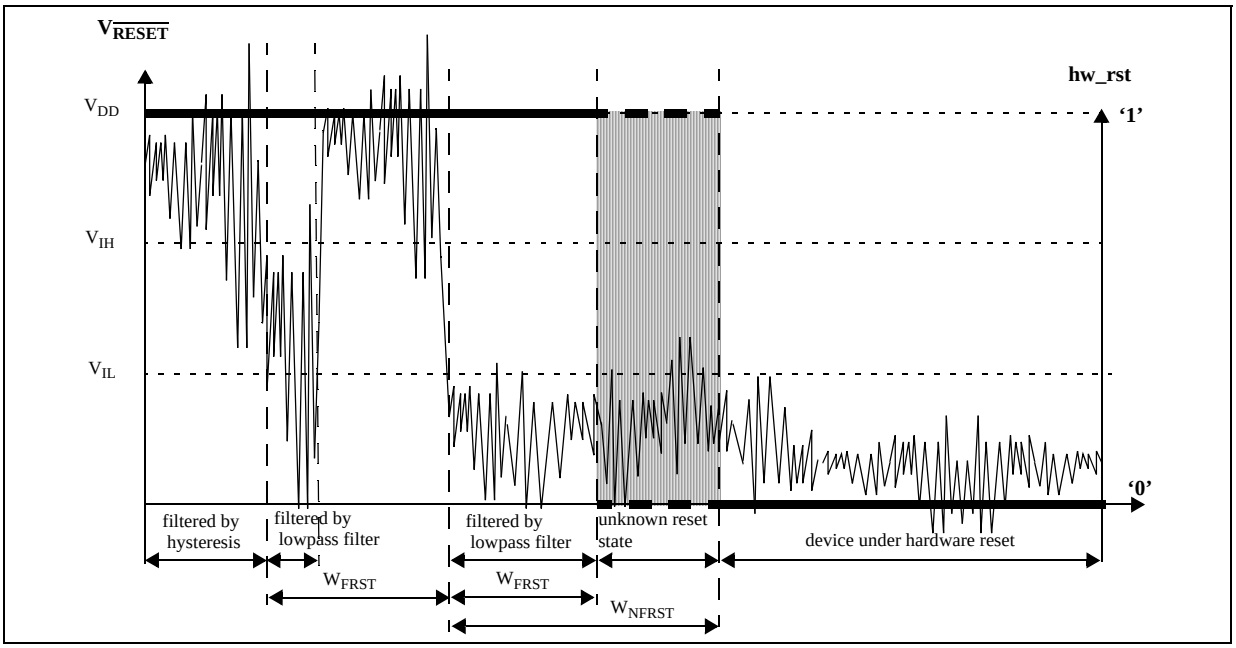
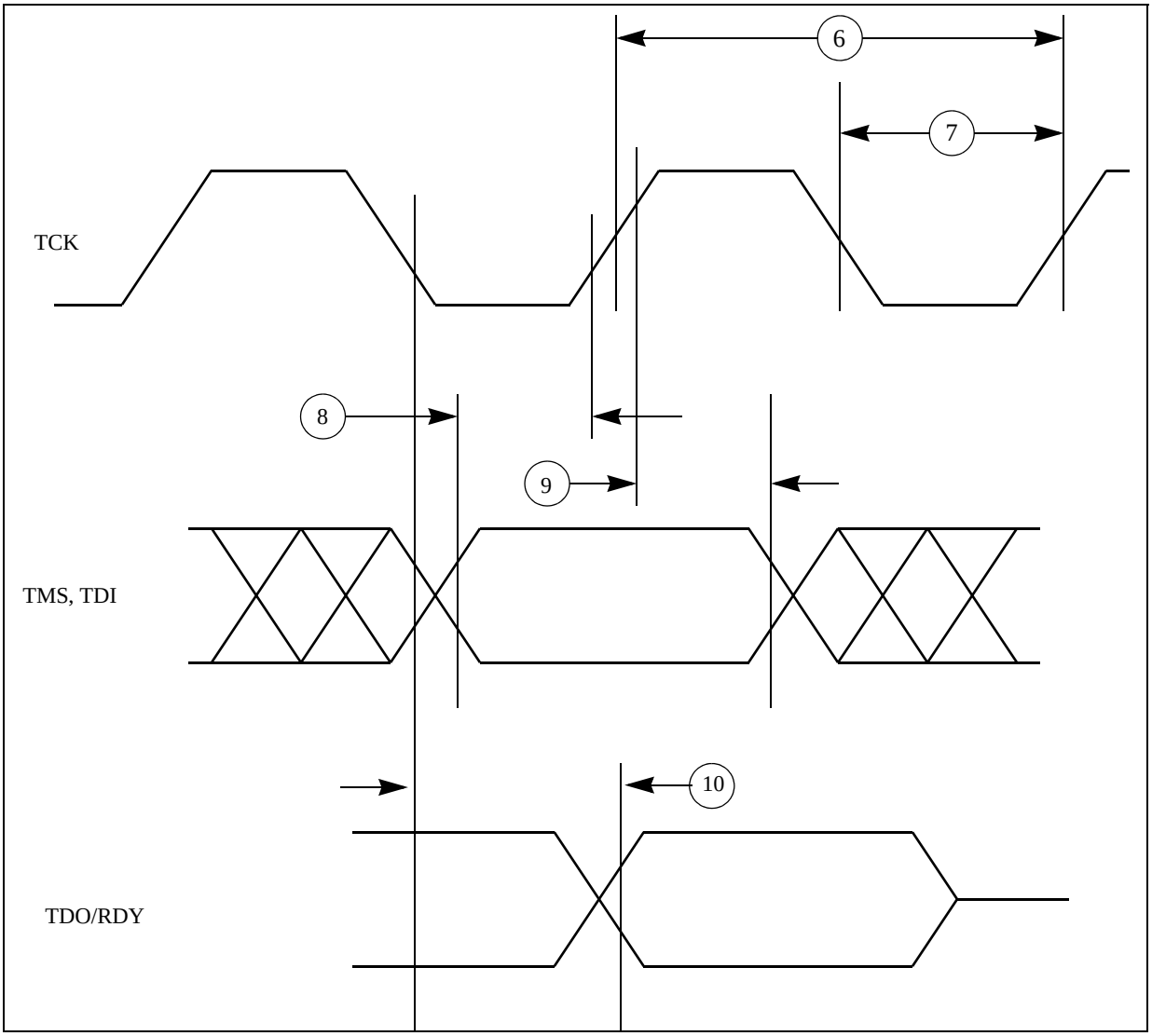


Table 36. RESET electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	nRESET input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	nRESET input not filtered pulse	—	500	—	—	ns

1. V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified.

Figure 30. Nexus TDI, TMS, TDO timing



3.21.5 External interrupt timing (IRQ pin)

Table 40. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time(1)	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Table 45. Document revision history

Date	Revision	Changes
18-Sep-2013	10	– Updated Disclaimer.
07-Feb-2014	11	– Removed “TBC” symbol in *Table 9* and *Table 22* – Resolved some cross references.
08-Jul-2015	12	Editorial and formatting changes throughout document. *Chapter 1: Introduction*: – In *Table 1: SPC56ELx/SPC564Lx device summary* added the column for SPC56EL54 device *Chapter 3: Electrical characteristics*: – In *Table 9: Absolute maximum ratings*, added condition “Valid only for ADC pins” for V_{IN} Symbol. – Added *Section 3.4: Decoupling capacitors*. – *Figure 10: Input Equivalent Circuit*: changed “V_{DD}” to “V_{REF}” in Internal circuit scheme – In *Table 32: Pad AC specifications (3.3 V, IPP_HVE = 0)* updated footnote 1 and footnote 2. – Updated *Figure 13: Pad output delay* Updated Disclaimer.