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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l3ccfsr

1.5 Feature details

1.5.1 High-performance e200z4d core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs

The following functions are implemented:

- ECC encoding (32-bit boundary for data and complete address bus)
- ECC decoding (32-bit boundary and entire address)
- Address translation from the AHB protocol on the XBAR to the SRAM array

The platform SRAM controller is replicated for each processor.

1.5.9 Memory subsystem access time

Every memory access, that the CPU performs, requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed is not parked on the requesting master in the crossbar.

Table 2 shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. Platform memory access time summary

AHB transfer	Data phase wait states	Description
e200z4d instruction fetch	0	Flash memory prefetch buffer hit (page hit)
e200z4d instruction fetch	3	Flash memory prefetch buffer miss (based on 4-cycle random flash array access time)
e200z4d data read	0–1	SRAM read
e200z4d data write	0	SRAM 32-bit write
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

1.5.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for SRAM

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO
- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
95	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
96	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
97	FCCU_F[1]	FCCU	F[1]	F[1]
98	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
99	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
100	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1. V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 4. LQFP144 pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
1	NMI	—		
2	A[6]	SIUL	GPIO[6]	GPIO[6]
		DSPI_1	SCK	SCK
		SIUL	—	EIRQ[6]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD\_HV\_IO}$	—		
127	$V_{SS\_HV\_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD\_HV\_REG\_2}$	—		
131	$V_{DD\_LV\_COR}$	—		
132	$V_{SS\_LV\_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD\_LV\_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS\_LV\_COR}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
L16	H[4]	SIUL	GPIO[116]	GPIO[116]
		FlexPWM_1	X[0]	X[0]
		eTimer_2	ETC[0]	ETC[0]
L17	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
M1	$V_{DD\_HV\_OSC}$	—		
M2	$V_{DD\_HV\_IO\_RING}$	—		
M3	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
M4	Not connected	—		
M6	V_{DD_LV}	—		
M7	V_{DD_LV}	—		
M8	V_{DD_LV}	—		
M9	V_{DD_LV}	—		
M10	V_{DD_LV}	—		
M11	V_{DD_LV}	—		
M12	V_{DD_LV}	—		
M14	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
M15	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
M16	TMS	—		
M17	H[5]	SIUL	GPIO[117]	GPIO[117]
		FlexPWM_1	A[0]	A[0]
		DSPI_0	CS4	—
N1	XTAL	—		
N2	$V_{SS\_HV\_IO\_RING}$	—		
N3	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
N4	$V_{SS\_LV\_PLL0\_PLL1}$	—		

Table 6. Supply pins (continued)

Supply		Pin #		
Symbol	**Description**	**100 pkg**	**144 pkg**	**257 pkg**
$V_{DD\_HV\_REG\_1}$	VDD_HV_REG_1	67	95	H15
$V_{SS\_HV\_FLA}$	VSS_HV_FLA	68	96	J16
$V_{DD\_HV\_FLA}$	VDD_HV_FLA	69	97	H16
$V_{DD\_HV\_IO}$	VDD_HV_IO	87	126	VDD_HV(3)
$V_{SS\_HV\_IO}$	VSS_HV_IO	88	127	VSS_HV(4)
$V_{DD\_HV\_REG\_2}$	VDD_HV_REG_2	91	130	C7
Power supply pins (1.2 V)				
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17	VSS_HV(2)
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18	VDD_LV(1)
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.	24	35	N4
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.	25	36	P4
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	28	39	VDD_LV(1)
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	29	40	VSS_LV(2)
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	—	70	VDD_LV(1)
$V_{SS\_LV\_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	—	71	VSS_LV(2)
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	65	93	VDD_LV(1)
$V_{SS\_LV\_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	66	94	VSS_LV(2)
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	92	131	VDD_LV(1)

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S	82	120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S	83	122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	—	M	S	95	136	C6
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1						
		SIUL	—	—	EIRQ[12]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
F[7]	PCR[87]	SIUL	GPIO[87]	ALT0	GPIO[87]	—	—	F	S	—	19	J1
		NPC	MCKO	ALT2	—	—						
F[8]	PCR[88]	SIUL	GPIO[88]	ALT0	GPIO[88]	—	—	F	S	—	20	K2
		NPC	MSEO[1]	ALT2	—	—						
F[9]	PCR[89]	SIUL	GPIO[89]	ALT0	GPIO[89]	—	—	F	S	—	23	K1
		NPC	MSEO[0]	ALT2	—	—						
F[10]	PCR[90]	SIUL	GPIO[90]	ALT0	GPIO[90]	—	—	F	S	—	24	L1
		NPC	EVTO	ALT2	—	—						
F[11]	PCR[91]	SIUL	GPIO[91]	ALT0	GPIO[91]	—	—	M	S	—	25	L2
		NPC	—	ALT2	EVTI	—						
F[12]	PCR[92]	SIUL	GPIO[92]	ALT0	GPIO[92]	—	—	M	S	—	106	C17
		eTimer_1	ETC[3]	ALT1	ETC[3]	PSMI[12]; PADSEL=2						
		SIUL	—	—	EIRQ[30]	—						
F[13]	PCR[93]	SIUL	GPIO[93]	ALT0	GPIO[93]	—	—	M	S	—	112	B14
		eTimer_1	ETC[4]	ALT1	ETC[4]	PSMI[13]; PADSEL=3						
		SIUL	—	—	EIRQ[31]	—						
F[14]	PCR[94]	SIUL	GPIO[94]	ALT0	GPIO[94]	—	—	M	S	—	115	C13
		LINFlexD_1	TXD	ALT1	—	—						
F[15]	PCR[95]	SIUL	GPIO[95]	ALT0	GPIO[95]	—	—	M	S	—	113	D13
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=2						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
H[4]	PCR[116]	SIUL	GPIO[116]	ALT0	GPIO[116]	—	—	M	S	—	—	L16
		FlexPWM_1	X[0]	ALT1	X[0]	—						
		eTimer_2	ETC[0]	ALT2	ETC[0]	PSMI[39]; PADSEL=0						
H[5]	PCR[117]	SIUL	GPIO[117]	ALT0	GPIO[117]	—	—	M	S	—	—	M17
		FlexPWM_1	A[0]	ALT1	A[0]	—						
		DSPI_0	CS4	ALT3	—	—						
H[6]	PCR[118]	SIUL	GPIO[118]	ALT0	GPIO[118]	—	—	M	S	—	—	H17
		FlexPWM_1	B[0]	ALT1	B[0]	—						
		DSPI_0	CS5	ALT3	—	—						
H[7]	PCR[119]	SIUL	GPIO[119]	ALT0	GPIO[119]	—	—	M	S	—	—	K16
		FlexPWM_1	X[1]	ALT1	X[1]	—						
		eTimer_2	ETC[1]	ALT2	ETC[1]	PSMI[40]; PADSEL=0						
H[8]	PCR[120]	SIUL	GPIO[120]	ALT0	GPIO[120]	—	—	M	S	—	—	K15
		FlexPWM_1	A[1]	ALT1	A[1]	—						
		DSPI_0	CS6	ALT3	—	—						
H[9]	PCR[121]	SIUL	GPIO[121]	ALT0	GPIO[121]	—	—	M	S	—	—	G16
		FlexPWM_1	B[1]	ALT1	B[1]	—						
		DSPI_0	CS7	ALT3	—	—						
H[10]	PCR[122]	SIUL	GPIO[122]	ALT0	GPIO[122]	—	—	M	S	—	—	A11
		FlexPWM_1	X[2]	ALT1	X[2]	—						
		eTimer_2	ETC[2]	ALT2	ETC[2]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	—	M	S	—	—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	—	M	S	—	—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	—	M	S	—	—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	—	F	S	—	—	K3
		NPC	RDY	ALT2	—	—						

1. Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)
2. The default function of this pin out of reset is ALT1 (TDO).
3. Analog

Note: Open Drain can be configured by the PCRn for all pins used as output (except FCCU_F[0] and FCCU_F[1]).

EME testing was performed and documented according to these standards: [IEC 61967-2 & -4]

EMS testing was performed and documented according to these standards: [IEC 62132-2 & -4]

Refer SPC56EL60 for detailed information pertaining to the EMC, EME, and EMS testing and results.

3.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (*n* + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Figure 8. Main oscillator electrical characteristics

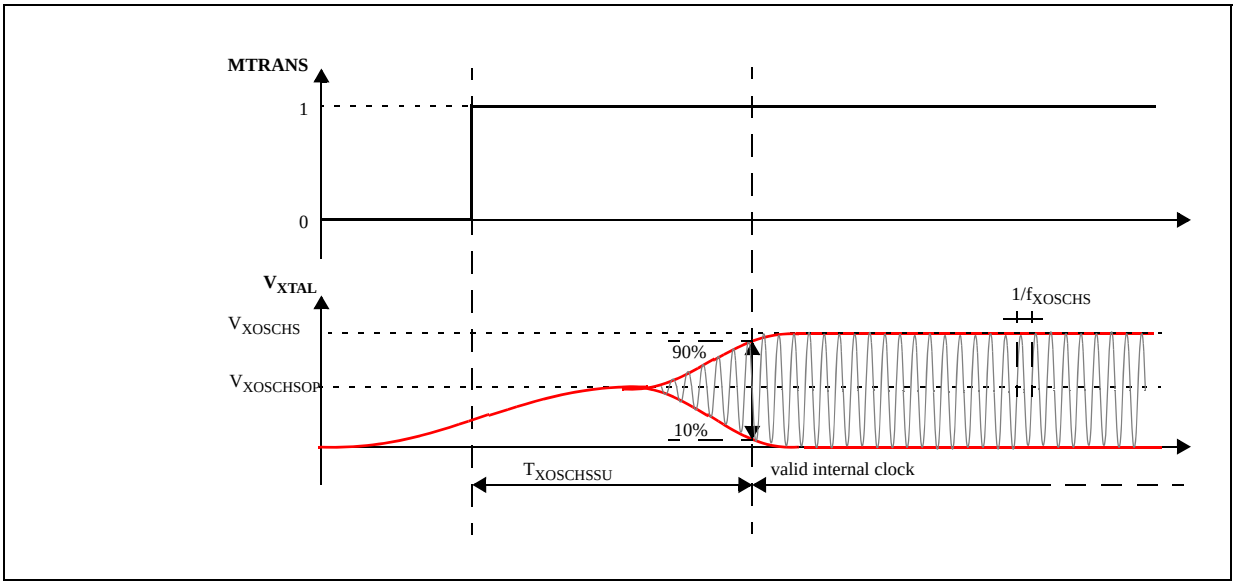


Table 24. Main oscillator electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
$g_{mXOSCHS}$	P	Oscillator transconductance	V_{DD} = 3.3 V ±10%	4.5	—	13.25	mA/V
V_{XOSCHS}	D	Oscillation amplitude	f_{OSC} = 4, 8, 10, 12, 16 MHz	1.3	—	—	V
			f_{OSC} = 40 MHz	1.1	—	—	
$V_{XOSCHSOP}$	D	Oscillation operating point	—	—	0.82	—	V
$T_{XOSCHSSU}$	T	Oscillator start-up time	f_{OSC} = 4, 8, 10, 12 MHz[2]	—	—	6	ms
			f_{OSC} = 16, 40 MHz[2]	—	—	2	
V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

1. V_{DD} = 3.3 V ±10%, T_J = –40 to +150 °C, unless otherwise specified.
2. The recommended configuration for maximizing the oscillator margin are:
   XOSC_MARGIN = 0 for 4 MHz quartz
   XOSC_MARGIN = 1 for 8/16/40 MHz quartz

Table 27. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
IS1WWINJ			(double ADC channel)				
	C	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	Vref = 3.3V	67	—	—	dB
SNR	T	Signal-to-noise ratio	Vref = 5.0V	69	—	—	dB
THD	T	Total harmonic distortion	—	-65	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$	T	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
			With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$	P	Total unadjusted error for IS1WWINJ (double ADC channels)	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1. T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.
4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time Tsample, but only the time for determining the digital result.
6. See *Figure 10*.
7. For the 144-pin package
8. No missing codes

3.17 Flash memory electrical characteristics

Table 28. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Typ (1)	Initial Max (2)	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	*[4]	Double word (64 bits) program time[4]	30	—	500	µs
2	$T_{PPROGRAM}$	*[4]	Page(128 bits) program time[4]	40	160	500	µs
3	$T_{16KPPERASE}$	*[4]	16 KB block pre-program and erase time	250	1000	5000	ms
4	$T_{48KPPERASE}$	*[4]	48 KB block pre-program and erase time	400	1500	5000	ms
5	$T_{64KPPERASE}$	*[4]	64 KB block pre-program and erase time	450	1800	5000	ms
6	$T_{128KPPERASE}$	*[4]	128 KB block pre-program and erase time	800	2600	7500	ms
7	$T_{256KPPERASE}$	*[4]	256 KB block pre-program and erase time	1400	5200	15000	ms

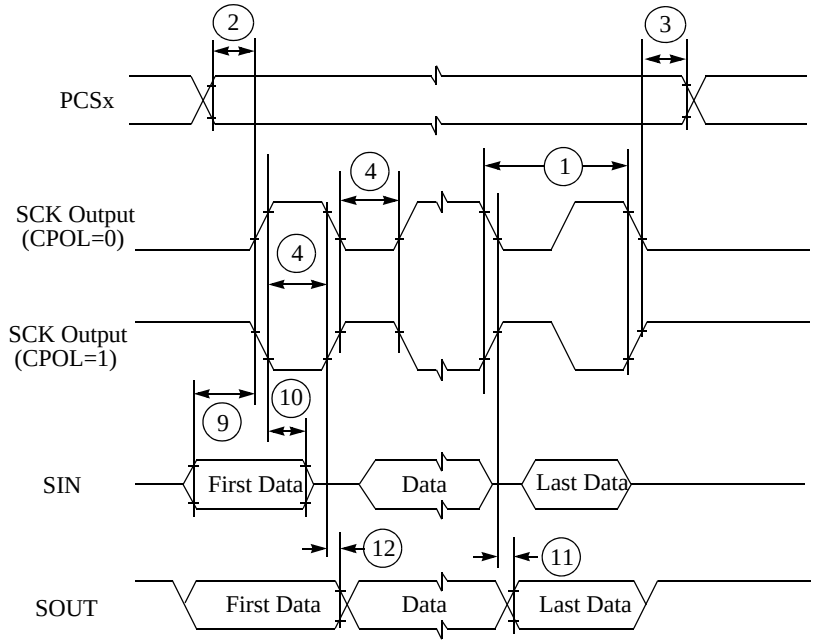
1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25°C. These values are characterized, but not tested.

Table 41. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	

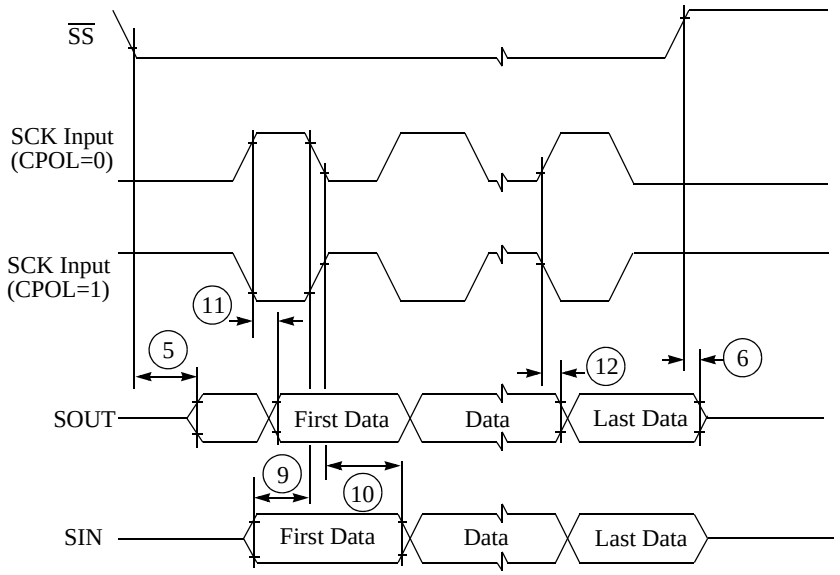
1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

Figure 32. DSPI classic SPI timing — master, CPHA = 0



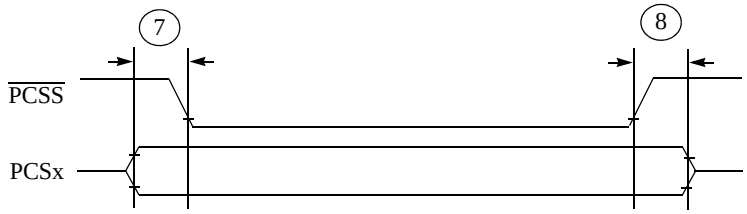
Note: The numbers shown are referenced in *Table 41*.

Figure 39. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 40. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing



Note: The numbers shown are referenced in *Table 41*.

Figure 42. LQFP144 package mechanical drawing

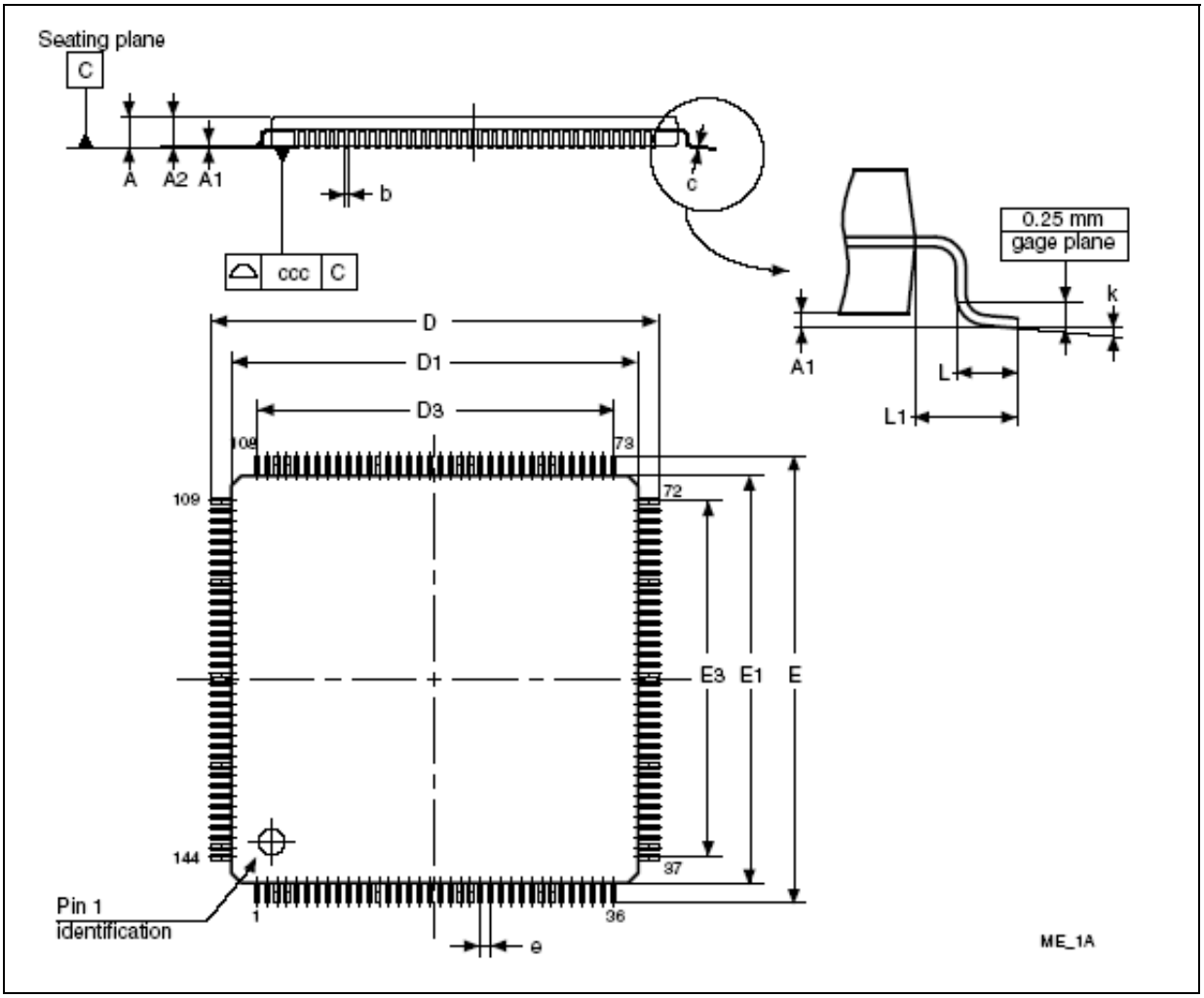


Table 43. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.0630
A1		0.05	0.15		0.0020	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	22	21.8	22.2	0.8661	0.8583	0.8740
D1	20	19.8	20.2	0.7874	0.7795	0.7953
D3	17.5			0.6890		
E	22	21.8	22.2	0.8661	0.8583	0.8740
E1	20	19.8	20.2	0.7874	0.7795	0.7953

Table 44. LFBGA257 mechanical data

TITLE: LFBGA 14x14x1.7 257 F17x17 PITCH 0.8 BALL 0.4

PACKAGE CODE:

JEDEC/EIAJ REFERENCE NUMBER: JEDEC STANDARD NO.95 SECTION 4.5 (Fine pitch, Square Ball Grid Array Package Design Guide)

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.70			1.45	(1)
A1	0.21			0.25	0.30	0.35	
A2		1.085		1.03	1.085	1.14	
A3		0.30		0.26	0.30	0.34	
A4			0.80	0.77	0.785	0.80	
b	0.35	0.40	0.45	0.35	0.40	0.45	(2)
D	13.85	14.00	14.15	13.85	14.00	14.15	
D1		12.80			12.80		
E	13.85	14.00	14.15	13.85	14.00	14.15	
E1		12.80			12.80		
e		0.80			0.80		
F		0.6			0.6		
ddd			0.12			0.12	
eee			0.15			0.15	(3)
fff			0.08			0.08	(4)

NOTES:

(1) - LFBGA stands for **L**ow profile **F**ine Pitch **B**all **G**rid **A**rray.
- Low Profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
- The maximum total package height is calculated by the following methodology:
A2 Typ+A1 Typ +√ ($A1^2+A3^2+A4^2$ tolerance values)

- Low profile: 1.20mm < A ≤ 1.70mm / Fine pitch: e < 1.00mm pitch.

(2) – The typical ball diameter before mounting is 0.40mm.

(3) - The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

(4) - The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

(5) - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 45. Document revision history

Date	Revision	Changes
18-Sep-2013	10	– Updated Disclaimer.
07-Feb-2014	11	– Removed “TBC” symbol in *Table 9* and *Table 22* – Resolved some cross references.
08-Jul-2015	12	Editorial and formatting changes throughout document. *Chapter 1: Introduction*: – In *Table 1: SPC56ELx/SPC564Lx device summary* added the column for SPC56EL54 device *Chapter 3: Electrical characteristics*: – In *Table 9: Absolute maximum ratings*, added condition “Valid only for ADC pins” for V_{IN} Symbol. – Added *Section 3.4: Decoupling capacitors*. – *Figure 10: Input Equivalent Circuit*: changed “V_{DD}” to “V_{REF}” in Internal circuit scheme – In *Table 32: Pad AC specifications (3.3 V, IPP_HVE = 0)* updated footnote 1 and footnote 2. – Updated *Figure 13: Pad output delay* Updated Disclaimer.