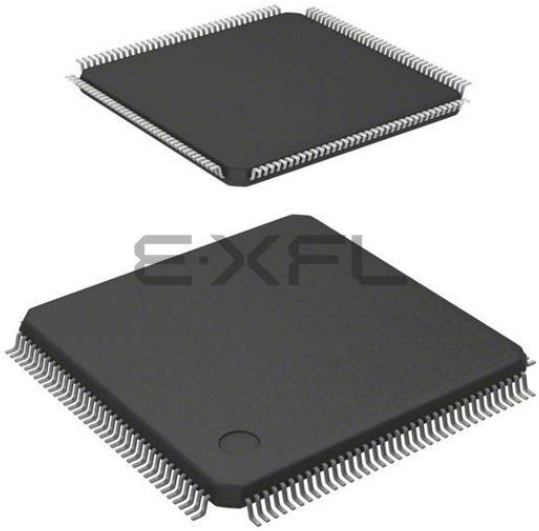

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l5bbfqy

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow block for test, censorship device and user option bits
- Wait states:
  - 3 wait states for frequencies =< 120 MHz
  - 2 wait states for frequencies =< 80 MHz
  - 1 wait state for frequencies =< 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The SPC56ELx/SPC564Lx SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

1.5.28 Serial communication interface module (LINFlexD)

The LINFlexD module (LINFlex with DMA support) on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 50-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, 16-bit, or 17-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (Parity, Noise and Framing errors)
  - Interrupt driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods
- Support for DMA enabled transfers

1.5.29 Deserial Serial Peripheral Interface (DSPI)

The DSPI modules provide a synchronous serial interface for communication between the SPC56ELx/SPC564Lx and external devices.

A DSPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase

1.5.37 Junction temperature sensor

The junction temperature sensor provides a value via an ADC channel that can be used by software to calculate the device junction temperature.

The key parameters of the junction temperature sensor include:

- Nominal temperature range from –40 to 150 °C
- Software temperature alarm via analog ADC comparator possible

1.5.38 Nexus Port Controller (NPC)

The NPC module provides real-time development support capabilities for this device in compliance with the IEEE-ISTO 5001-2003. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

The NPC block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2003 Class 3+, including selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the Power Architecture internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Full and reduced port modes
- MCKO (message clock out) pin
- 4 or 12 MDO (message data out) pins[b]
- 2 $\overline{\text{MSEO}}$ (message start/end out) pins
- $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
- $\overline{\text{EVTI}}$ (event in) pin
- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Supports JTAG mode
- Host processor (e200) development support features
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches,

b. 4 MDO pins on LQFP144 package, 12 MDO pins on LFBGA257 package.

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
144	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1. V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 5. LFBGA257 pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
A1	$V_{SS\_HV\_IO\_RING}$	—		
A2	$V_{SS\_HV\_IO\_RING}$	—		
A3	$V_{DD\_HV\_IO\_RING}$	—		
A4	H[2]	SIUL	GPIO[114]	GPIO[114]
		NPC	MDO[5]	—

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
B11	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]
B12	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
B13	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
B14	F[13]	SIUL	GPIO[93]	GPIO[93]
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[31]
B15	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
B16	$V_{DD\_HV\_IO\_RING}$	—		
B17	$V_{SS\_HV\_IO\_RING}$	—		
C1	$V_{DD\_HV\_IO\_RING}$	—		
C2	Not connected	—		
C3	$V_{SS\_HV\_IO\_RING}$	—		
C4	FCCU_F[1]	FCCU	F[1]	F[1]
C5	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
C6	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
C7	$V_{DD\_HV\_REG\_2}$	—		
C8	$V_{DD\_HV\_REG\_2}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
G14	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
G15	H[13]	SIUL	GPIO[125]	GPIO[125]
		FlexPWM_1	X[3]	X[3]
		eTimer_2	ETC[3]	ETC[3]
G16	H[9]	SIUL	GPIO[121]	GPIO[121]
		FlexPWM_1	B[1]	B[1]
		DSPI_0	CS7	—
G17	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
H1	G[13]	SIUL	GPIO[109]	GPIO[109]
		NPC	MDO[10]	—
H2	$V_{SS\_HV\_IO\_RING}$	—		
H3	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
H4	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
H6	V_{DD_LV}	—		
H7	V_{SS_LV}	—		
H8	V_{SS_LV}	—		
H9	V_{SS_LV}	—		
H10	V_{SS_LV}	—		
H11	V_{SS_LV}	—		
H12	V_{DD_LV}	—		
H14	V_{SS_LV}	—		
H15	$V_{DD\_HV\_REG\_1}$	—		
H16	$V_{DD\_HV\_FLA}$	—		

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[14]	PCR[14]	SIUL	GPIO[14]	ALT0	GPIO[14]	—	—	M	S	99	143	B4
		FlexCAN_1	TXD	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=0						
		SIUL	—	—	EIRQ[13]	—						
A[15]	PCR[15]	SIUL	GPIO[15]	ALT0	GPIO[15]	—	—	M	S	100	144	D3
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=0						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=0						
		SIUL	—	—	EIRQ[14]	—						
Port B												
B[0]	PCR[16]	SIUL	GPIO[16]	ALT0	GPIO[16]	—	—	M	S	76	109	B15
		FlexCAN_0	TXD	ALT1	—	—						
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=0						
		SSCM	DEBUG[0]	ALT3	—	—						
		SIUL	—	—	EIRQ[15]	—						

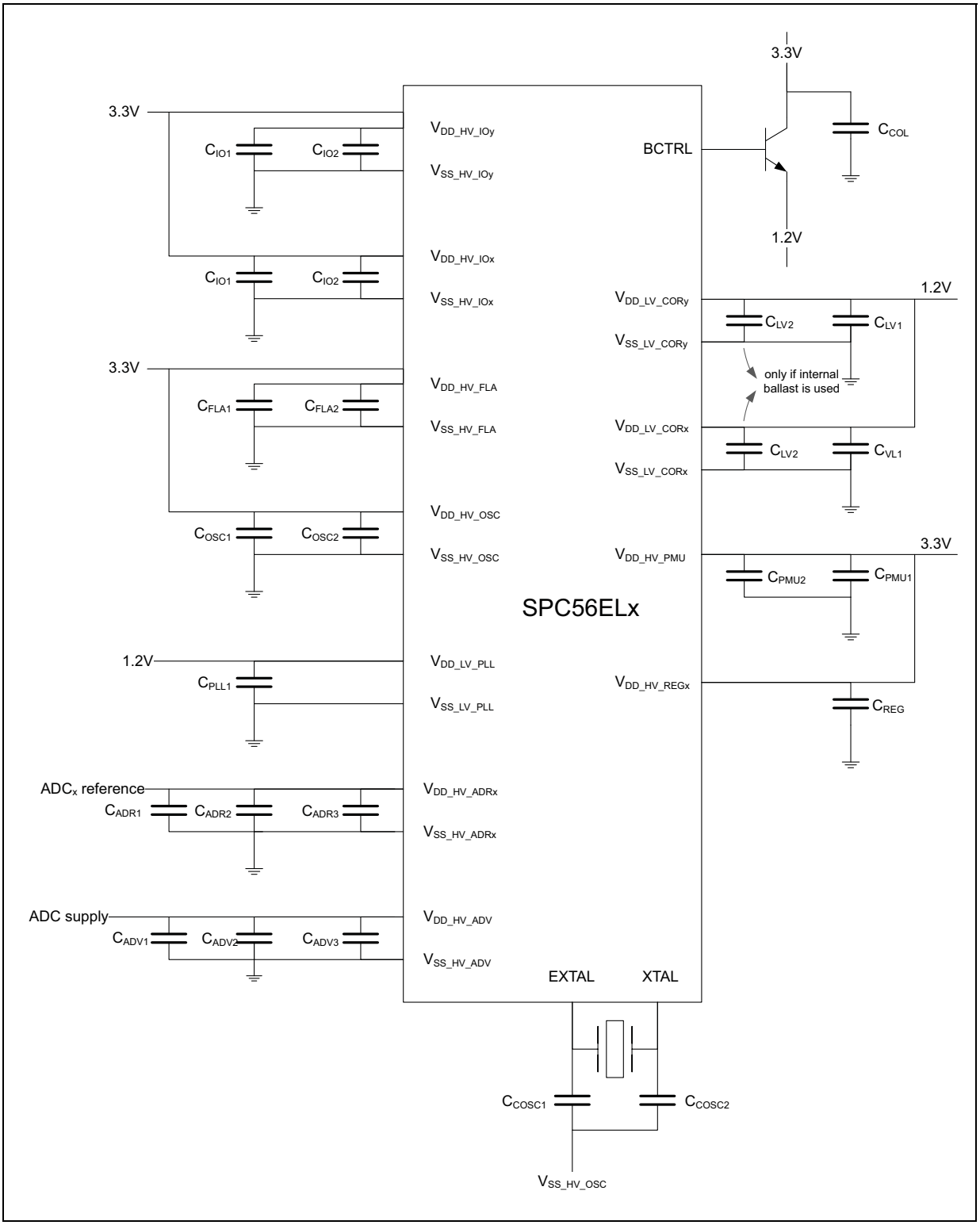
Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[6]	PCR[54]	SIUL	GPIO[54]	ALT0	GPIO[54]	—	—	M	S	23	34	P3
		DSPI_0	CS2	ALT1	—	—						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=1						
D[7]	PCR[55]	SIUL	GPIO[55]	ALT0	GPIO[55]	—	—	M	S	26	37	R4
		DSPI_1	CS3	ALT1	—	—						
		DSPI_0	CS4	ALT3	—	—						
		SWG	analog output	—	—	—						
D[8]	PCR[56]	SIUL	GPIO[56]	ALT0	GPIO[56]	—	—	M	S	21	32	M3
		DSPI_1	CS2	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=2						
		DSPI_0	CS5	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=1						
D[9]	PCR[57]	SIUL	GPIO[57]	ALT0	GPIO[57]	—	—	M	S	15	26	L3
		FlexPWM_0	X[0]	ALT1	X[0]	—						
		LINFlexD_1	TXD	ALT2	—	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[10]	PCR[58]	SIUL	GPIO[58]	ALT0	GPIO[58]	—	—	M	S	53	76	T15
		FlexPWM_0	A[0]	ALT1	A[0]	PSMI[20]; PADSEL=1						
		eTimer_0	—	—	ETC[0]	PSMI[35]; PADSEL=1						
D[11]	PCR[59]	SIUL	GPIO[59]	ALT0	GPIO[59]	—	—	M	S	54	78	R16
		FlexPWM_0	B[0]	ALT1	B[0]	PSMI[24]; PADSEL=1						
		eTimer_0	—	—	ETC[1]	PSMI[36]; PADSEL=1						
D[12]	PCR[60]	SIUL	GPIO[60]	ALT0	GPIO[60]		—	M	S	70	99	G14
		FlexPWM_0	X[1]	ALT1	X[1]	PSMI[28]; PADSEL=1						
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=1						
D[14]	PCR[62]	SIUL	GPIO[62]	ALT0	GPIO[62]	—	—	M	S	73	105	D16
		FlexPWM_0	B[1]	ALT1	B[1]	PSMI[25]; PADSEL=2						
		eTimer_0	—	—	ETC[3]	PSMI[38]; PADSEL=1						
Port E												
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—	46	68	T13
		ADC_1	—	—	AN[5](3)	—						
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—	32	49	U6
		ADC_0	—	—	AN[5](3)	—						

Figure 5. Decoupling capacitors



2. Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for <100 program/erase cycles, nominal supply values and operation at 25°C. These values are verified at production test.
3. Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.
4. Program times are actual hardware programming times and do not include software overhead.

Table 29. Flash memory timing

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
T_{RES}	D	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns
T_{DONE}	D	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared	—	—	5	ns
T_{PSRT}	D	Time between program suspend resume and the next program suspend request.(1)	100	—	—	µs
T_{ESRT}	D	Time between erase suspend resume and the next erase suspend request.(2)	10			ms

1. Repeated suspends at a high frequency may result in the operation timing out, and the flash module will respond by completing the operation with a fail code (MCR[PEG] = 0), or the operation not able to finish (MCR[DONE] = 1 during Program operation). The minimum time between suspends to ensure this does not occur is T_{PSRT}.
2. If Erase suspend rate is less than T_{ESRT}, an increase of slope voltage ramp occurs during erase pulse. This improves erase time but reduces cycling figure due to overstress.

Table 30. Flash memory module life

No.	Symbol		Parameter	Value			Unit
				Minimum	Typical	Maximum	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range(1)	100000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range(1)	1000	100000 (2)	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature(3) Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

1. Operating temperature range is T_J from –40 °C to 150 °C. Typical endurance is evaluated at 25 °C.
2. Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks.
3. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 34. Reset sequence trigger — reset sequence (continued)

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive Reset Sequence, BIST enabled(1)	***Destructive Reset Sequence, BIST disabled***(1)	***External Reset Sequence Long, BIST enabled***	***Functional Reset Sequence Long***	***Functional Reset Sequence Short***
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$(7)	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1. Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.
2. End of the internal reset sequence (as specified in *Table 33*) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till $\overline{\text{RESET}}$ is released externally.
3. The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).
4. If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is enabled via chip configuration data stored in the shadow sector of the NVM.
5. If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is disabled via chip configuration data stored in the shadow sector of the NVM.
6. If $\overline{\text{RESET}}$ is configured for short reset
7. Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.20.4 Reset sequence — start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence becomes important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.20.4.1 Destructive reset

Figure 19 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*.

Figure 22. Start-up reset requirements

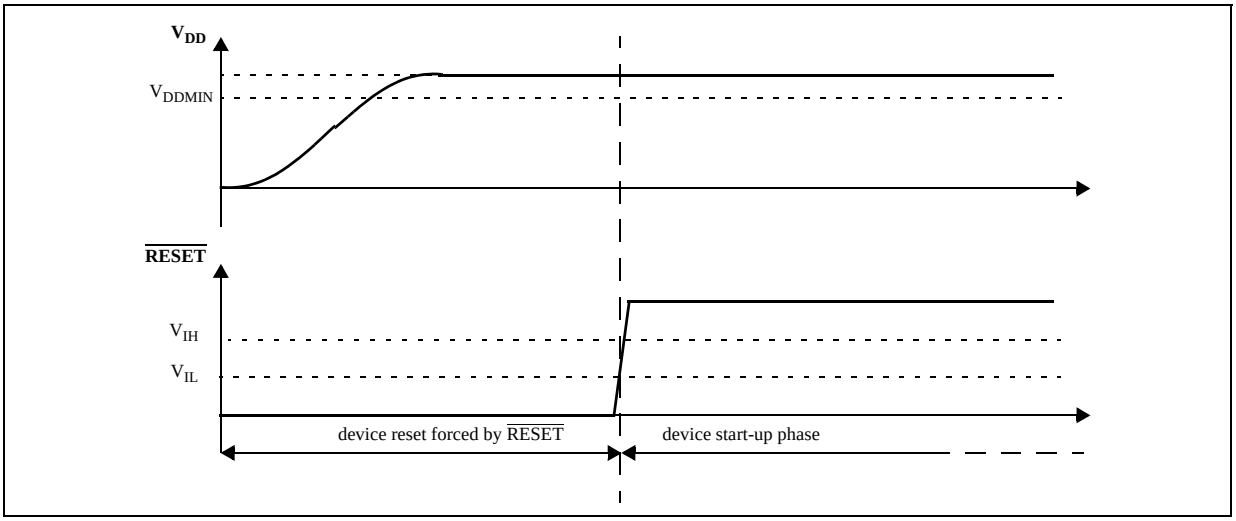


Figure 23. Noise filtering on reset signal

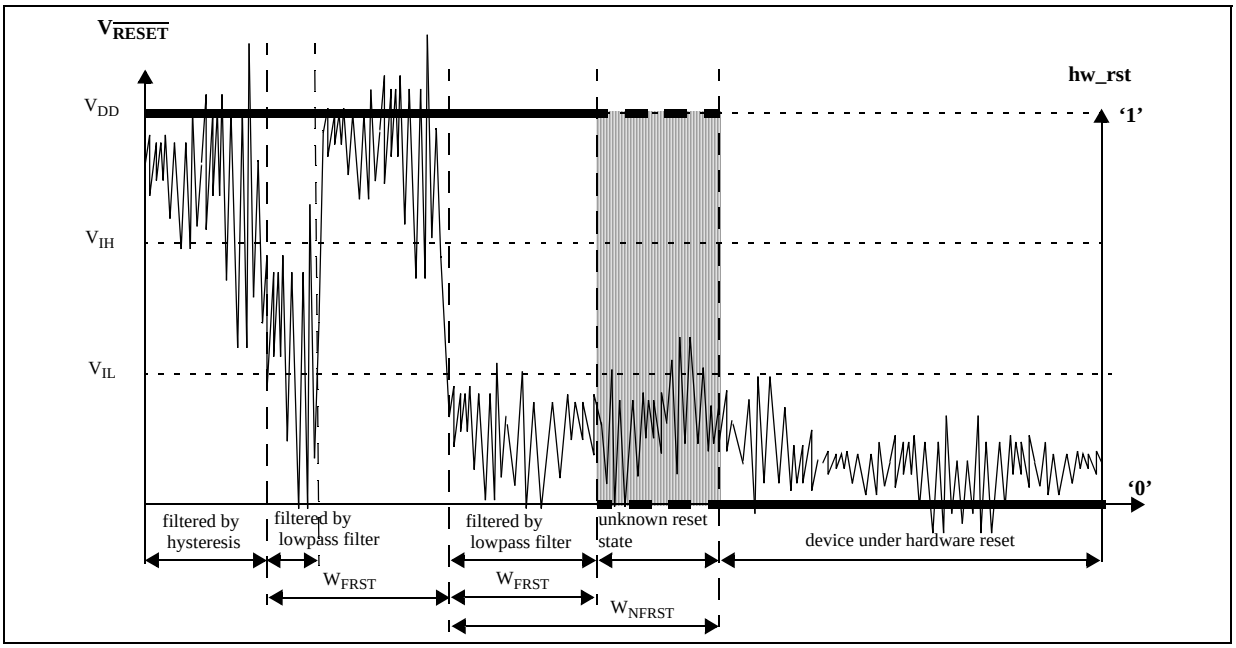


Table 36. RESET electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	nRESET input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	nRESET input not filtered pulse	—	500	—	—	ns

1. V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified.

2. C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.21.2 WKUP/NMI timing

Table 37. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	45	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	205	—	—	ns

3.21.3 IEEE 1149.1 JTAG interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	62.5	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Table 39. Nexus debug port timing(1) (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	D	TDI, TMS Data Hold Time		5	—	ns
10	t_{JOV}	D	TCK Low to TDO/RDY Data Valid		0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

Figure 27. Nexus output timing

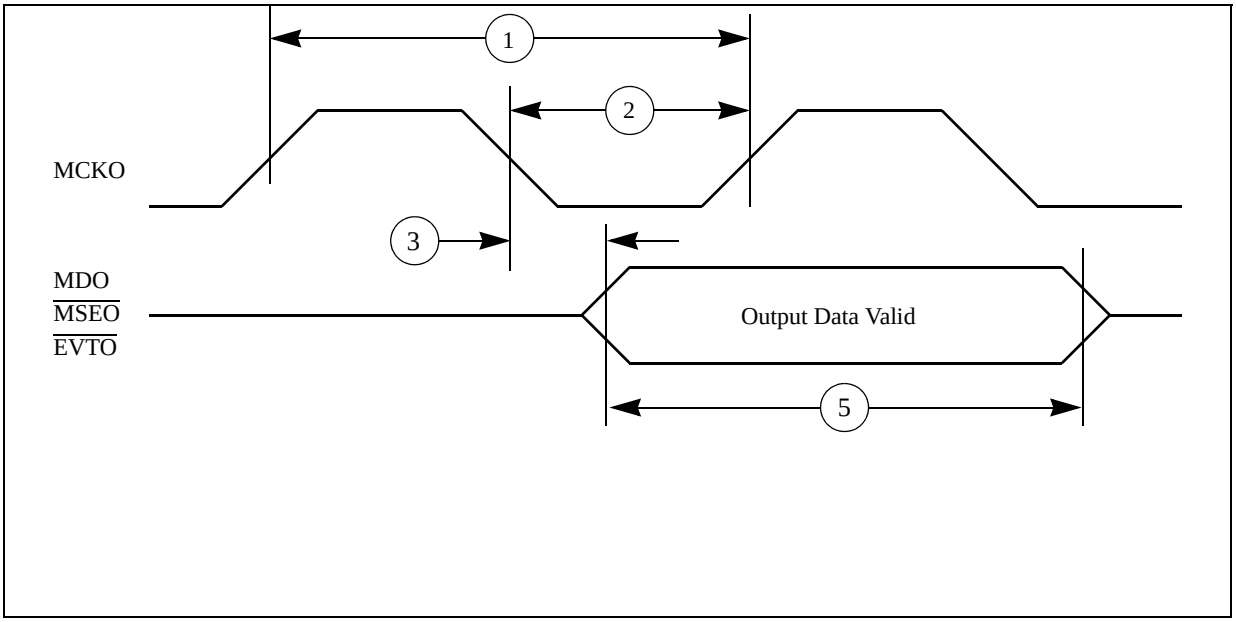


Figure 28. Nexus EVTI Input Pulse Width

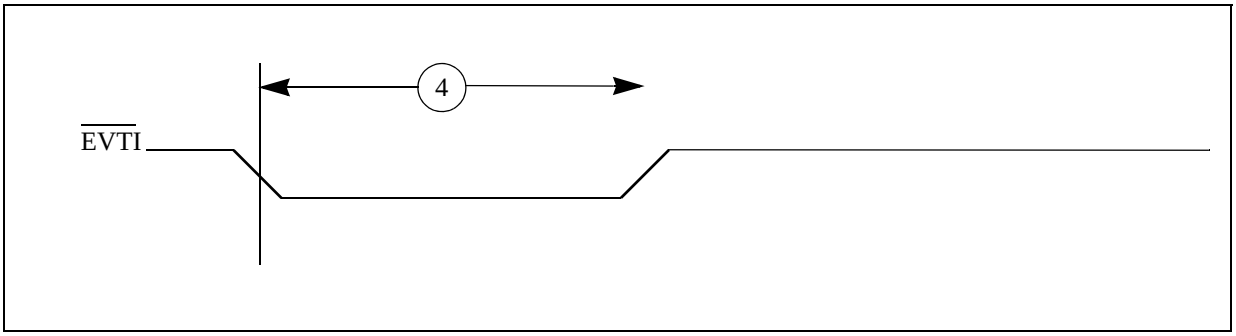
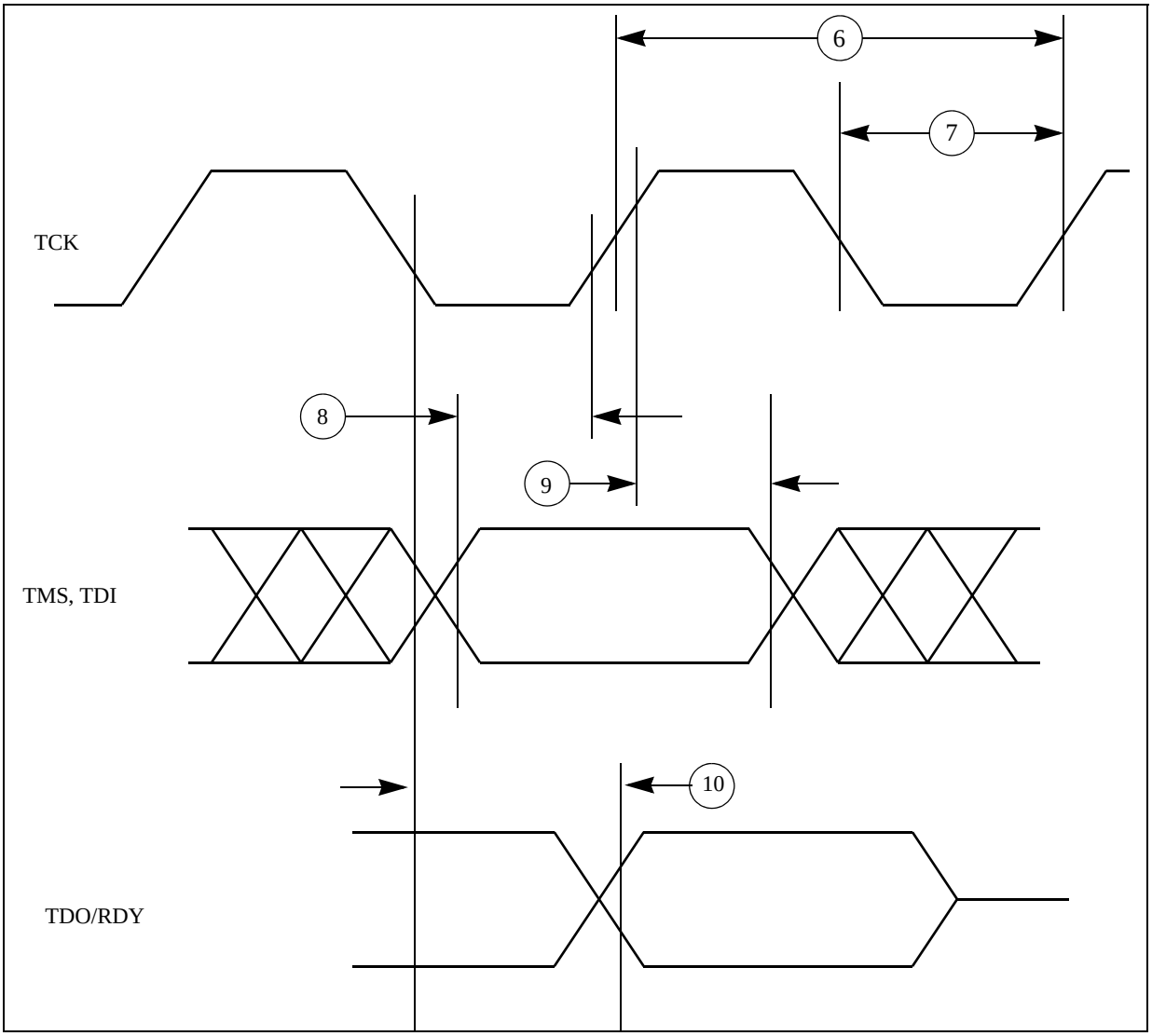


Figure 30. Nexus TDI, TMS, TDO timing



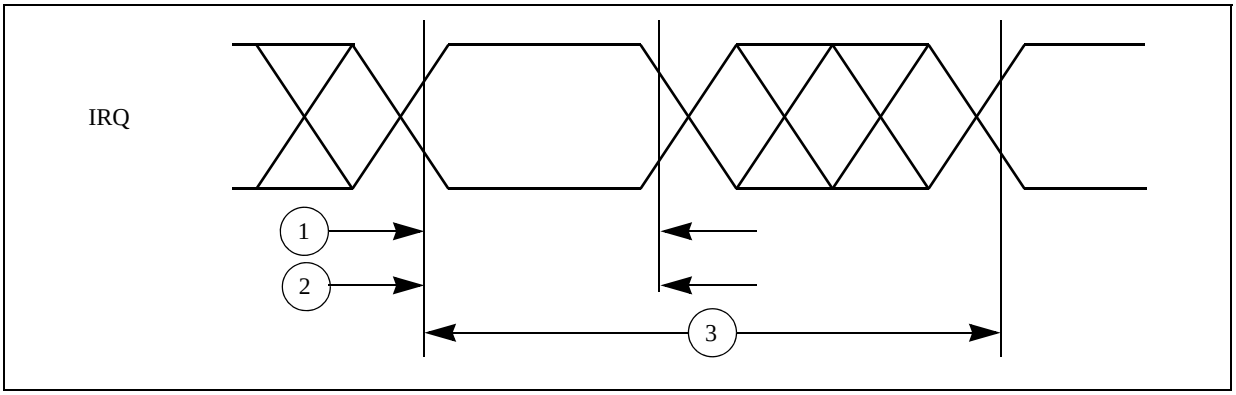
3.21.5 External interrupt timing (IRQ pin)

Table 40. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time(1)	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Figure 31. External interrupt timing



3.21.6 DSPI timing

Table 41. DSPI timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		D		Slave (MTFE = 0)	62	—	
		D		Slave Receive Only Mode(1)	16	—	
2	t_{CSC}	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	D	After SCK delay	—	16	—	ns
4	t_{SDC}	D	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	ns
5	t_A	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	12	
				Master (MTFE = 1, CPHA = 1)	—	4	

Figure 42. LQFP144 package mechanical drawing

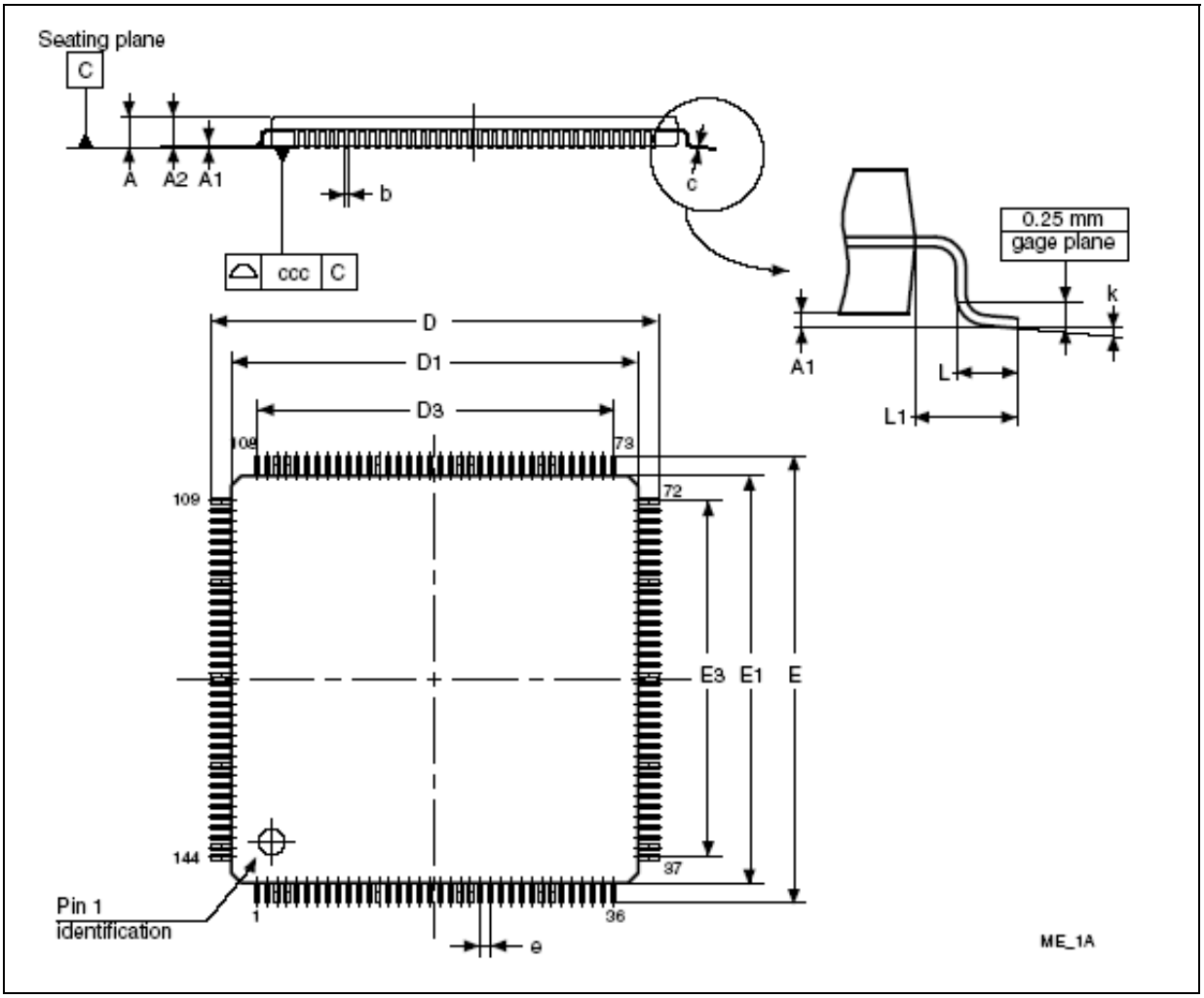


Table 43. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.0630
A1		0.05	0.15		0.0020	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	22	21.8	22.2	0.8661	0.8583	0.8740
D1	20	19.8	20.2	0.7874	0.7795	0.7953
D3	17.5			0.6890		
E	22	21.8	22.2	0.8661	0.8583	0.8740
E1	20	19.8	20.2	0.7874	0.7795	0.7953

Table 45. Document revision history

Date	Revision	Changes
23-Mar-2011	6 (continued)	In the “Supply current characteristics (cut2)“ table: – Changed “$I_{DD\_LV\_MAX}$” to “$I_{DD\_LV\_MAX}$“; – Removed all “40-120 MHz” frequency ranges from the “Conditions” column; – Updated the “Max” values column; – Added parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ with “P” classification and special footnote; – Changed all “25°C“ temperature conditions to “ambient”; – Added “T_J = 150 °C“ condition to parameters $I_{DD\_HV\_ADC}$, $I_{DD\_HV\_AREF}$, $I_{DD\_HV\_OSC}$, and $I_{DD\_HV\_FLASH}$. Changed the timing diagram in the “Main oscillator electrical characteristics” section to reference MTRANS assertion instead of V_{DDMIN}. Updated the jitter specs in the “FMPLL electrical characteristics“ table. In the “ADC conversion characteristics“ table, changed all parameters with units of “counts” to units of “LSB” and updated Min/Max values. Changed $I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$ operating current (for both cases) to TBD. In the “Supply current characteristics (cut2)” section, added a footnote that $I_{DD\_HV\_ADC}$ and $I_{DD\_HV\_AREF}$ represent the total current of both ADCs in the “Current consumption characteristics” table. In the “ADC conversion characteristics” table: – Changed DNL min from -2 to -1. – Changed OFS min from -2 to -6. – Changed OFS max from 2 to 6. – Changed GNE min from -2 to -6. – Changed GNE max from 2 to 6. – Changed SNR min from 69 to 67. – Changed TUE min (without current injection) from -6 to -8. – Changed TUE max (without current injection) from 6 to 8. – Changed TUE min (with current injection) from -8 to -10. Changed TUE max (with current injection) from 8 to 10.