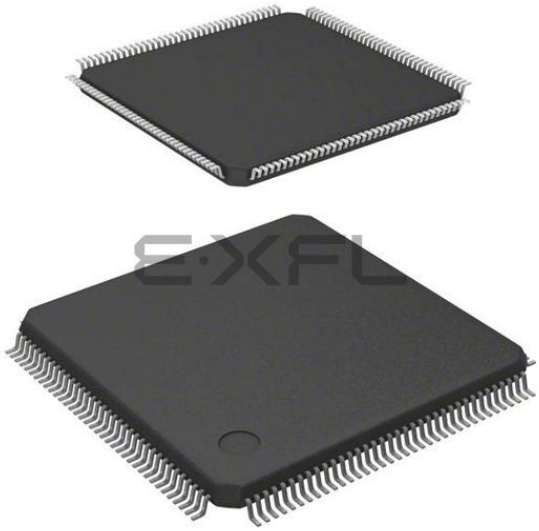
STMicroelectronics - SPC56EL60L5CBFQR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l5cbfqr

The SRAM module provides the following features:

- System SRAM: 128 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - 1 wait state for frequencies =< 120 MHz
  - 0 wait states for frequencies =< 80 MHz

1.5.7 Platform flash memory controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.
- Single-cycle read responses (0 AHB data-phase wait states) for hits in the buffers. The buffers implement a least-recently-used replacement algorithm to maximize performance.
- Programmable response for read-while-write sequences including support for stall-while-write, optional stall notification interrupt, optional flash operation abort, and optional abort notification interrupt.
- Separate and independent configurable access timing (on a per bank basis) to support use across a wide range of platforms and frequencies.
- Support of address-based read access timing for emulation of other memory types.
- Support for reporting of single- and multi-bit error events.
- Typical operating configuration loaded into programming model by system reset.

The platform flash controller is replicated for each processor.

1.5.8 Platform Static RAM Controller (SRAMC)

The SRAMC module is the platform SRAM array controller, with integrated error detection and correction.

The main features of the SRAMC provide connectivity for the following interfaces:

- XBAR Slave Port (64-bit data path)
- ECSM (ECC Error Reporting, error injection and configuration)
- SRAM array

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
62	$V_{SS\_HV\_IO}$	—		
63	$V_{DD\_HV\_IO}$	—		
64	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
65	$V_{DD\_LV\_COR}$	—		
66	$V_{SS\_LV\_COR}$	—		
67	$V_{DD\_HV\_REG\_1}$	—		
68	$V_{SS\_HV\_FLA}$	—		
69	$V_{DD\_HV\_FLA}$	—		
70	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
71	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
72	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
73	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
74	V_{PP_TEST}(1)	—		
75	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
83	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
84	JCOMP	—	—	JCOMP
85	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
86	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
87	$V_{DD\_HV\_IO}$	—		
88	$V_{SS\_HV\_IO}$	—		
89	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
90	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
91	$V_{DD\_HV\_REG\_2}$	—		
92	$V_{DD\_LV\_COR}$	—		
93	$V_{SS\_LV\_COR}$	—		
94	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
4	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
5	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
6	$V_{DD\_HV\_IO}$	—		
7	$V_{SS\_HV\_IO}$	—		
8	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
9	MDO0	—		
10	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
11	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
12	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
13	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
81	G[8]	SIUL	GPIO[104]	GPIO[104]
		FlexRay	DBG0	—
		DSPI_0	CS1	—
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[21]
82	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
83	G[7]	SIUL	GPIO[103]	GPIO[103]
		FlexPWM_0	B[3]	B[3]
84	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
85	G[5]	SIUL	GPIO[101]	GPIO[101]
		FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
86	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
87	TMS	—		
88	TCK	—		
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS\_HV\_IO}$	—		
91	$V_{DD\_HV\_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD\_LV\_COR}$	—		
94	$V_{SS\_LV\_COR}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
G14	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
G15	H[13]	SIUL	GPIO[125]	GPIO[125]
		FlexPWM_1	X[3]	X[3]
		eTimer_2	ETC[3]	ETC[3]
G16	H[9]	SIUL	GPIO[121]	GPIO[121]
		FlexPWM_1	B[1]	B[1]
		DSPI_0	CS7	—
G17	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
H1	G[13]	SIUL	GPIO[109]	GPIO[109]
		NPC	MDO[10]	—
H2	$V_{SS\_HV\_IO\_RING}$	—		
H3	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
H4	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
H6	V_{DD_LV}	—		
H7	V_{SS_LV}	—		
H8	V_{SS_LV}	—		
H9	V_{SS_LV}	—		
H10	V_{SS_LV}	—		
H11	V_{SS_LV}	—		
H12	V_{DD_LV}	—		
H14	V_{SS_LV}	—		
H15	$V_{DD\_HV\_REG\_1}$	—		
H16	$V_{DD\_HV\_FLA}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
N14	Not connected	—		
N15	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
N16	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
N17	G[5]	SIUL	GPIO[101]	GPIO[101]
		FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
P1	$V_{SS\_HV\_OSC}$	—		
P2	RESET	—		
P3	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
P4	$V_{DD\_LV\_PLL0\_PLL1}$	—		
P5	$V_{DD\_LV\_CORE\_RING}$	—		
P6	$V_{SS\_LV\_CORE\_RING}$	—		
P7	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
P8	Not connected	—		
P9	$V_{SS\_HV\_IO\_RING}$	—		
P10	$V_{DD\_HV\_IO\_RING}$	—		
P11	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
P12	$V_{DD\_LV\_CORE\_RING}$	—		
P13	$V_{SS\_LV\_CORE\_RING}$	—		
P14	$V_{DD\_HV\_IO\_RING}$	—		

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[14]	PCR[14]	SIUL	GPIO[14]	ALT0	GPIO[14]	—	—	M	S	99	143	B4
		FlexCAN_1	TXD	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=0						
		SIUL	—	—	EIRQ[13]	—						
A[15]	PCR[15]	SIUL	GPIO[15]	ALT0	GPIO[15]	—	—	M	S	100	144	D3
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=0						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=0						
		SIUL	—	—	EIRQ[14]	—						
Port B												
B[0]	PCR[16]	SIUL	GPIO[16]	ALT0	GPIO[16]	—	—	M	S	76	109	B15
		FlexCAN_0	TXD	ALT1	—	—						
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=0						
		SSCM	DEBUG[0]	ALT3	—	—						
		SIUL	—	—	EIRQ[15]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
G[11]	PCR[107]	SIUL	GPIO[107]	ALT0	GPIO[107]	—	—	M	S	—	75	U15
		FlexRay	DBG3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=2						
G[12]	PCR[108]	SIUL	GPIO[108]	ALT0	GPIO[108]	—	—	F	S	—	—	F2
		NPC	MDO[11]	ALT2	—	—						
G[13]	PCR[109]	SIUL	GPIO[109]	ALT0	GPIO[109]	—	—	F	S	—	—	H1
		NPC	MDO[10]	ALT2	—	—						
G[14]	PCR[110]	SIUL	GPIO[110]	ALT0	GPIO[110]	—	—	F	S	—	—	A6
		NPC	MDO[9]	ALT2	—	—						
G[15]	PCR[111]	SIUL	GPIO[111]	ALT0	GPIO[111]	—	—	F	S	—	—	J2
		NPC	MDO[8]	ALT2	—	—						
Port H												
H[0]	PCR[112]	SIUL	GPIO[112]	ALT0	GPIO[112]	—	—	F	S	—	—	A5
		NPC	MDO[7]	ALT2	—	—						
H[1]	PCR[113]	SIUL	GPIO[113]	ALT0	GPIO[113]	—	—	F	S	—	—	F1
		NPC	MDO[6]	ALT2	—	—						
H[2]	PCR[114]	SIUL	GPIO[114]	ALT0	GPIO[114]	—	—	F	S	—	—	A4
		NPC	MDO[5]	ALT2	—	—						
H[3]	PCR[115]	SIUL	GPIO[115]	ALT0	GPIO[115]	—	—	F	S	—	—	G1
		NPC	MDO[4]	ALT2	—	—						

Table 14. Thermal characteristics for LFBGA257 package(1)

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection(2)	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	26	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	37	°C/W
			Four layer board – 2s2p	22	
$R_{\theta JB}$	D	Thermal resistance junction-to-board(3)	—	13	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case(4)	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection(5)	—	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1: $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A= ambient temperature for the package (^oC)

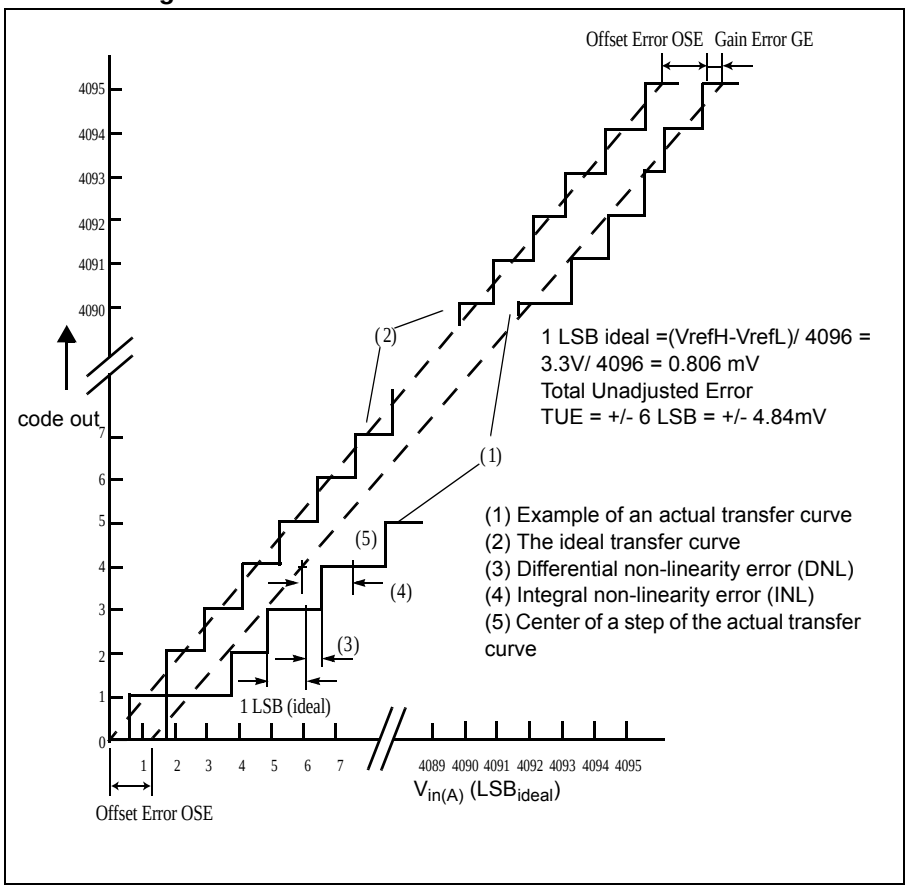
$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D= power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Figure 9. ADC characteristics and error definitions



3.16.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the *Equation 4*:

Table 33. RESET sequences

No.	Symbol		Parameter	Conditions	T_{Reset}			Unit
					Min	Typ	Max(1)	
1	T_{DRB}	CC	Destructive Reset Sequence, BIST enabled		28	34	39	ms
2	T_{DR}	CC	Destructive Reset Sequence, BIST disabled	—	500	4200	5000	µs
3	T_{ERLB}	CC	External Reset Sequence Long, BIST enabled		28	32	37	ms
4	T_{FRL}	CC	Functional Reset Sequence Long	—	35	150	400	µs
5	T_{FRS}	CC	Functional Reset Sequence Short	—	1	4	10	µs

1. The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

3.20.2 Reset sequence description

The figures in this section show the internal states of the chip during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in *Table 33*. The start point and end point conditions as well as the reset trigger mapping to the different reset sequences are specified in *Section 3.20.3*.

With the beginning of DRUN mode the first instruction is fetched and executed. At this point application execution starts and the internal reset sequence is finished.

The figures below show the internal states of the chip during the execution of the reset sequence and the possible states of the signal pin $\overline{\text{RESET}}$.

Note: $\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the chip internal reset circuitry. A high level on this pin can only be generated by an external pull up resistor which is strong enough to overdrive the weak internal pull down resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in table Table 33 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

Figure 14. Destructive Reset Sequence, BIST enabled

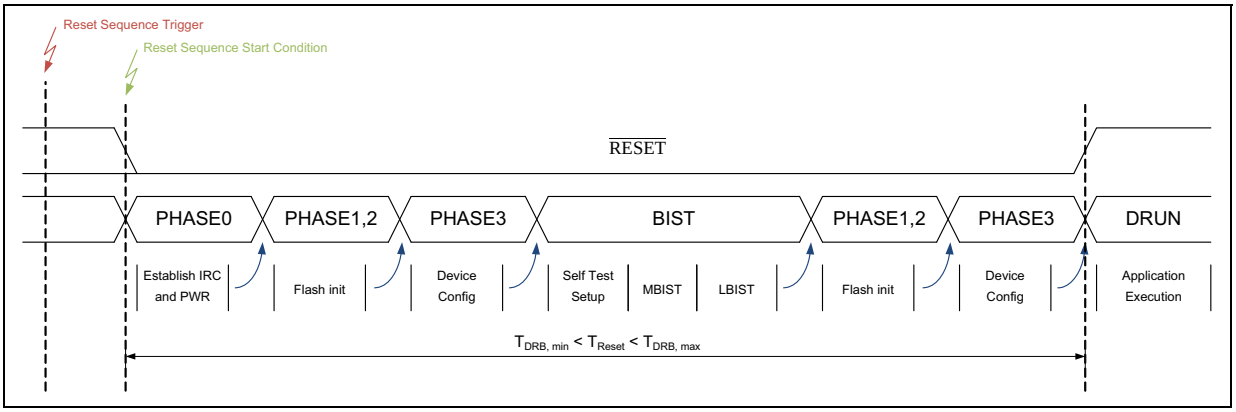
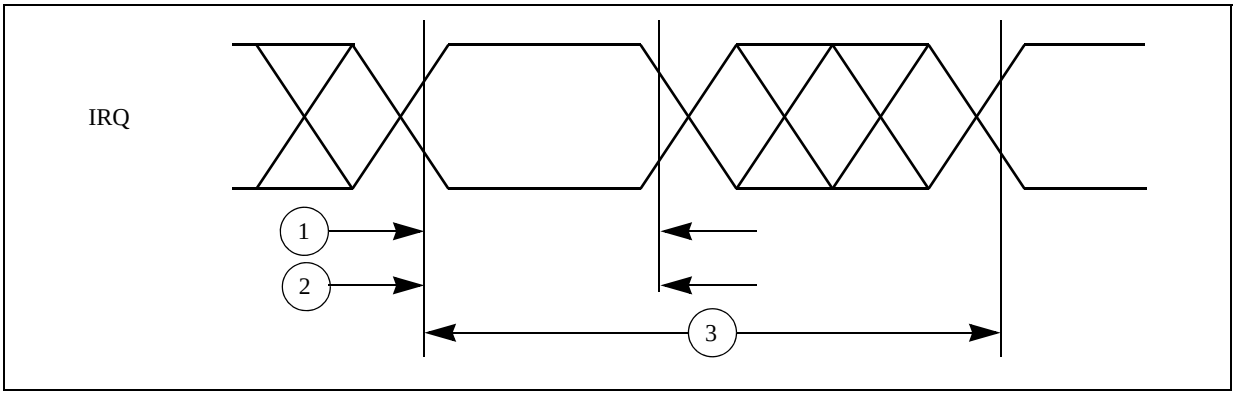


Figure 31. External interrupt timing



3.21.6 DSPI timing

Table 41. DSPI timing

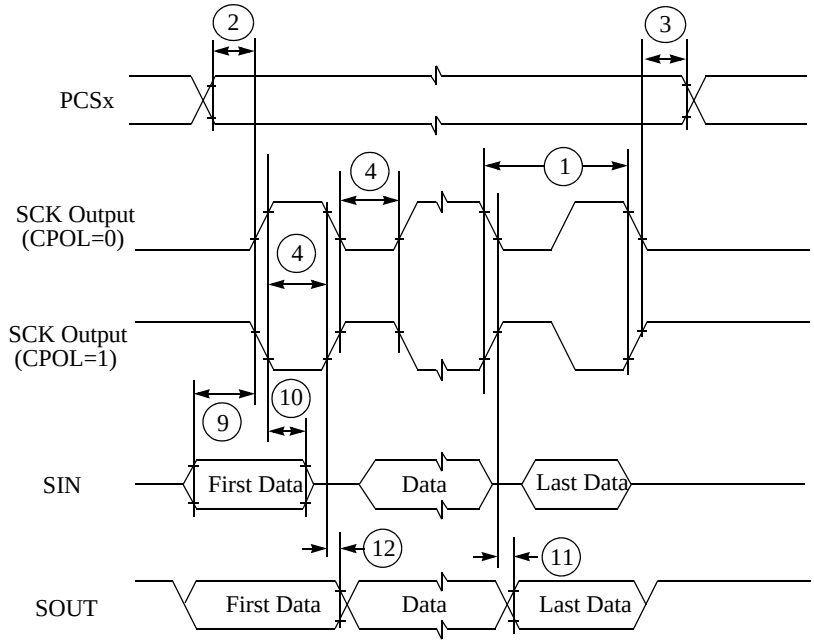
No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		D		Slave (MTFE = 0)	62	—	
		D		Slave Receive Only Mode(1)	16	—	
2	t_{CSC}	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	D	After SCK delay	—	16	—	ns
4	t_{SDC}	D	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	ns
5	t_A	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	12	
				Master (MTFE = 1, CPHA = 1)	—	4	

Table 41. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	

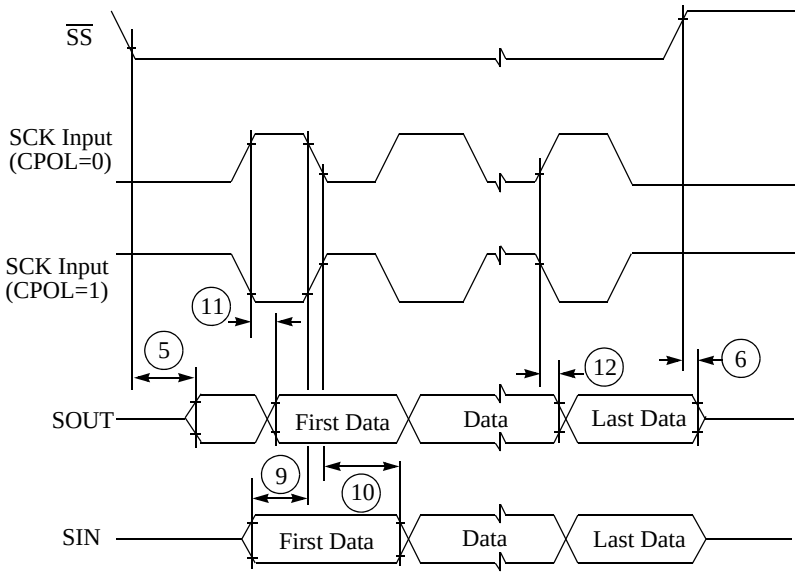
1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

Figure 32. DSPI classic SPI timing — master, CPHA = 0



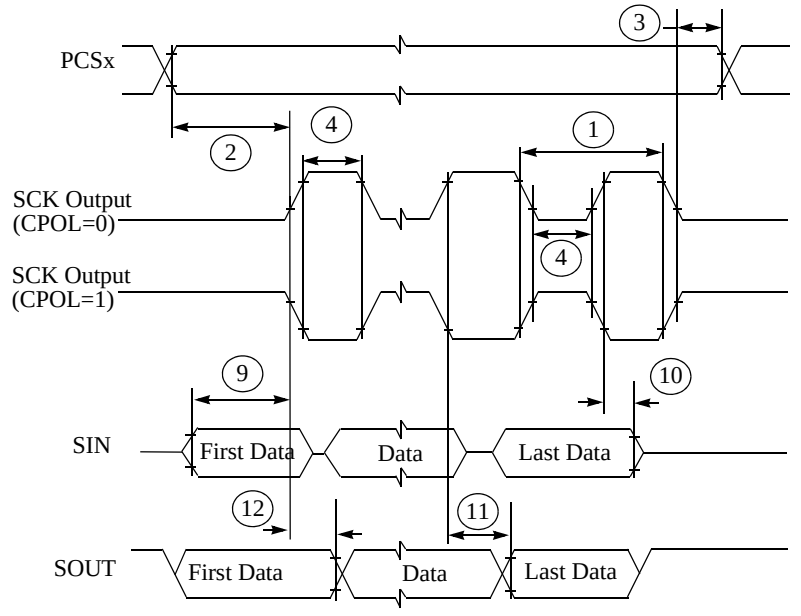
Note: The numbers shown are referenced in *Table 41*.

Figure 35. DSPI classic SPI timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 36. DSPI modified transfer format timing — master, CPHA = 0



Note: The numbers shown are referenced in *Table 41*.

Figure 42. LQFP144 package mechanical drawing

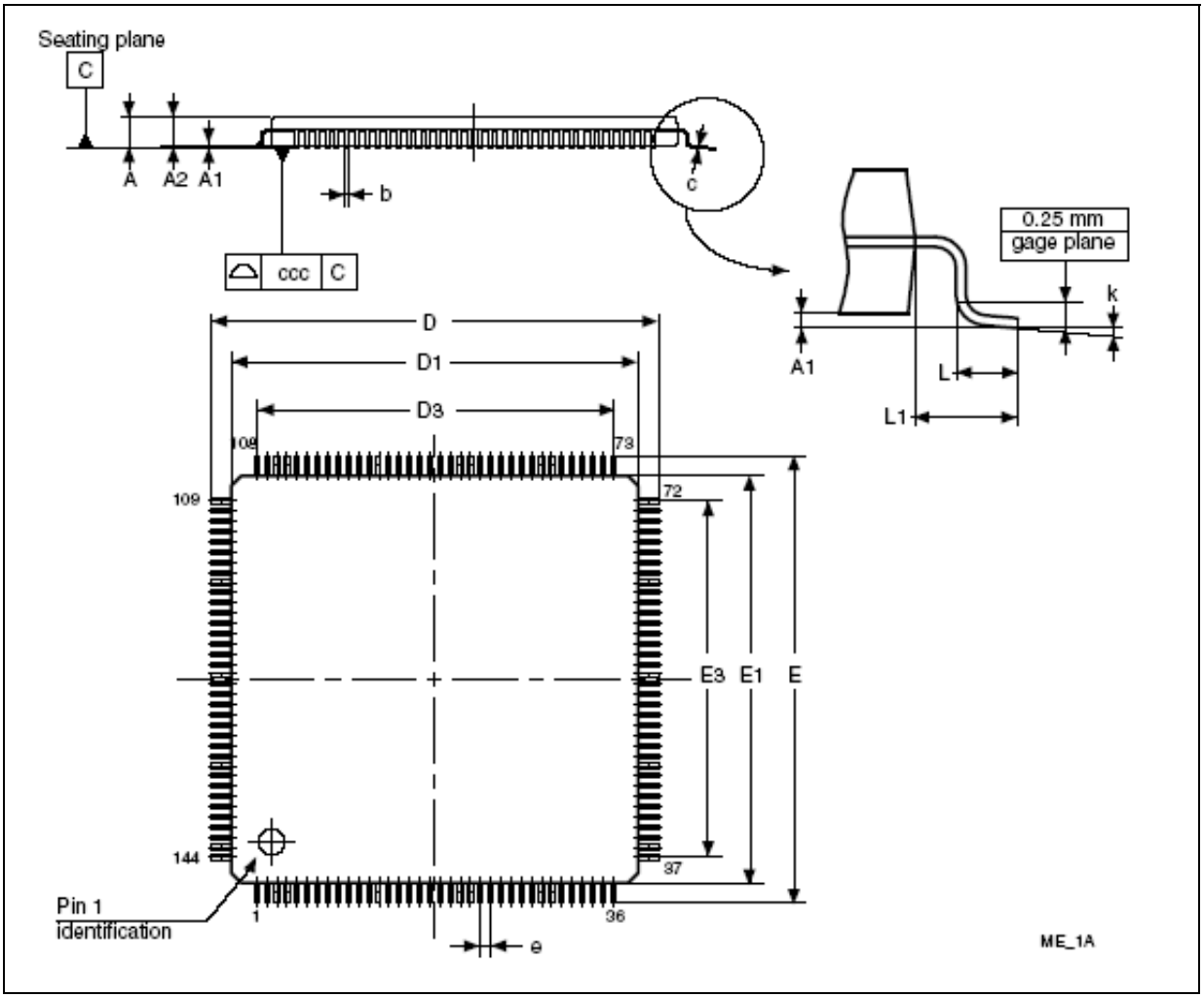


Table 43. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.0630
A1		0.05	0.15		0.0020	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	22	21.8	22.2	0.8661	0.8583	0.8740
D1	20	19.8	20.2	0.7874	0.7795	0.7953
D3	17.5			0.6890		
E	22	21.8	22.2	0.8661	0.8583	0.8740
E1	20	19.8	20.2	0.7874	0.7795	0.7953

Table 45. Document revision history

Date	Revision	Changes
23-Nov-2010	5 (continued)	In the “BCP68 board schematic example” figure, removed the resistor at the base of the BCP68 transistor. In the “DC electrical characteristics” table: – Changed the guarantee parameter for I_{INJ} (was P, is T). – Added a specification for input leakage current for shared ADC input-only ports. Revised the “Flash memory module life” table. In the “FMPLL electrical characteristics” table, revised the footnote defining f_{SCM} and f_{VCO}. In the “Main oscillator electrical characteristics” table: – Changed the max specification for $g_{mXOSCHS}$ (was 11.8 mA/V, is 13.25 mA/V). – Revised the conditions for $T_{XOSCHSSU}$. In the ‘RC oscillator electrical characteristics” table, deleted the specification for $\Delta_{RCMTRIM}$. Revised the “ADC conversion characteristics” table. In the “$\overline{\text{RESET}}$ pin characteristics” section, changed “n$\overline{\text{RSTIN}}$” to “$\overline{\text{RESET}}$”. Added the “Reset sequence” section. Revised the footnotes in the “Nexus debug port timing” table. Added the mechanical drawing for the 100-pin package. In the “Order codes” table, added a footnote about frequency modulation to the “Speed (MHz)” column heading.
23-Mar-2011	6	Editorial changes. In the “Document overview” section, added information about how content specific to silicon versions (“cut1” and “cut2”) is presented. In the isometric miniature package drawings on the front page, removed the third dimension. Changed Symbol from P to D for “Conversion Time” in “ADC conversion characteristics” table. Added classification symbol “D” to seven entries in “Voltage regulator electrical specifications“ table. Removed irrelevant FlexCAN specs. Updated Table “Voltage Thresholds” to reference values specified in Table “Voltage Regulator Electrical Specifications”. RDY pin added for cut2. In the “System pins” table, added a footnote about the MDO0 pad speed. Updated Rsw1 values. Added TUE-related spec information for single and double ADC channels. Added AC Test Timing Conditions to the “AC timing characteristics” section. Added a statement on the first page describing cut1 versus cut2. Moved the first paragraph from the “Description” section to the beginning of the “Document overview” section. Changed pad speed from “M” to “SYM” for FlexRay pins in the “Pin Muxing” table and added this pad type to the footnote. Moved the newly added device current specification entries from the “DC electrical characteristics“ table into a newly created “Supply current characteristics“ table.

Table 45. Document revision history

Date	Revision	Changes
23-Mar-2011	6 (continued)	Added symbol “CC” to the description in the “Introduction” section. Updated “Input leakage current” specs in the “DC electrical characteristics” table. Changed T_{ADC_S} to T_{sample} and T_{ADC_C} toT_{conv} in the “ADC conversion characteristics” table and footnotes. Removed “IINJ” from the “ADC conversion characteristics” table as this is included in IS1WIKNJ and IS1WWiNJ. Changed RESET_B to $\overline{\text{RESET}}$ in the "Reset sequence" section. Added the “Flash memory timing” table. Added cut2 specs for T_{DRB} and T_{ERLB} to the “Reset sequences” table. Added “WKUP/NMI Timing” subsection and “WKUP/NMI Glitch Filter” table to the “AC timing characteristics” section. Added “Nexus DDR Mode output timing” table to the “Nexus timing” section. Removed the “CLKOUT” diagram from the “External interrupt timing (IRQ pin)” section as it is not relevant. Corrected an error in the IRQ timing in the “External interrupt timing” figure. Updated the t_{SDC} parameters in the “DSPI timing” table. Renamed the “Electromagnetic Interference (EMI) characteristics” section (is “Electromagnetic Interference (EMI) characteristics (cut1)”) and revised all information in that section. In the “Voltage regulator electrical characteristics” section, added the BCX68 from Infineon to the list of supported transistors. Revised the “Voltage regulator electrical specifications” table to include cut1 and cut2 information. Renamed the “Supply current characteristics” section (is “Supply current characteristics (cut2)”) and revised it to show meaningful data. In the footnotes of the “Main oscillator electrical characteristics” table, changed SELMARGIN to XOSC_MARGIN. In the “ADC conversion characteristics” table: – Changed “LSB” to “Counts”. – Created separate rows for the TUE specifications. Removed the BGA row from the “Temperature” table entry. Added bullet regarding HALT and STOP in the “Clock, reset, power, mode and test control modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)” subsection of the “Features” section. In the “Analog-to-Digital Converter module “subsection of the “Feature Details” section, changed “Motor control mode” to “CTU mode” to be consistent with the nomenclature used in the Reference Manual. Updated the JCOMP entries in the “Pin function summary” table. Added footnotes regarding pad pull devices to NMI, TMS, TCK, and JCOMP in the “System pins” table. Added “Time constant of RC filter at LVD input” parameters to the “Main supply LVD (LVD Main) specifications” table.