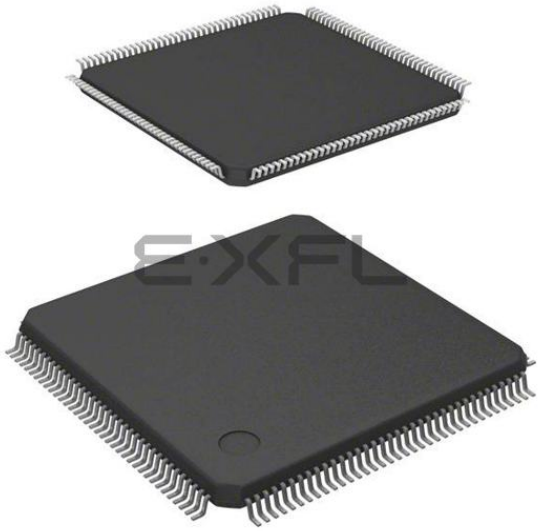

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l5cbfqy

List of figures

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56ELx/SPC564Lx series of microcontroller units (MCUs). For functional characteristics, see the *SPC56ELx/SPC564Lx Microcontroller Reference Manual*. For use of the SPC56ELx/SPC564Lx in a fail-safe system according to safety standard ISO26262, see the *Safety Application Guide for SPCEL60.*

1.2 Description

The SPC56ELx/SPC564Lx series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The SPC56ELx/SPC564Lx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the SPC56ELx/SPC564Lx automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

1.5.28 Serial communication interface module (LINFlexD)

The LINFlexD module (LINFlex with DMA support) on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 50-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, 16-bit, or 17-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (Parity, Noise and Framing errors)
  - Interrupt driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods
- Support for DMA enabled transfers

1.5.29 Deserial Serial Peripheral Interface (DSPI)

The DSPI modules provide a synchronous serial interface for communication between the SPC56ELx/SPC564Lx and external devices.

A DSPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase

1.5.37 Junction temperature sensor

The junction temperature sensor provides a value via an ADC channel that can be used by software to calculate the device junction temperature.

The key parameters of the junction temperature sensor include:

- Nominal temperature range from –40 to 150 °C
- Software temperature alarm via analog ADC comparator possible

1.5.38 Nexus Port Controller (NPC)

The NPC module provides real-time development support capabilities for this device in compliance with the IEEE-ISTO 5001-2003. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

The NPC block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2003 Class 3+, including selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the Power Architecture internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Full and reduced port modes
- MCKO (message clock out) pin
- 4 or 12 MDO (message data out) pins[b]
- 2 $\overline{\text{MSEO}}$ (message start/end out) pins
- $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
- $\overline{\text{EVTI}}$ (event in) pin
- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Supports JTAG mode
- Host processor (e200) development support features
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches,

b. 4 MDO pins on LQFP144 package, 12 MDO pins on LFBGA257 package.

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
83	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
84	JCOMP	—	—	JCOMP
85	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
86	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
87	$V_{DD\_HV\_IO}$	—		
88	$V_{SS\_HV\_IO}$	—		
89	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
90	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
91	$V_{DD\_HV\_REG\_2}$	—		
92	$V_{DD\_LV\_COR}$	—		
93	$V_{SS\_LV\_COR}$	—		
94	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
144	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1. V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 5. LFBGA257 pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
A1	$V_{SS\_HV\_IO\_RING}$	—		
A2	$V_{SS\_HV\_IO\_RING}$	—		
A3	$V_{DD\_HV\_IO\_RING}$	—		
A4	H[2]	SIUL	GPIO[114]	GPIO[114]
		NPC	MDO[5]	—

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
D17	G[3]	SIUL	GPIO[99]	GPIO[99]
		FlexPWM_0	A[2]	A[2]
		eTimer_0	—	ETC[4]
E1	MDO0	—		
E2	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
E3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
E4	NMI	—		
E14	Not connected	—		
E15	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
E16	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
E17	I[3]	SIUL	GPIO[131]	GPIO[131]
		eTimer_2	ETC[3]	ETC[3]
		DSPI_0	CS7	—
		CTU_0	EXT_TGR	—
		FlexPWM_1	—	FAULT[3]
F1	H[1]	SIUL	GPIO[113]	GPIO[113]
		NPC	MDO[6]	—
F2	G[12]	SIUL	GPIO[108]	GPIO[108]
		NPC	MDO[11]	—
F3	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
F4	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
F6	$V_{DD\_LV\_CORE\_RING}$	—		
F7	$V_{DD\_LV\_CORE\_RING}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
G14	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
G15	H[13]	SIUL	GPIO[125]	GPIO[125]
		FlexPWM_1	X[3]	X[3]
		eTimer_2	ETC[3]	ETC[3]
G16	H[9]	SIUL	GPIO[121]	GPIO[121]
		FlexPWM_1	B[1]	B[1]
		DSPI_0	CS7	—
G17	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
H1	G[13]	SIUL	GPIO[109]	GPIO[109]
		NPC	MDO[10]	—
H2	$V_{SS\_HV\_IO\_RING}$	—		
H3	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
H4	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
H6	V_{DD_LV}	—		
H7	V_{SS_LV}	—		
H8	V_{SS_LV}	—		
H9	V_{SS_LV}	—		
H10	V_{SS_LV}	—		
H11	V_{SS_LV}	—		
H12	V_{DD_LV}	—		
H14	V_{SS_LV}	—		
H15	$V_{DD\_HV\_REG\_1}$	—		
H16	$V_{DD\_HV\_FLA}$	—		

Table 6. Supply pins (continued)

Supply		Pin #		
Symbol	**Description**	**100 pkg**	**144 pkg**	**257 pkg**
$V_{DD\_HV\_REG\_1}$	VDD_HV_REG_1	67	95	H15
$V_{SS\_HV\_FLA}$	VSS_HV_FLA	68	96	J16
$V_{DD\_HV\_FLA}$	VDD_HV_FLA	69	97	H16
$V_{DD\_HV\_IO}$	VDD_HV_IO	87	126	VDD_HV(3)
$V_{SS\_HV\_IO}$	VSS_HV_IO	88	127	VSS_HV(4)
$V_{DD\_HV\_REG\_2}$	VDD_HV_REG_2	91	130	C7
Power supply pins (1.2 V)				
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17	VSS_HV(2)
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18	VDD_LV(1)
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.	24	35	N4
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.	25	36	P4
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	28	39	VDD_LV(1)
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	29	40	VSS_LV(2)
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	—	70	VDD_LV(1)
$V_{SS\_LV\_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	—	71	VSS_LV(2)
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	65	93	VDD_LV(1)
$V_{SS\_LV\_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	66	94	VSS_LV(2)
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	92	131	VDD_LV(1)

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[6]	PCR[6]	SIUL	GPIO[6]	ALT0	GPIO[6]	—	—	M	S	2	2	G4
		DSPI_1	SCK	ALT1	SCK	—						
		SIUL	—	—	EIRQ[6]	—						
A[7]	PCR[7]	SIUL	GPIO[7]	ALT0	GPIO[7]	—	—	M	S	4	10	F3
		DSPI_1	SOUT	ALT1	—	—						
		SIUL	—	—	EIRQ[7]	—						
A[8]	PCR[8]	SIUL	GPIO[8]	ALT0	GPIO[8]	—	—	M	S	6	12	F4
		DSPI_1	—	—	SIN	—						
		SIUL	—	—	EIRQ[8]	—						
A[9]	PCR[9]	SIUL	GPIO[9]	ALT0	GPIO[9]	—	—	M	S	94	134	B6
		DSPI_2	CS1	ALT1	—	—						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=0						
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	—	M	S	81	118	A13
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1						
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0						
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0						
		SIUL	—	—	EIRQ[9]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S	82	120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S	83	122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	—	M	S	95	136	C6
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1						
		SIUL	—	—	EIRQ[12]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	—	M	S	—	—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	—	M	S	—	—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	—	M	S	—	—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	—	F	S	—	—	K3
		NPC	RDY	ALT2	—	—						

1. Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)
2. The default function of this pin out of reset is ALT1 (TDO).
3. Analog

Note: Open Drain can be configured by the PCRn for all pins used as output (except FCCU_F[0] and FCCU_F[1]).

SPC56XL60/54 makes a transition from HPREG1 to HPREG2. This transition is dynamic. Once HPREG2 is fully operational, the controller part of HPREG1 is switched off.

The following bipolar transistors are supported:

- BCP68 from ON Semiconductor
- BCX68 from Infineon

Table 19. Characteristics

Symbol	Parameter	Value	Unit
$h_{FE}(\beta)$	DC current gain (Beta)	85 - 375	—
P_D	Maximum power dissipation @ T_A=25°C(1)	1.5	W
I_{CMaxDC}	Maximum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage (Max)	600(2)	mV
V_{BE}	Base-to-emitter voltage (Max)	1.0	V

1. Derating factor 12mW/degC.
2. Adjust resistor at bipolar transistor collector for 3.3V to avoid VCE<VCE_{SAT}.

The recommended external ballast transistor is the bipolar transistor BCP68 with the gain range of 85 up to 375 (for IC=500mA, VCE=1V) provided by several suppliers. This includes the gain variations BCP68-10, BCP68-16 and BCP68-25.The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter. SPC56XL60/54 Voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

Table 20. Voltage regulator electrical specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
C_{ext}		External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
	SR	Combined ESR of external capacitor	—	1	—	100	mΩ
	SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	300	—	900	nF
t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms

2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.
3. The max input voltage on the ADC pins is the ADC reference voltage VDD_HV_ADRx.
4. Measured values are applicable to all modes of the pad i.e. IBE = 0/1 and / or APC= 0/1.

3.11 Supply current characteristics

Current consumption data is given in *Table 22*. These specifications are design targets and are subject to change per device characterization.

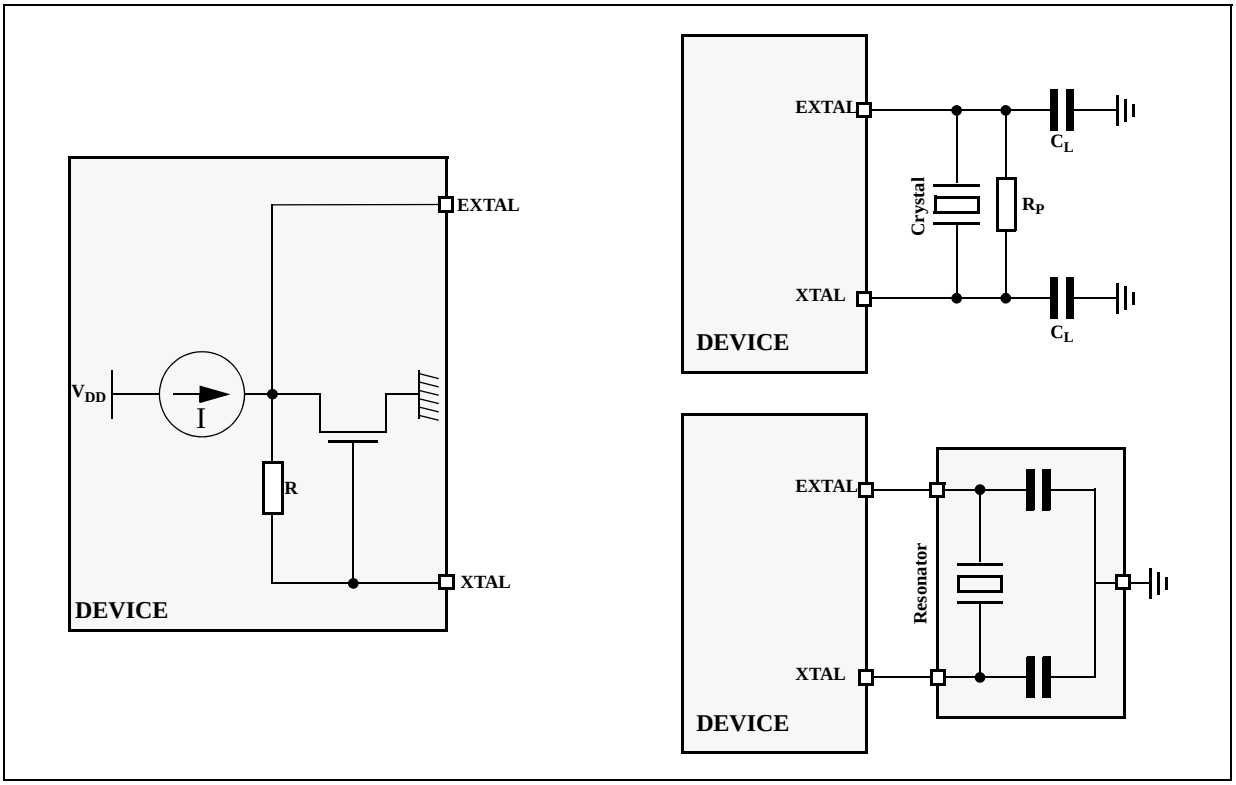
Table 22. Current consumption characteristics

Symbol		Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{DD\_LV\_FULL}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	50 mA+ 2.18 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	80 mA+ 2.50 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$(2)	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	26 + 2.10 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	41 mA+ 2.30 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies during LBIST (full LBIST configuration) T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	250	mA
			1.2 V supplies during LBIST (full LBIST configuration) T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	290	
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$(2)	P	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	279	mA
			T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	318	mA

3.13 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver. *Figure 7* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Figure 7. Crystal oscillator and resonator connection scheme



Note: XTAL/EXTAL must not be directly used to drive external circuits.

Table 27. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
IS1WWINJ			(double ADC channel)				
	C	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	Vref = 3.3V	67	—	—	dB
SNR	T	Signal-to-noise ratio	Vref = 5.0V	69	—	—	dB
THD	T	Total harmonic distortion	—	-65	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$	T	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
			With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$	P	Total unadjusted error for IS1WWINJ (double ADC channels)	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1. T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.
4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time Tsample, but only the time for determining the digital result.
6. See *Figure 10*.
7. For the 144-pin package
8. No missing codes

3.17 Flash memory electrical characteristics

Table 28. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Typ (1)	Initial Max (2)	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	*[4]	Double word (64 bits) program time[4]	30	—	500	µs
2	$T_{PPROGRAM}$	*[4]	Page(128 bits) program time[4]	40	160	500	µs
3	$T_{16KPPERASE}$	*[4]	16 KB block pre-program and erase time	250	1000	5000	ms
4	$T_{48KPPERASE}$	*[4]	48 KB block pre-program and erase time	400	1500	5000	ms
5	$T_{64KPPERASE}$	*[4]	64 KB block pre-program and erase time	450	1800	5000	ms
6	$T_{128KPPERASE}$	*[4]	128 KB block pre-program and erase time	800	2600	7500	ms
7	$T_{256KPPERASE}$	*[4]	256 KB block pre-program and erase time	1400	5200	15000	ms

1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25°C. These values are characterized, but not tested.

Figure 22. Start-up reset requirements

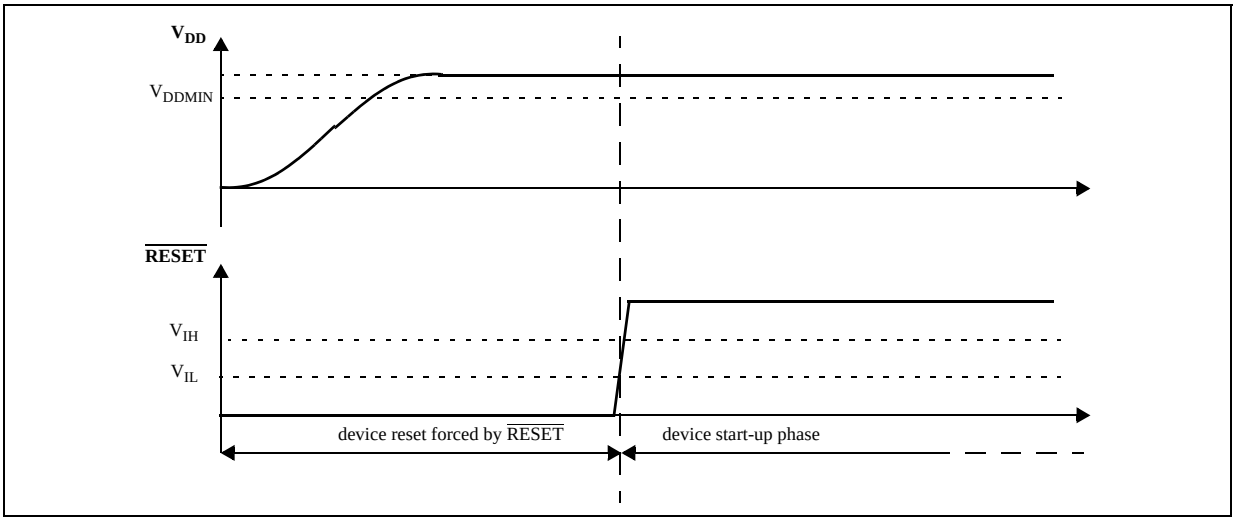


Figure 23. Noise filtering on reset signal

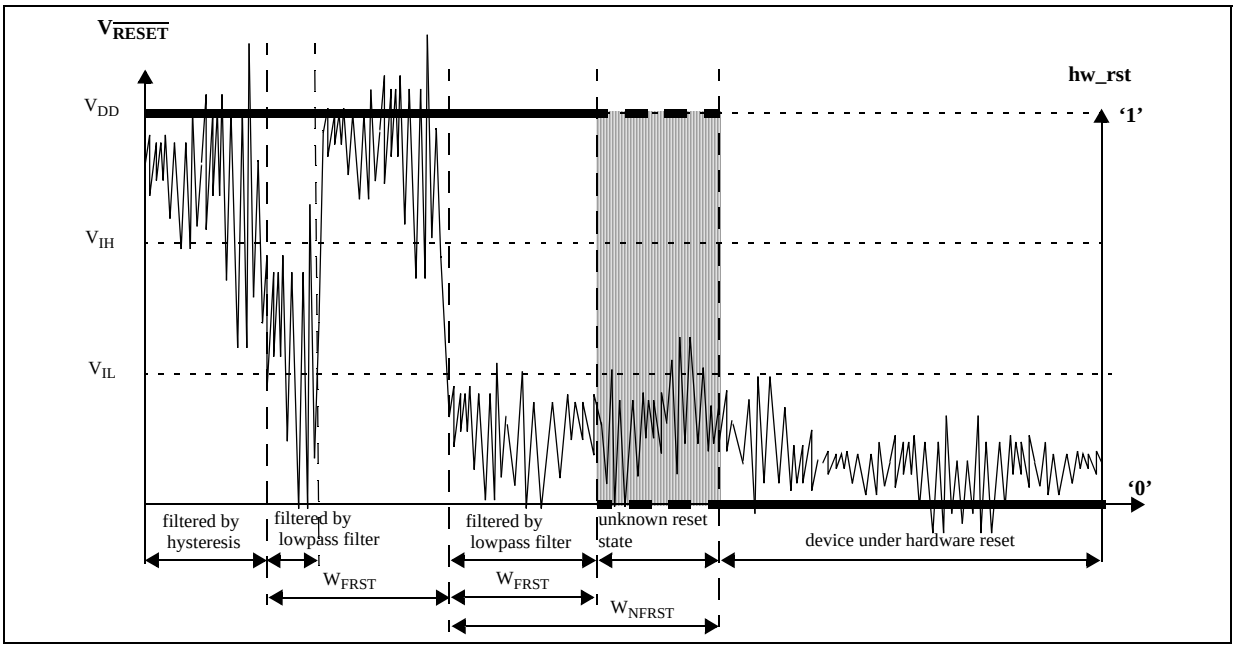
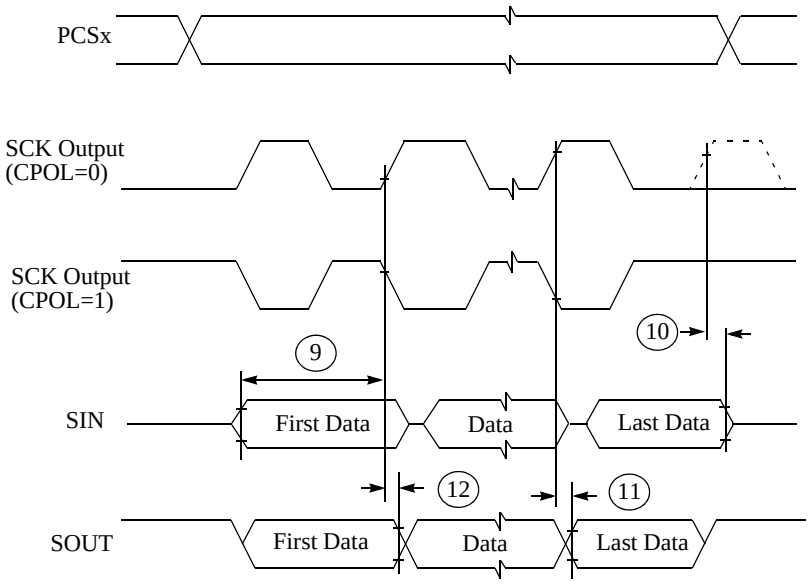


Table 36. RESET electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	nRESET input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	nRESET input not filtered pulse	—	500	—	—	ns

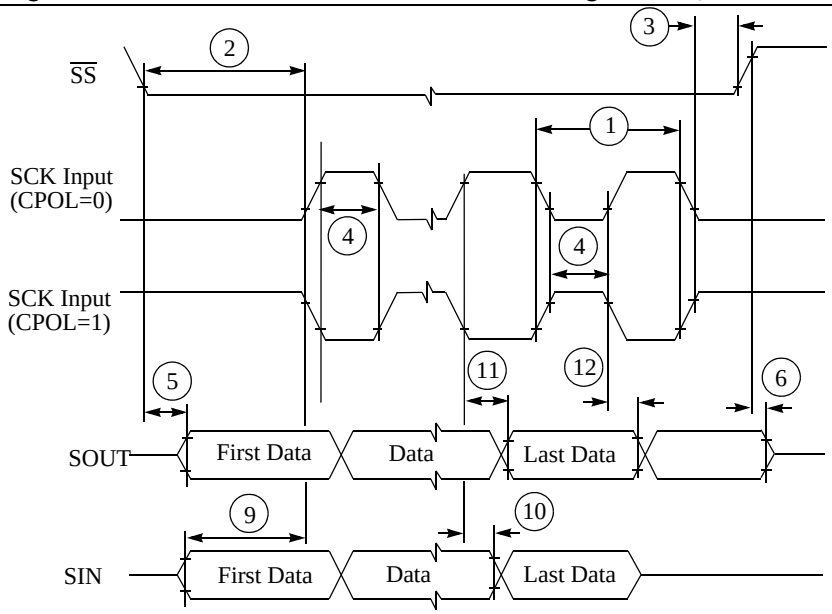
1. V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified.

Figure 37. DSPI modified transfer format timing — master, CPHA = 1



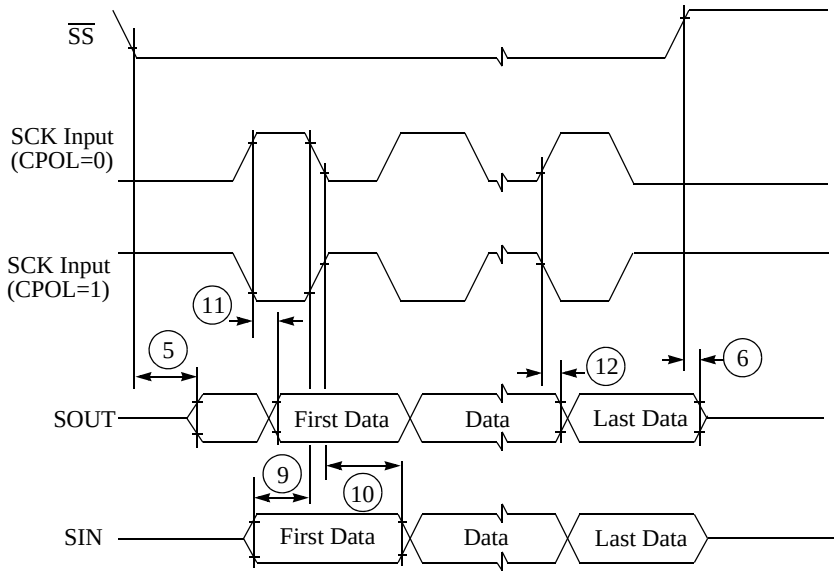
Note: The numbers shown are referenced in *Table 41*.

Figure 38. DSPI modified transfer format timing – slave, CPHA = 0



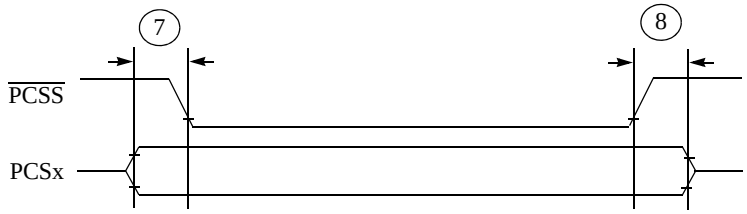
Note: The numbers shown are referenced in *Table 41*.

Figure 39. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 40. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing



Note: The numbers shown are referenced in *Table 41*.

Table 43. LQFP144 mechanical data (continued)

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
E3	17.5			0.6890		
e	0.5			0.0197		
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
k	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
Tolerance	mm			inches		
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 43. LFBGA257 package mechanical drawing