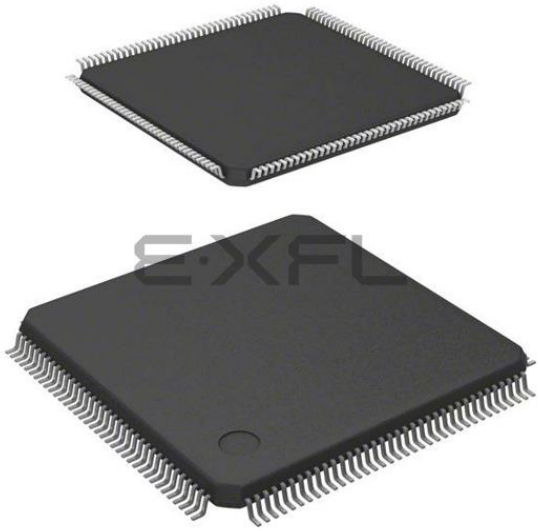

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l5cbfsr

1.5 Feature details

1.5.1 High-performance e200z4d core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow block for test, censorship device and user option bits
- Wait states:
  - 3 wait states for frequencies =< 120 MHz
  - 2 wait states for frequencies =< 80 MHz
  - 1 wait state for frequencies =< 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The SPC56ELx/SPC564Lx SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the FMPLL
- RC oscillator is used as the default system clock during startup and can be used as back-up input source of FMPLL(s) in case XOSC fails

1.5.17 Clock, reset, power, mode and test control modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)

These modules provide the following:

- Clock gating and clock distribution control
- Halt, stop mode control
- Flexible configurable system and auxiliary clock dividers
- Various execution modes
  - HALT and STOP mode as reduced activity low power mode
  - Reset, Idle, Test, Safe
  - Various RUN modes with software selectable powered modules
  - No stand-by mode implemented (no internal switchable power domains)

1.5.18 Periodic Interrupt Timer Module (PIT)

The PIT module implements the following features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Can be used for software tick or DMA trigger operation

1.5.19 System Timer Module (STM)

The STM implements the following features:

- Up-counter with 4 output compare registers
- OS task protection and hardware tick implementation per AUTOSAR[(a)] requirement

The STM is replicated for each processor.

1.5.20 Software Watchdog Timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

a. Automotive Open System Architecture.

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the LQFP100 pinout.

Figure 2. LQFP100 pinout

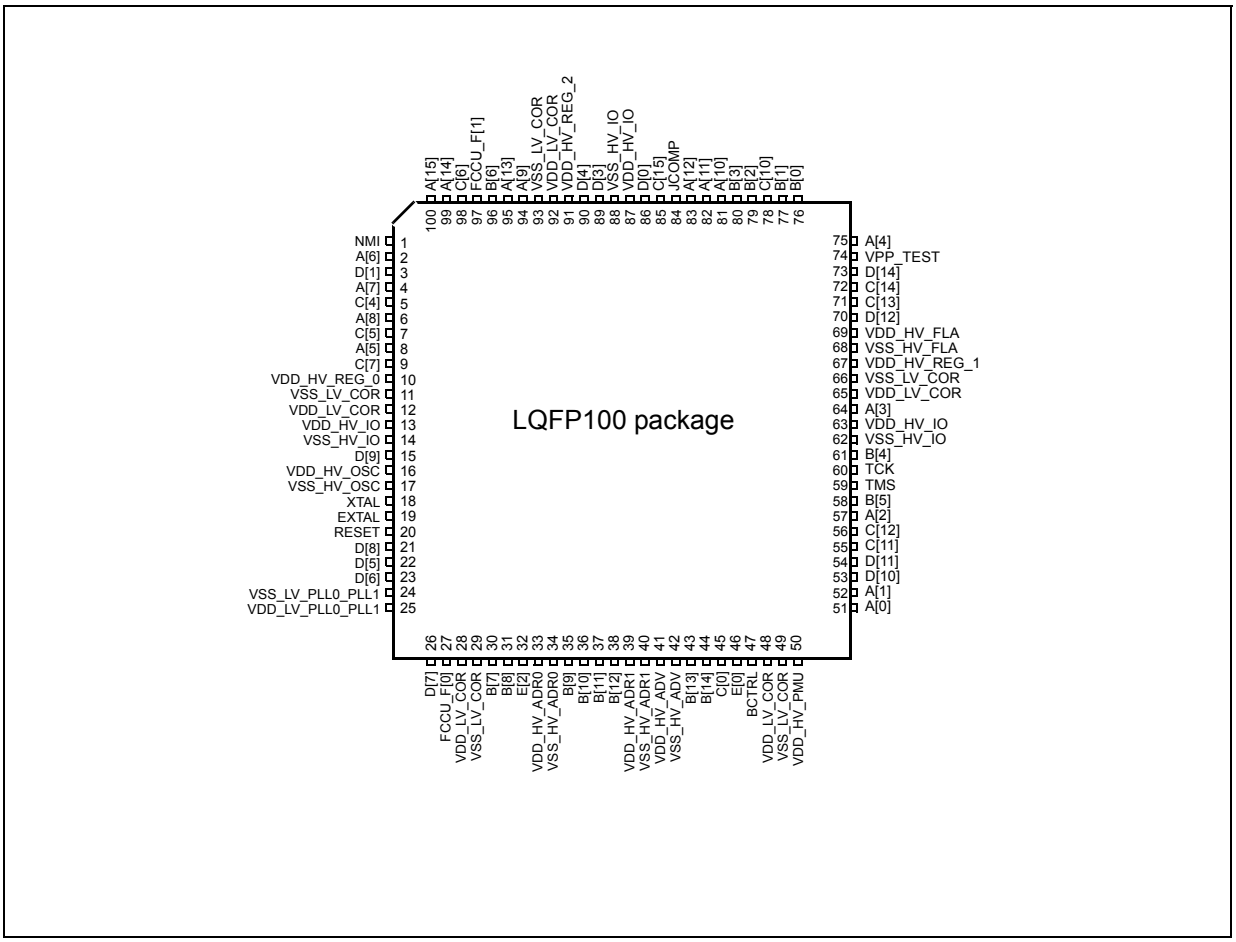


Figure 3 shows the SPC56ELx/SPC564Lx in the LQFP144 package.

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
4	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
5	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
6	$V_{DD\_HV\_IO}$	—		
7	$V_{SS\_HV\_IO}$	—		
8	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
9	MDO0	—		
10	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
11	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
12	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
13	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
L16	H[4]	SIUL	GPIO[116]	GPIO[116]
		FlexPWM_1	X[0]	X[0]
		eTimer_2	ETC[0]	ETC[0]
L17	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
M1	$V_{DD\_HV\_OSC}$	—		
M2	$V_{DD\_HV\_IO\_RING}$	—		
M3	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
M4	Not connected	—		
M6	V_{DD_LV}	—		
M7	V_{DD_LV}	—		
M8	V_{DD_LV}	—		
M9	V_{DD_LV}	—		
M10	V_{DD_LV}	—		
M11	V_{DD_LV}	—		
M12	V_{DD_LV}	—		
M14	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
M15	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
M16	TMS	—		
M17	H[5]	SIUL	GPIO[117]	GPIO[117]
		FlexPWM_1	A[0]	A[0]
		DSPI_0	CS4	—
N1	XTAL	—		
N2	$V_{SS\_HV\_IO\_RING}$	—		
N3	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
N4	$V_{SS\_LV\_PLL0\_PLL1}$	—		

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S	82	120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S	83	122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	—	M	S	95	136	C6
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1						
		SIUL	—	—	EIRQ[12]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—	43	60	R10
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=0						
		ADC_1	—	—	AN[0](3)	—						
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—	44	64	P11
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2						
		SIUL	—	—	EIRQ[19]	—						
		ADC_1	—	—	AN[1](3)	—						
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—	—	62	R11
		SIUL	—	—	EIRQ[20]	—						
		ADC_1	—	—	AN[2](3)	—						
Port C												
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—	45	66	R12
		ADC_1	—	—	AN[3](3)	—						
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—	—	41	T4
		ADC_0	—	—	AN[2](3)	—						
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—	—	45	U5
		ADC_0	—	—	AN[3](3)	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
E[4]	PCR[68]	SIUL	—	ALT0	GPI[68]	—	—	—	—	—	42	U4
		ADC_0	—	—	AN[7](3)	—						
E[5]	PCR[69]	SIUL	—	ALT0	GPI[69]	—	—	—	—	—	44	T5
		ADC_0	—	—	AN[8](3)	—						
E[6]	PCR[70]	SIUL	—	ALT0	GPI[70]	—	—	—	—	—	46	R6
		ADC_0	—	—	AN[4](3)	—						
E[7]	PCR[71]	SIUL	—	ALT0	GPI[71]	—	—	—	—	—	48	T6
		ADC_0	—	—	AN[6](3)	—						
E[9]	PCR[73]	SIUL	—	ALT0	GPI[73]	—	—	—	—	—	61	T10
		ADC_1	—	—	AN[7](3)	—						
E[10]	PCR[74]	SIUL	—	ALT0	GPI[74]	—	—	—	—	—	63	T11
		ADC_1	—	—	AN[8](3)	—						
E[11]	PCR[75]	SIUL	—	ALT0	GPI[75]	—	—	—	—	—	65	U11
		ADC_1	—	—	AN[4](3)	—						
E[12]	PCR[76]	SIUL	—	ALT0	GPI[76]	—	—	—	—	—	67	T12
		ADC_1	—	—	AN[6](3)	—						
E[13]	PCR[77]	SIUL	GPIO[77]	ALT0	GPIO[77]	—	—	M	S	—	117	D12
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=1						
		DSPI_2	CS3	ALT2	—	—						
		SIUL	—	—	EIRQ[25]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
FCCU												
FCCU_F[0]	—	FCCU	F[0]	ALT0	F[0]	—	—	S	S	27	38	R2
FCCU_F[1]	—	FCCU	F[1]	ALT0	F[1]	—	—	S	S	97	141	C4
Port G												
G[2]	PCR[98]	SIUL	GPIO[98]	ALT0	GPIO[98]	—	—	M	S	—	102	E16
		FlexPWM_0	X[2]	ALT1	X[2]	PSMI[29]; PADSEL=1						
		DSPI_1	CS1	ALT2	—	—						
G[3]	PCR[99]	SIUL	GPIO[99]	ALT0	GPIO[99]	—	—	M	S	—	104	D17
		FlexPWM_0	A[2]	ALT1	A[2]	PSMI[22]; PADSEL=2						
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=3						
G[4]	PCR[100]	SIUL	GPIO[100]	ALT0	GPIO[100]	—	—	M	S	—	100	F17
		FlexPWM_0	B[2]	ALT1	B[2]	PSMI[26]; PADSEL=2						
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=3						
G[5]	PCR[101]	SIUL	GPIO[101]	ALT0	GPIO[101]	—	—	M	S	—	85	N17
		FlexPWM_0	X[3]	ALT1	X[3]	PSMI[30]; PADSEL=2						
		DSPI_2	CS3	ALT2	—	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
H[11]	PCR[123]	SIUL	GPIO[123]	ALT0	GPIO[123]	—	—	M	S	—	—	C11
		FlexPWM_1	A[2]	ALT1	A[2]	—						
H[12]	PCR[124]	SIUL	GPIO[124]	ALT0	GPIO[124]	—	—	M	S	—	—	B10
		FlexPWM_1	B[2]	ALT1	B[2]	—						
H[13]	PCR[125]	SIUL	GPIO[125]	ALT0	GPIO[125]	—	—	M	S	—	—	G15
		FlexPWM_1	X[3]	ALT1	X[3]	—						
		eTimer_2	ETC[3]	ALT2	ETC[3]	PSMI[42]; PADSEL=0						
H[14]	PCR[126]	SIUL	GPIO[126]	ALT0	GPIO[126]	—	—	M	S	—	—	A12
		FlexPWM_1	A[3]	ALT1	A[3]	—						
		eTimer_2	ETC[4]	ALT2	ETC[4]	—						
H[15]	PCR[127]	SIUL	GPIO[127]	ALT0	GPIO[127]	—	—	M	S	—	—	J17
		FlexPWM_1	B[3]	ALT1	B[3]	—						
		eTimer_2	ETC[5]	ALT2	ETC[5]	—						
Port I												
I[0]	PCR[128]	SIUL	GPIO[128]	ALT0	GPIO[128]	—	—	M	S	—	—	C9
		eTimer_2	ETC[0]	ALT1	ETC[0]	PSMI[39]; PADSEL=1						
		DSPI_0	CS4	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[0]	—						

Table 11. Decoupling capacitors (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
C_{PMU1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		µF
C_{PMU2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{REG}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		20		µF
C_{IO1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{IO2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		470		pF
C_{FLA1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{FLA2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{OSC1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{OSC2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{PLL1}	SR	External decoupling / stability capacitor		22		100	nF
C_{ADR1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADR2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADR3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF
C_{ADV1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADV2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADV3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF

1. Capacitors shall be placed as close as possible to the respective pads.
2. Total ESR considering all decoupling capacitor close to the $V_{DD}/V_{SS\_LV\_CORy}$ pairs shall be between 1 mΩ and 100 mΩ.

3.5 Thermal characteristics

Table 12. Thermal characteristics for LQFP100 package(1)

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection(2)	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	34	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	36	°C/W
			Four layer board – 2s2p	28	
$R_{\theta JB}$	D	Thermal resistance junction-to-board(3)	—	19	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case(4)	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection(5)	—	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 13. Thermal characteristics for LQFP144 package(1)

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection(2)	Single layer board – 1s	44	°C/W
			Four layer board – 2s2p	36	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	35	°C/W
			Four layer board – 2s2p	30	
$R_{\theta JB}$	D	Thermal resistance junction-to-board(3)	—	24	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case(4)	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection(5)	—	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.6 Electromagnetic Interference (EMI) characteristics

The characteristics in *Table 16* were measured using:

- Device configuration, test conditions, and EM testing per standard IEC61967-2
- Supply voltage of 3.3 V DC
- Ambient temperature of 25 °C

The configuration information referenced in *Table 16* is explained in *Table 15*.

Table 15. EMI configuration summary

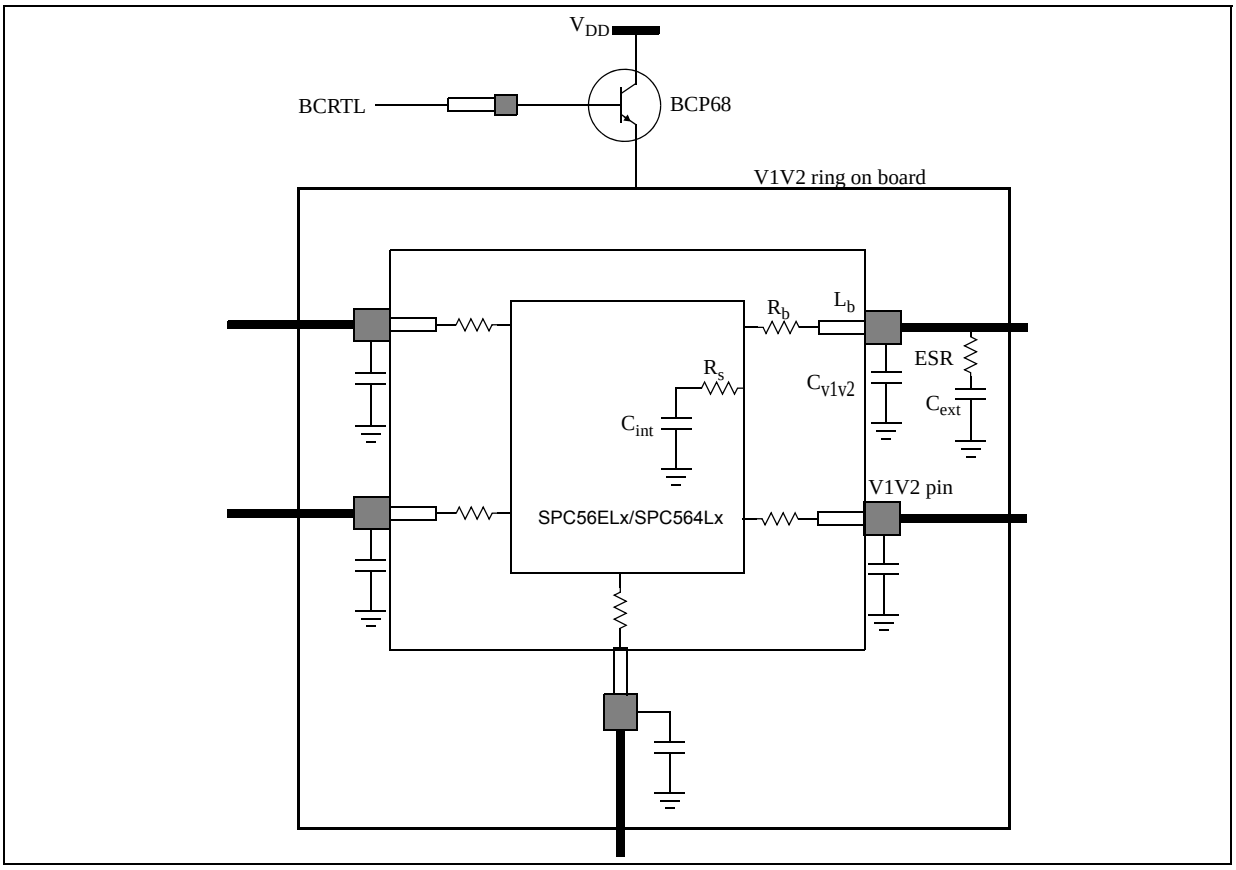
Configuration name	Description
Configuration A	– High emission = all pads have max slew rate, LVDS pads running at 40 MHz – Oscillator frequency = 40 MHz – System bus frequency = 80 MHz – No PLL frequency modulation – IEC level I (≤ 36 dBµV)
Configuration B	– Reference emission = pads use min, mid and max slew rates, LVDS pads disabled – Oscillator frequency = 40 MHz – System bus frequency = 80 MHz – 2% PLL frequency modulation – IEC level K(≤ 30 dBµV)

Table 16. EMI emission testing specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{EME}	CC	Radiated emissions	Configuration A; frequency range 150 kHz–50 MHz	—	16	—	dBµV
			Configuration A; frequency range 50–150 MHz	—	16	—	
			Configuration A; frequency range 150–500 MHz	—	32	—	
			Configuration A; frequency range 500–1000 MHz	—	25	—	
			Configuration B; frequency range 50–150 MHz	—	15	—	
			Configuration B; frequency range 50–150 MHz	—	21	—	
			Configuration B; frequency range 150–500 MHz	—	30	—	
			Configuration B; frequency range 500–1000 MHz	—	24	—	

EMC testing was performed and documented according to these standards: [IEC61508-2-7.4.5.1.b, IEC61508-2-7.2.3.2.e, IEC61508-2-Table-A.17 (partially), IEC61508-2-Table-B.5(partially),SRS2110]

Figure 6. BCP68 board schematic example



Note: The minimum value of the ESR is constrained by the resonance caused by the external components, bonding inductance, and internal decoupling. The minimum ESR is required to avoid the resonance and make the regulator stable.

3.10 DC electrical characteristics

Table 21 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V).

Table 21. DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(2)	—	—	V
V_{IL}	P	Maximum low level input voltage	—	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	—	V
V_{IH}	D	Maximum high level input voltage	—	—	—	$V_{DD\_HV\_IOx}$ + 0.1(2), (3)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	—	V

3.18 SWG electrical characteristics

Table 31. SPC56XL60/54 SWG Specifications

Symbol	Parameter	Value		
		Minimum	Typical	Maximum
T	Input clock	12 MHz	16 MHz	20 MHz
T	Frequency Range	1 kHz	—	50 kHz
T	Peak to Peak(1)	0.4 V	—	2.0V
T	Peak to Peak variation(2)	-6%	—	6%
T	Common Mode(3)	—	1.3 V	—
T	Common Mode variation	-6%	—	6%
T	SiNAD(4)	45 dB	—	—
T	Load C	25 pF	—	100 pF
T	Load I	0 µA	—	100 µA
T	ESD Pad Resistance(5)	230 Ω	—	360 Ω

1. Peak to Peak value is measured with no R or I load.
2. Peak to Peak excludes noise, SiNAD must be considered.
3. Common mode value is measured with no R or I load.
4. SiNAD is measured at Max Peak to Peak voltage.
5. Internal device routing resistance. ESD pad resistance is in series and must be considered for max Peak to Peak voltages, depending on application I load and/or R load.

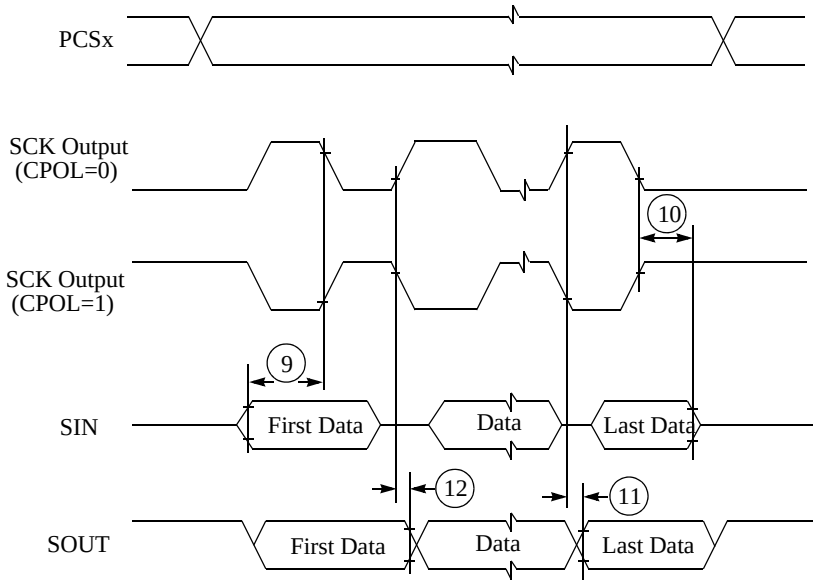
3.19 AC specifications

3.19.1 Pad AC specifications

Table 32. Pad AC specifications (3.3 V, IPP_HVE = 0)(1)

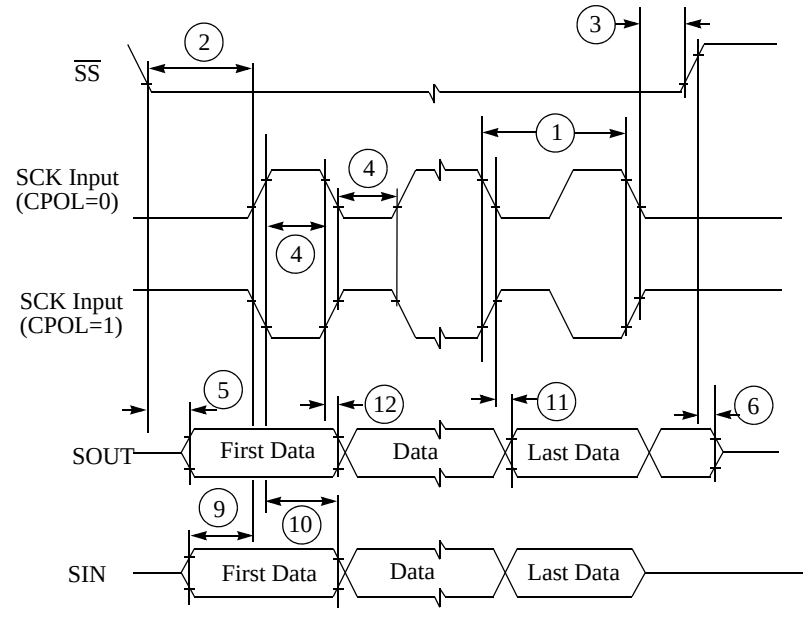
No.	Pad		Tswitchon(1)(ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200

Figure 33. DSPI classic SPI timing — master, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 34. DSPI classic SPI timing — slave, CPHA = 0



Note: The numbers shown are referenced in *Table 41*.

Table 42. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 45. Document revision history

Date	Revision	Changes
14-Jun-2010	4 (continued)	In the “Main oscillator electrical characteristics” table, changed the maximum specification for $g_{mXOSCHS}$ (was 11 mA/V, is 11.8 mA/V). Revised the “ADC electrical characteristics” section.In the “ADC conversion characteristics” table: – Changed the t_{ADC_S} specification (was TBD, is minimum of 383 ns). – Added the footnote “No missing codes” to the DNL specification. – Added specifications for SNR, THD, SINAD, and ENOB. Revised the “Ordering information” section.
23-Nov-2010	5	Editorial changes and improvements. Revised the Overview section. Replaced references to PowerPC with references to Power Architecture. In the feature summary, changed “As much as 128 KB on-chip SRAM” to “128 KB on-chip SRAM”. In the “Feature details” section: – In the “On-chip SRAM with ECC” section, added information about required RAM wait states. – In the PIT section, deleted “32-bit counter for real time interrupt, clocked from main external oscillator” (not supported on this device). – In the flash-memory section, changed “16 KB Test” to “16 KB test sector”, revised the wait state information, and deleted the associated Review_Q&A content. – In the SRAM section, revised the wait state information. In the 100-pin pinout diagram: – Renamed pin 41 (was VDD_HV_ADV0_ADV1, is VDD_HV_ADV). – Renamed pin 42 (was VSS_HV_ADV0_ADV1, is VSS_HV_ADV). In the 144-pin pinout diagram: – Renamed pin 58 (was VDD_HV_ADV0_ADV1, is VDD_HV_ADV). – Renamed pin 59 (was VSS_HV_ADV0_ADV1, is VSS_HV_ADV). Added the “LQFP100 pin function summary” table. In the “LQFP144 pin function summary” table, for pin 39, changed $V_{SS\_LV\_COR}$ to $V_{DD\_LV\_COR}$. In the “Supply pins” table: – Changed the description for $V_{DD\_LV\_COR}$ (was “Voltage regulator supply voltage”, is “Core logic supply”). – Changed the description for $V_{DD\_HV\_PMU}$ (was “Core regulator supply”, is “Voltage regulator supply”). In the “Pin muxing” table: – In the “Pad speed” column headings, changed “SRC = 0” to “SRC = 1” and “SRC = 1” to “SRC = 0” – For port B[6], changed the pad speed for SRC=0 (was M, is F). In the “Thermal characteristics” section, added meaningful values to the thermal-characteristics tables. Added the “SWG electrical specifications” section. In the “Voltage regulator electrical characteristics” section, changed the table title (was “HPREG1, HPREG2, Main LVDs, Digital HVD, and Digital LVD electrical specifications”, is “Voltage regulator electrical characteristics”) and revised the table.

Table 45. Document revision history

Date	Revision	Changes
18-Sep-2013	10	– Updated Disclaimer.
07-Feb-2014	11	– Removed “TBC” symbol in *Table 9* and *Table 22* – Resolved some cross references.
08-Jul-2015	12	Editorial and formatting changes throughout document. *Chapter 1: Introduction*: – In *Table 1: SPC56ELx/SPC564Lx device summary* added the column for SPC56EL54 device *Chapter 3: Electrical characteristics*: – In *Table 9: Absolute maximum ratings*, added condition “Valid only for ADC pins” for V_{IN} Symbol. – Added *Section 3.4: Decoupling capacitors*. – *Figure 10: Input Equivalent Circuit*: changed “V_{DD}” to “V_{REF}” in Internal circuit scheme – In *Table 32: Pad AC specifications (3.3 V, IPP_HVE = 0)* updated footnote 1 and footnote 2. – Updated *Figure 13: Pad output delay* Updated Disclaimer.