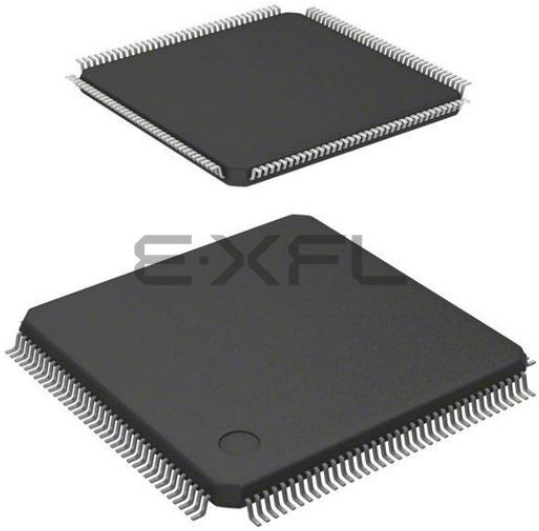

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l5cbfsy

1.5.13 System clocks and clock generation

The following list summarizes the system clock and clock generation on this device:

- Lock status continuously monitored by lock detect circuitry
- Loss-of-clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and fewer external components required)
- Programmable output clock divider of system clock (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and as many as three eTimer modules running on an auxiliary clock independent from system clock (with max frequency 120 MHz)
- On-chip crystal oscillator with automatic level control
- Dedicated internal 16 MHz internal RC oscillator for rapid start-up
  - Supports automated frequency trimming by hardware during device startup and by user application
- Auxiliary clock domain for motor control periphery (FlexPWM, eTimer, CTU, ADC, and SWG)

- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as 8 chip select lines available, depending on package and pin multiplexing
- 4 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.30 FlexPWM

The pulse width modulator module (FlexPWM) contains four PWM channels, each of which is configured to control a single half-bridge power stage. Two modules are included on LFBGA257 devices; on the LQFP144 package, only one module is present. Additionally, four fault input channels are provided per FlexPWM module.

This PWM is capable of controlling most motor types, including:

- AC induction motors (ACIM)
- Permanent Magnet AC motors (PMAC)
- Brushless (BLDC) and brush DC motors (BDC)
- Switched (SRM) and variable reluctance motors (VRM)
- Stepper motors

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via secondary FMPLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values

1.5.40 Voltage regulator / Power Management Unit (PMU)

The on-chip voltage regulator module provides the following features:

- Single external rail required
- Single high supply required: nominal 3.3 V both for packaged and Known Good Die option
  - Packaged option requires external ballast transistor due to reduced dissipation capacity at high temperature but can use embedded transistor if power dissipation is maintained within package dissipation capacity (lower frequency of operation)
  - Known Good Die option uses embedded ballast transistor as dissipation capacity is increased to reduce system cost
- All I/Os are at same voltage as external supply (3.3 V nominal)
- Duplicated Low-Voltage Detectors (LVD) to guarantee proper operation at all stages (reset, configuration, normal operation) and, to maximize safety coverage, one LVD can be tested while the other operates (on-line self-testing feature)

1.5.41 Built-In Self-Test (BIST) capability

This device includes the following protection against latent faults:

- Boot-time Memory Built-In Self-Test (MBIST)
- Boot-time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

Figure 4. SPC56ELx/SPC564Lx LFBGA257 pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC(1)	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]		C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1. NC = Not connected (the pin is physically not connected to anything on the device).

Table 3, *Table 4*, and *Table 5* provide the pin function summaries for the 100-pin, 144-pin, and 257-pin packages, respectively, listing all the signals multiplexed to each pin.

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
4	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
5	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
6	$V_{DD\_HV\_IO}$	—		
7	$V_{SS\_HV\_IO}$	—		
8	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
9	MDO0	—		
10	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
11	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
12	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
13	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD\_HV\_IO}$	—		
127	$V_{SS\_HV\_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD\_HV\_REG\_2}$	—		
131	$V_{DD\_LV\_COR}$	—		
132	$V_{SS\_LV\_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD\_LV\_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS\_LV\_COR}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
D3	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]
D4	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
D5	$V_{SS\_LV\_CORE\_RING}$	—		
D6	$V_{DD\_LV\_CORE\_RING}$	—		
D7	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
D8	$V_{DD\_HV\_IO\_RING}$	—		
D9	$V_{SS\_HV\_IO\_RING}$	—		
D10	Not connected	—		
D11	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
D12	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
D13	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
D14	$V_{DD\_HV\_IO\_RING}$	—		
D15	V_{PP_TEST}(1)	—		
D16	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
FCCU												
FCCU_F[0]	—	FCCU	F[0]	ALT0	F[0]	—	—	S	S	27	38	R2
FCCU_F[1]	—	FCCU	F[1]	ALT0	F[1]	—	—	S	S	97	141	C4
Port G												
G[2]	PCR[98]	SIUL	GPIO[98]	ALT0	GPIO[98]	—	—	M	S	—	102	E16
		FlexPWM_0	X[2]	ALT1	X[2]	PSMI[29]; PADSEL=1						
		DSPI_1	CS1	ALT2	—	—						
G[3]	PCR[99]	SIUL	GPIO[99]	ALT0	GPIO[99]	—	—	M	S	—	104	D17
		FlexPWM_0	A[2]	ALT1	A[2]	PSMI[22]; PADSEL=2						
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=3						
G[4]	PCR[100]	SIUL	GPIO[100]	ALT0	GPIO[100]	—	—	M	S	—	100	F17
		FlexPWM_0	B[2]	ALT1	B[2]	PSMI[26]; PADSEL=2						
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=3						
G[5]	PCR[101]	SIUL	GPIO[101]	ALT0	GPIO[101]	—	—	M	S	—	85	N17
		FlexPWM_0	X[3]	ALT1	X[3]	PSMI[30]; PADSEL=2						
		DSPI_2	CS3	ALT2	—	—						

Table 11. Decoupling capacitors (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
C_{PMU1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		µF
C_{PMU2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{REG}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		20		µF
C_{IO1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{IO2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		470		pF
C_{FLA1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{FLA2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{OSC1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{OSC2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{PLL1}	SR	External decoupling / stability capacitor		22		100	nF
C_{ADR1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADR2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADR3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF
C_{ADV1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADV2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADV3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF

1. Capacitors shall be placed as close as possible to the respective pads.
2. Total ESR considering all decoupling capacitor close to the $V_{DD}/V_{SS\_LV\_CORy}$ pairs shall be between 1 mΩ and 100 mΩ.

3.6 Electromagnetic Interference (EMI) characteristics

The characteristics in *Table 16* were measured using:

- Device configuration, test conditions, and EM testing per standard IEC61967-2
- Supply voltage of 3.3 V DC
- Ambient temperature of 25 °C

The configuration information referenced in *Table 16* is explained in *Table 15*.

Table 15. EMI configuration summary

Configuration name	Description
Configuration A	– High emission = all pads have max slew rate, LVDS pads running at 40 MHz – Oscillator frequency = 40 MHz – System bus frequency = 80 MHz – No PLL frequency modulation – IEC level I (≤ 36 dBµV)
Configuration B	– Reference emission = pads use min, mid and max slew rates, LVDS pads disabled – Oscillator frequency = 40 MHz – System bus frequency = 80 MHz – 2% PLL frequency modulation – IEC level K(≤ 30 dBµV)

Table 16. EMI emission testing specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{EME}	CC	Radiated emissions	Configuration A; frequency range 150 kHz–50 MHz	—	16	—	dBµV
			Configuration A; frequency range 50–150 MHz	—	16	—	
			Configuration A; frequency range 150–500 MHz	—	32	—	
			Configuration A; frequency range 500–1000 MHz	—	25	—	
			Configuration B; frequency range 50–150 MHz	—	15	—	
			Configuration B; frequency range 50–150 MHz	—	21	—	
			Configuration B; frequency range 150–500 MHz	—	30	—	
			Configuration B; frequency range 500–1000 MHz	—	24	—	

EMC testing was performed and documented according to these standards: [IEC61508-2-7.4.5.1.b, IEC61508-2-7.2.3.2.e, IEC61508-2-Table-A.17 (partially), IEC61508-2-Table-B.5(partially),SRS2110]

2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.
3. The max input voltage on the ADC pins is the ADC reference voltage VDD_HV_ADRx.
4. Measured values are applicable to all modes of the pad i.e. IBE = 0/1 and / or APC= 0/1.

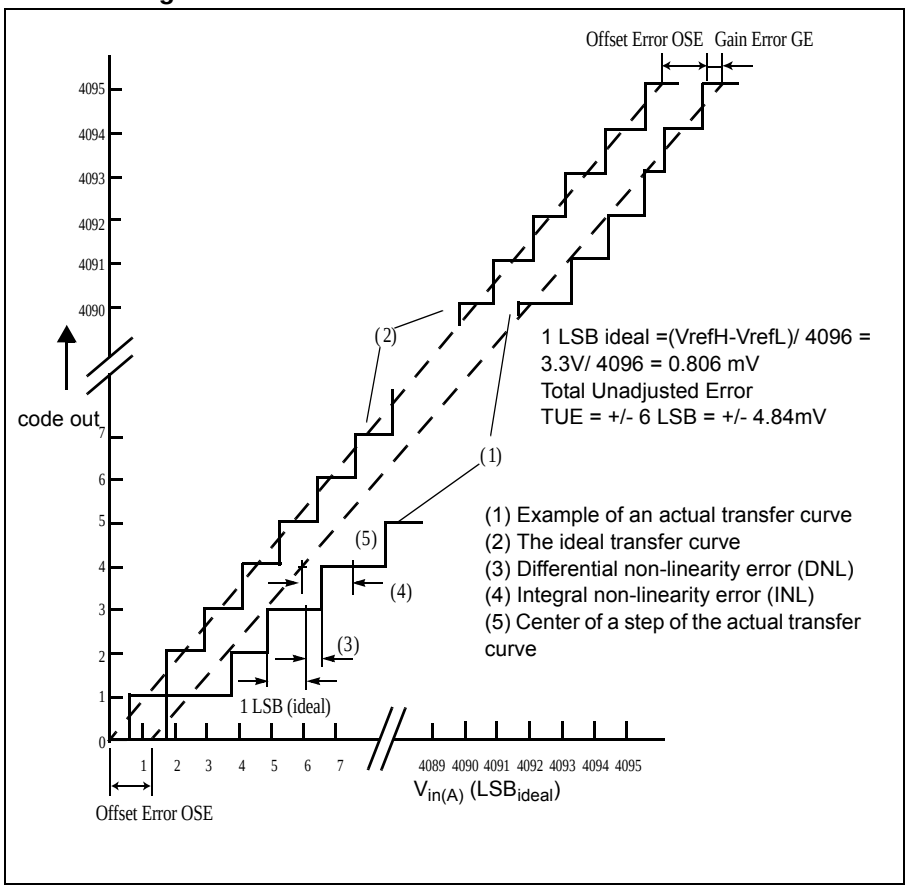
3.11 Supply current characteristics

Current consumption data is given in *Table 22*. These specifications are design targets and are subject to change per device characterization.

Table 22. Current consumption characteristics

Symbol		Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{DD\_LV\_FULL}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	50 mA+ 2.18 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	80 mA+ 2.50 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$(2)	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	26 + 2.10 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	41 mA+ 2.30 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies during LBIST (full LBIST configuration) T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	250	mA
			1.2 V supplies during LBIST (full LBIST configuration) T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	290	
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$(2)	P	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	279	mA
			T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	318	mA

Figure 9. ADC characteristics and error definitions



3.16.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the *Equation 4*:

2. Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for <100 program/erase cycles, nominal supply values and operation at 25°C. These values are verified at production test.
3. Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.
4. Program times are actual hardware programming times and do not include software overhead.

Table 29. Flash memory timing

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
T_{RES}	D	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns
T_{DONE}	D	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared	—	—	5	ns
T_{PSRT}	D	Time between program suspend resume and the next program suspend request.(1)	100	—	—	µs
T_{ESRT}	D	Time between erase suspend resume and the next erase suspend request.(2)	10			ms

1. Repeated suspends at a high frequency may result in the operation timing out, and the flash module will respond by completing the operation with a fail code (MCR[PEG] = 0), or the operation not able to finish (MCR[DONE] = 1 during Program operation). The minimum time between suspends to ensure this does not occur is T_{PSRT}.
2. If Erase suspend rate is less than T_{ESRT}, an increase of slope voltage ramp occurs during erase pulse. This improves erase time but reduces cycling figure due to overstress.

Table 30. Flash memory module life

No.	Symbol		Parameter	Value			Unit
				Minimum	Typical	Maximum	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range(1)	100000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range(1)	1000	100000 (2)	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature(3) Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

1. Operating temperature range is T_J from –40 °C to 150 °C. Typical endurance is evaluated at 25 °C.
2. Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks.
3. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.18 SWG electrical characteristics

Table 31. SPC56XL60/54 SWG Specifications

Symbol	Parameter	Value		
		Minimum	Typical	Maximum
T	Input clock	12 MHz	16 MHz	20 MHz
T	Frequency Range	1 kHz	—	50 kHz
T	Peak to Peak(1)	0.4 V	—	2.0V
T	Peak to Peak variation(2)	-6%	—	6%
T	Common Mode(3)	—	1.3 V	—
T	Common Mode variation	-6%	—	6%
T	SiNAD(4)	45 dB	—	—
T	Load C	25 pF	—	100 pF
T	Load I	0 µA	—	100 µA
T	ESD Pad Resistance(5)	230 Ω	—	360 Ω

1. Peak to Peak value is measured with no R or I load.
2. Peak to Peak excludes noise, SiNAD must be considered.
3. Common mode value is measured with no R or I load.
4. SiNAD is measured at Max Peak to Peak voltage.
5. Internal device routing resistance. ESD pad resistance is in series and must be considered for max Peak to Peak voltages, depending on application I load and/or R load.

3.19 AC specifications

3.19.1 Pad AC specifications

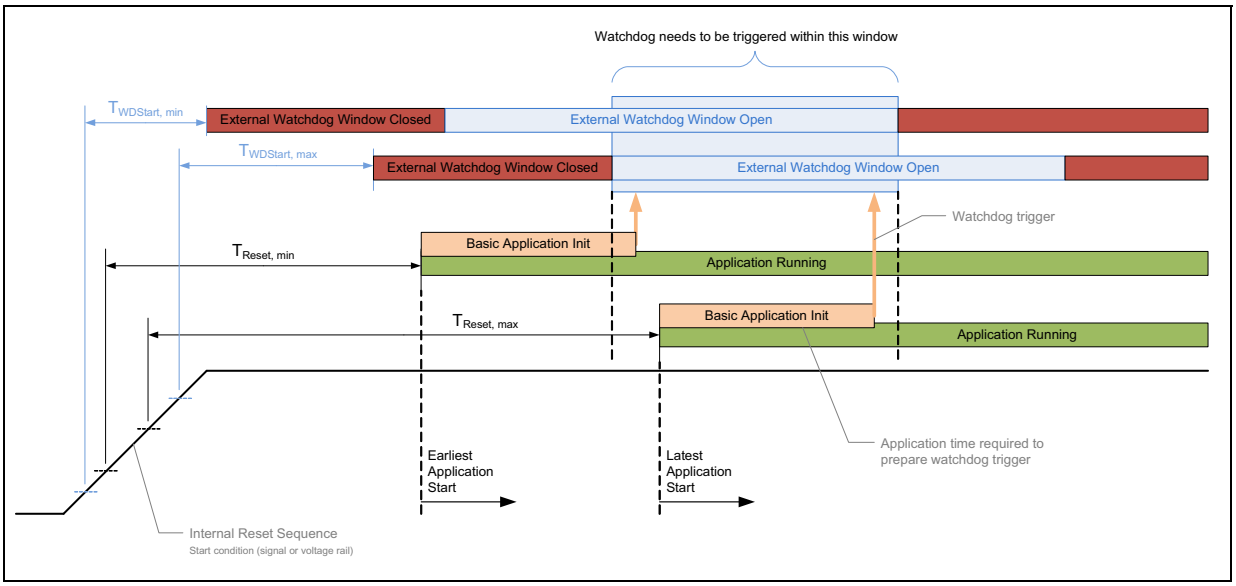
Table 32. Pad AC specifications (3.3 V, IPP_HVE = 0)(1)

No.	Pad		Tswitchon(1)(ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200

3.20.5 External watchdog window

If the application design requires the use of an external watchdog the data provided in *Section 3.20* can be used to determine the correct positioning of the trigger window for the external watchdog. *Figure 21* shows the relationships between the minimum and the maximum duration of a given reset sequence and the position of an external watchdog trigger window.

Figure 21. Reset sequence - External watchdog trigger window position



3.21 AC timing characteristics

AC Test Timing Conditions: Unless otherwise noted, all test conditions are as follows:

- TJ = –40 to 150 °C
- Supply voltages as specified in *Table 10*
- Input conditions: All Inputs: tr, tf = 1 ns
- Output Loading: All Outputs: 50 pF

3.21.1 $\overline{\text{RESET}}$ pin characteristics

The SPC56ELx/SPC564Lx implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 29. Nexus Double Data Rate (DDR) Mode output timing

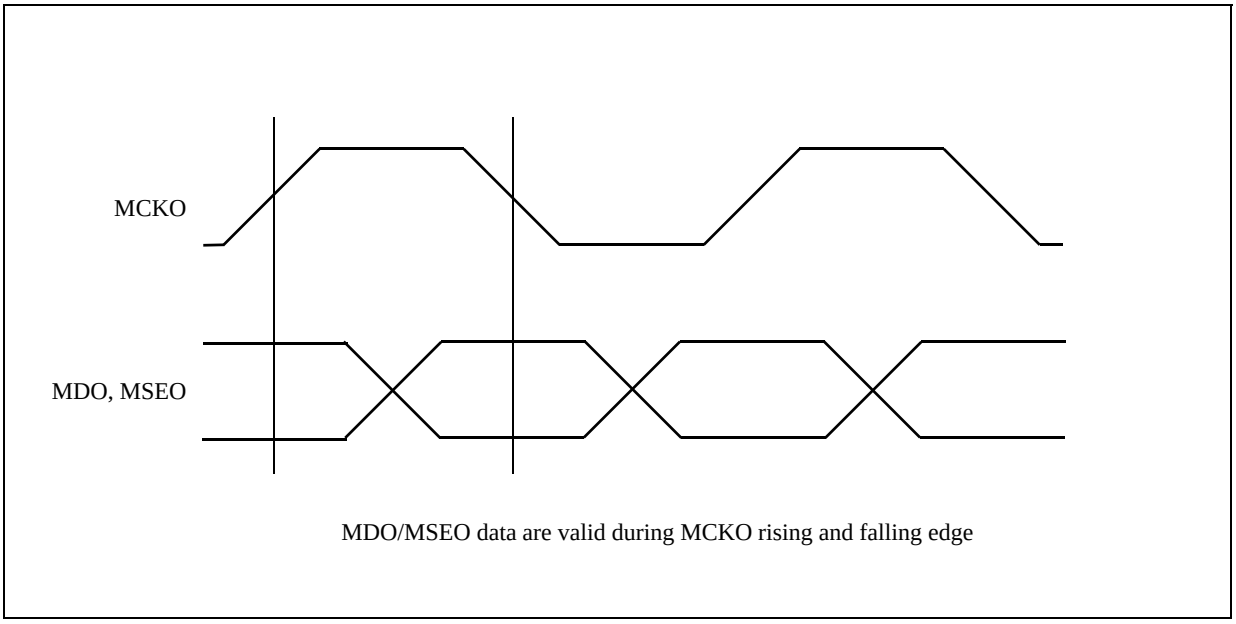
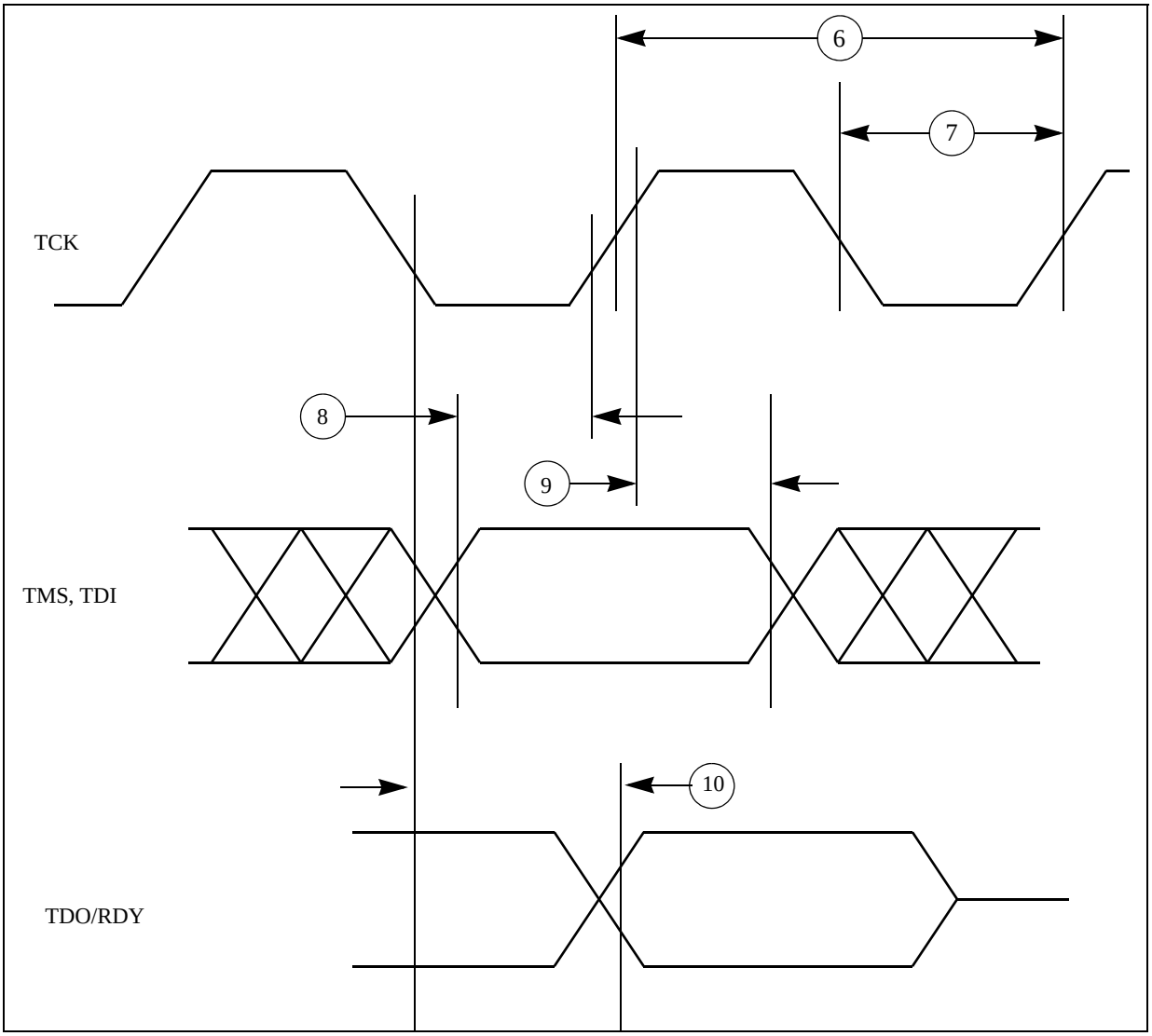


Figure 30. Nexus TDI, TMS, TDO timing



3.21.5 External interrupt timing (IRQ pin)

Table 40. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time(1)	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Table 43. LQFP144 mechanical data (continued)

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
E3	17.5			0.6890		
e	0.5			0.0197		
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
k	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
Tolerance	mm			inches		
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 43. LFBGA257 package mechanical drawing

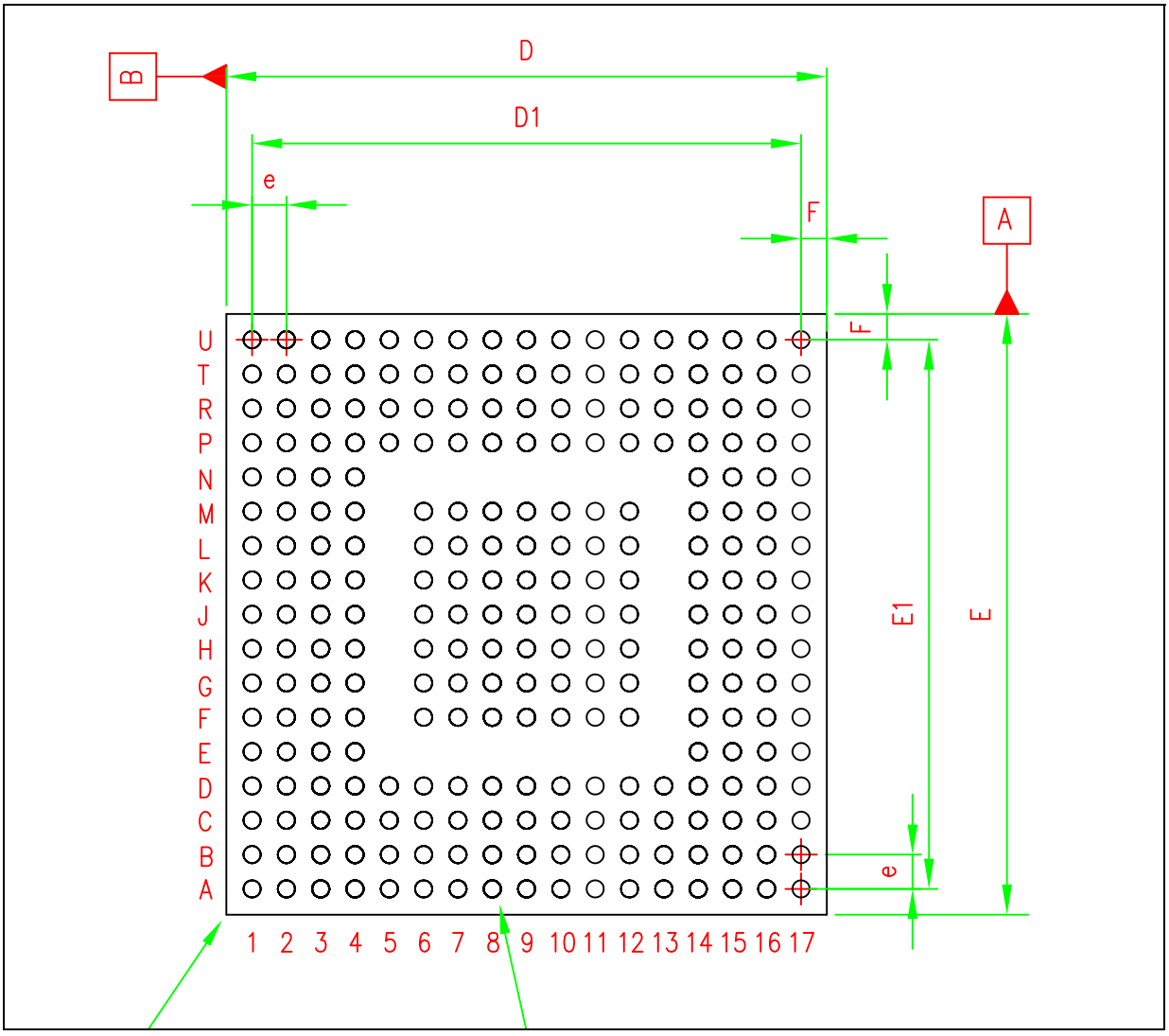


Table 45. Document revision history

Date	Revision	Changes
23-Nov-2010	5 (continued)	In the “BCP68 board schematic example” figure, removed the resistor at the base of the BCP68 transistor. In the “DC electrical characteristics” table: – Changed the guarantee parameter for I_{INJ} (was P, is T). – Added a specification for input leakage current for shared ADC input-only ports. Revised the “Flash memory module life” table. In the “FMPLL electrical characteristics” table, revised the footnote defining f_{SCM} and f_{VCO}. In the “Main oscillator electrical characteristics” table: – Changed the max specification for $g_{mXOSCHS}$ (was 11.8 mA/V, is 13.25 mA/V). – Revised the conditions for $T_{XOSCHSSU}$. In the ‘RC oscillator electrical characteristics” table, deleted the specification for $\Delta_{RCMTRIM}$. Revised the “ADC conversion characteristics” table. In the “$\overline{\text{RESET}}$ pin characteristics” section, changed “n$\overline{\text{RSTIN}}$” to “$\overline{\text{RESET}}$”. Added the “Reset sequence” section. Revised the footnotes in the “Nexus debug port timing” table. Added the mechanical drawing for the 100-pin package. In the “Order codes” table, added a footnote about frequency modulation to the “Speed (MHz)” column heading.
23-Mar-2011	6	Editorial changes. In the “Document overview” section, added information about how content specific to silicon versions (“cut1” and “cut2”) is presented. In the isometric miniature package drawings on the front page, removed the third dimension. Changed Symbol from P to D for “Conversion Time” in “ADC conversion characteristics” table. Added classification symbol “D” to seven entries in “Voltage regulator electrical specifications“ table. Removed irrelevant FlexCAN specs. Updated Table “Voltage Thresholds” to reference values specified in Table “Voltage Regulator Electrical Specifications”. RDY pin added for cut2. In the “System pins” table, added a footnote about the MDO0 pad speed. Updated Rsw1 values. Added TUE-related spec information for single and double ADC channels. Added AC Test Timing Conditions to the “AC timing characteristics” section. Added a statement on the first page describing cut1 versus cut2. Moved the first paragraph from the “Description” section to the beginning of the “Document overview” section. Changed pad speed from “M” to “SYM” for FlexRay pins in the “Pin Muxing” table and added this pad type to the footnote. Moved the newly added device current specification entries from the “DC electrical characteristics“ table into a newly created “Supply current characteristics“ table.

Table 45. Document revision history

Date	Revision	Changes
23-Mar-2011	6 (continued)	In the “Supply current characteristics (cut2)“ table: – Changed “$I_{DD\_LV\_MAX}$” to “$I_{DD\_LV\_MAX}$“; – Removed all “40-120 MHz” frequency ranges from the “Conditions” column; – Updated the “Max” values column; – Added parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ with “P” classification and special footnote; – Changed all “25°C“ temperature conditions to “ambient”; – Added “T_J = 150 °C“ condition to parameters $I_{DD\_HV\_ADC}$, $I_{DD\_HV\_AREF}$, $I_{DD\_HV\_OSC}$, and $I_{DD\_HV\_FLASH}$. Changed the timing diagram in the “Main oscillator electrical characteristics” section to reference MTRANS assertion instead of V_{DDMIN}. Updated the jitter specs in the “FMPLL electrical characteristics“ table. In the “ADC conversion characteristics“ table, changed all parameters with units of “counts” to units of “LSB” and updated Min/Max values. Changed $I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$ operating current (for both cases) to TBD. In the “Supply current characteristics (cut2)” section, added a footnote that $I_{DD\_HV\_ADC}$ and $I_{DD\_HV\_AREF}$ represent the total current of both ADCs in the “Current consumption characteristics” table. In the “ADC conversion characteristics” table: – Changed DNL min from -2 to -1. – Changed OFS min from -2 to -6. – Changed OFS max from 2 to 6. – Changed GNE min from -2 to -6. – Changed GNE max from 2 to 6. – Changed SNR min from 69 to 67. – Changed TUE min (without current injection) from -6 to -8. – Changed TUE max (without current injection) from 6 to 8. – Changed TUE min (with current injection) from -8 to -10. Changed TUE max (with current injection) from 8 to 10.