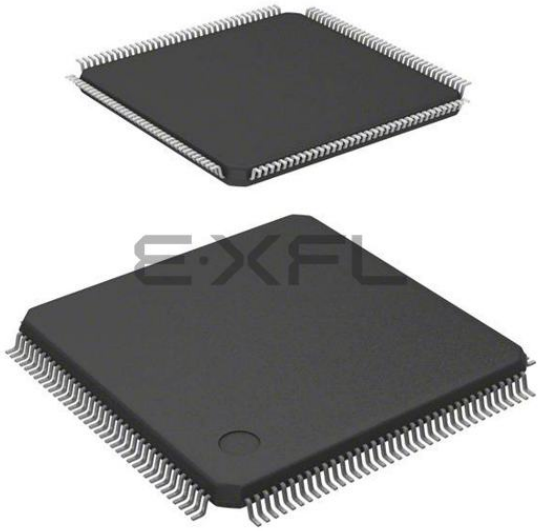

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l5cbosy

1.5 Feature details

1.5.1 High-performance e200z4d core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs

1.5.25 System Status and Configuration Module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification

- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO
- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
68	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
69	BCTRL	—		
70	$V_{DD\_LV\_COR}$	—		
71	$V_{SS\_LV\_COR}$	—		
72	$V_{DD\_HV\_PMU}$	—		
73	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
74	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
75	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
76	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
77	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]
78	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
79	G[9]	SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
		DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
80	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
81	G[8]	SIUL	GPIO[104]	GPIO[104]
		FlexRay	DBG0	—
		DSPI_0	CS1	—
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[21]
82	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
83	G[7]	SIUL	GPIO[103]	GPIO[103]
		FlexPWM_0	B[3]	B[3]
84	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
85	G[5]	SIUL	GPIO[101]	GPIO[101]
		FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
86	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
87	TMS	—		
88	TCK	—		
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS\_HV\_IO}$	—		
91	$V_{DD\_HV\_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD\_LV\_COR}$	—		
94	$V_{SS\_LV\_COR}$	—		

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD\_HV\_IO}$	—		
127	$V_{SS\_HV\_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD\_HV\_REG\_2}$	—		
131	$V_{DD\_LV\_COR}$	—		
132	$V_{SS\_LV\_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD\_LV\_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS\_LV\_COR}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
L16	H[4]	SIUL	GPIO[116]	GPIO[116]
		FlexPWM_1	X[0]	X[0]
		eTimer_2	ETC[0]	ETC[0]
L17	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
M1	$V_{DD\_HV\_OSC}$	—		
M2	$V_{DD\_HV\_IO\_RING}$	—		
M3	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
M4	Not connected	—		
M6	V_{DD_LV}	—		
M7	V_{DD_LV}	—		
M8	V_{DD_LV}	—		
M9	V_{DD_LV}	—		
M10	V_{DD_LV}	—		
M11	V_{DD_LV}	—		
M12	V_{DD_LV}	—		
M14	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
M15	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
M16	TMS	—		
M17	H[5]	SIUL	GPIO[117]	GPIO[117]
		FlexPWM_1	A[0]	A[0]
		DSPI_0	CS4	—
N1	XTAL	—		
N2	$V_{SS\_HV\_IO\_RING}$	—		
N3	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
N4	$V_{SS\_LV\_PLL0\_PLL1}$	—		

Table 8. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
Port A												
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	—	M	S	51	73	T14
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0						
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0						
		SIUL	—	—	EIRQ[0]	—						
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	—	M	S	52	74	R14
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0						
		DSPI_2	SOUT	ALT2	—	—						
		SIUL	—	—	EIRQ[1]	—						
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S	57	84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[3]	PCR[3]	SIUL	GPIO[3]	ALT0	GPIO[3]	—	Pull down	M	S	64	92	K17
		eTimer_0	ETC[3]	ALT1	ETC[3]	PSMI[38]; PADSEL=0						
		DSPI_2	CS0	ALT2	CS0	PSMI[3]; PADSEL=0						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=0						
		MC_RGM	—	—	ABS[2]	—						
		SIUL	—	—	EIRQ[3]	—						
A[4]	PCR[4]	SIUL	GPIO[4]	ALT0	GPIO[4]	—	Pull down	M	S	75	108	C16
		eTimer_1	ETC[0]	ALT1	ETC[0]	PSMI[9]; PADSEL=0						
		DSPI_2	CS1	ALT2	—	—						
		eTimer_0	ETC[4]	ALT3	ETC[4]	PSMI[7]; PADSEL=0						
		MC_RGM	—	—	FAB	—						
		SIUL	—	—	EIRQ[4]	—						
A[5]	PCR[5]	SIUL	GPIO[5]	ALT0	GPIO[5]	—	—	M	S	8	14	H4
		DSPI_1	CS0	ALT1	CS0	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=0						
		DSPI_0	CS7	ALT3	—	—						
		SIUL	—	—	EIRQ[5]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[14]	PCR[14]	SIUL	GPIO[14]	ALT0	GPIO[14]	—	—	M	S	99	143	B4
		FlexCAN_1	TXD	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=0						
		SIUL	—	—	EIRQ[13]	—						
A[15]	PCR[15]	SIUL	GPIO[15]	ALT0	GPIO[15]	—	—	M	S	100	144	D3
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=0						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=0						
		SIUL	—	—	EIRQ[14]	—						
Port B												
B[0]	PCR[16]	SIUL	GPIO[16]	ALT0	GPIO[16]	—	—	M	S	76	109	B15
		FlexCAN_0	TXD	ALT1	—	—						
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=0						
		SSCM	DEBUG[0]	ALT3	—	—						
		SIUL	—	—	EIRQ[15]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[4]	PCR[36]	SIUL	GPIO[36]	ALT0	GPIO[36]	—	—	M	S	5	11	H3
		DSPI_0	CS0	ALT1	CS0	—						
		FlexPWM_0	X[1]	ALT2	X[1]	PSMI[28]; PADSEL=0						
		SSCM	DEBUG[4]	ALT3	—	—						
		SIUL	—	—	EIRQ[22]	—						
C[5]	PCR[37]	SIUL	GPIO[37]	ALT0	GPIO[37]	—	—	M	S	7	13	G3
		DSPI_0	SCK	ALT1	SCK	—						
		SSCM	DEBUG[5]	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=0						
		SIUL	—	—	EIRQ[23]	—						
C[6]	PCR[38]	SIUL	GPIO[38]	ALT0	GPIO[38]	—	—	M	S	98	142	D4
		DSPI_0	SOUT	ALT1	—	—						
		FlexPWM_0	B[1]	ALT2	B[1]	PSMI[25]; PADSEL=0						
		SSCM	DEBUG[6]	ALT3	—	—						
		SIUL	—	—	EIRQ[24]	—						
C[7]	PCR[39]	SIUL	GPIO[39]	ALT0	GPIO[39]	—	—	M	S	9	15	K4
		FlexPWM_0	A[1]	ALT2	A[1]	PSMI[21]; PADSEL=0						
		SSCM	DEBUG[7]	ALT3	—	—						
		DSPI_0	—	—	SIN	—						

Table 10. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_AD0}$ $V_{SS\_HV\_AD1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD\_LV\_REGCOR}$(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(5)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_PLL}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	$f_{CPU} \leq 120$ MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. $V_{DD\_HV\_ADR0}$ and $V_{DD\_HV\_ADR1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.
3. $V_{DD\_HV\_ADRx}$ must always be applied and should be stable before LBIST starts. If this supply is not above its absolute minimum level, LBIST operations can fail.
4. Can be connected to emitter of external NPN. Low voltage supplies are not under user control. They are produced by an on-chip voltage regulator.
5. For the device to function properly, the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter, if one is used.

3.4 Decoupling capacitors

The internal voltage regulator requires an external NPN ballast and some additional decoupling capacitors. These capacitors shall be placed on the board as close as possible to the associated pin.

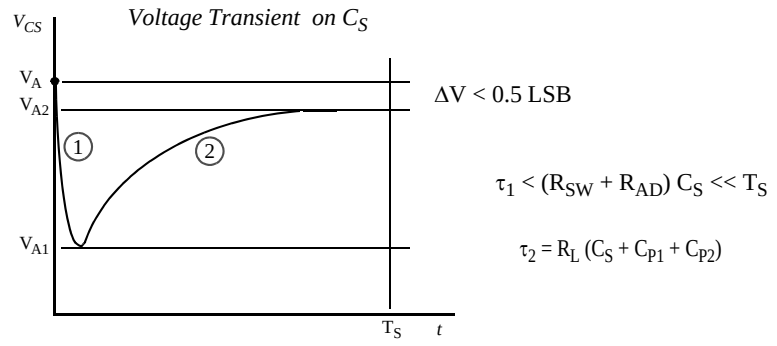
Table 11. Decoupling capacitors

Symbol		Parameter	Conditions(1)	Value			Unit
				Min	Typ	Max	
C_{COL}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Max ESR = 100 mΩ.		20		µF
C_{LV1}	SR	External decoupling / stability capacitor	Sum of C_{LV1} placed close to $V_{DD}/V_{SS\_LV\_CORy}$ pairs(2).	12µF		40µF	µF
C_{LV2}	SR	External decoupling / stability capacitor	Sum of C_{LV2} placed close to $V_{DD}/V_{SS\_LV\_CORy}$ pairs shall be between 300 nF and 900 nF.		100(2)		nF

Table 22. Current consumption characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$[2]	T	Operating current	1.2V supplies Tj=105°C $V_{DD\_LV\_COR}$ = 1.2V LSM mode	—	—	275	mA
			1.2V supplies Tj=125°C $V_{DD\_LV\_COR}$ = 1.2V LSM mode	—	—	299	mA
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$[2]	T	Operating current	1.2V supplies Tj=105°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	189	mA
			1.2V supplies Tj=125°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	214	mA
			1.2V supplies Tj=150°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	235	mA
$I_{DD\_LV\_STOP}$	T	Operating current in V_{DD} STOP mode	T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	20	mA
	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	57	
	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	105	
$I_{DD\_LV\_HALT}$	T	Operating current in V_{DD} HALT mode	T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	25	mA
	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	64	
	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	115	
$I_{DD\_HV\_ADC}$[3], [4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_ADC}$ = 3.6 V	—	—	10	mA

Figure 11. Transient Behavior during Sampling Phase



In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

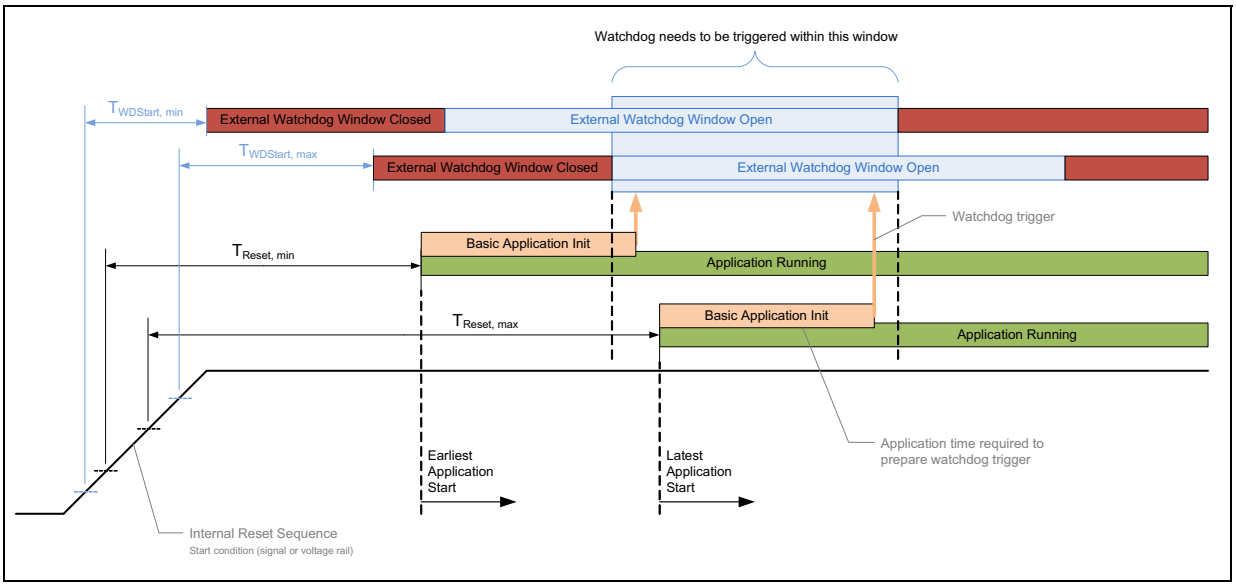
$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2}

3.20.5 External watchdog window

If the application design requires the use of an external watchdog the data provided in *Section 3.20* can be used to determine the correct positioning of the trigger window for the external watchdog. *Figure 21* shows the relationships between the minimum and the maximum duration of a given reset sequence and the position of an external watchdog trigger window.

Figure 21. Reset sequence - External watchdog trigger window position



3.21 AC timing characteristics

AC Test Timing Conditions: Unless otherwise noted, all test conditions are as follows:

- TJ = –40 to 150 °C
- Supply voltages as specified in *Table 10*
- Input conditions: All Inputs: tr, tf = 1 ns
- Output Loading: All Outputs: 50 pF

3.21.1 $\overline{\text{RESET}}$ pin characteristics

The SPC56ELx/SPC564Lx implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 22. Start-up reset requirements

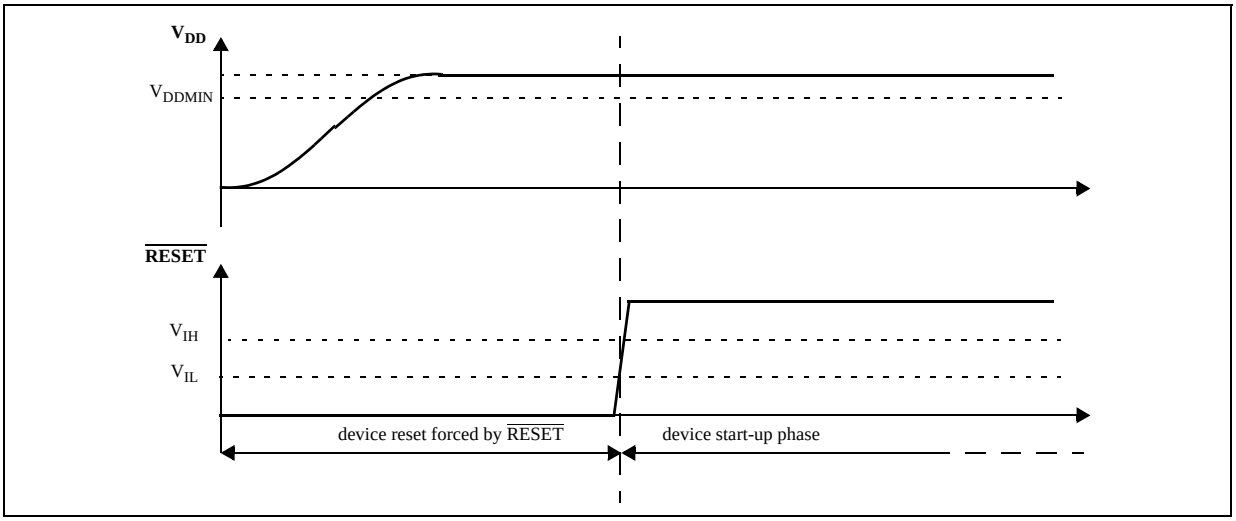


Figure 23. Noise filtering on reset signal

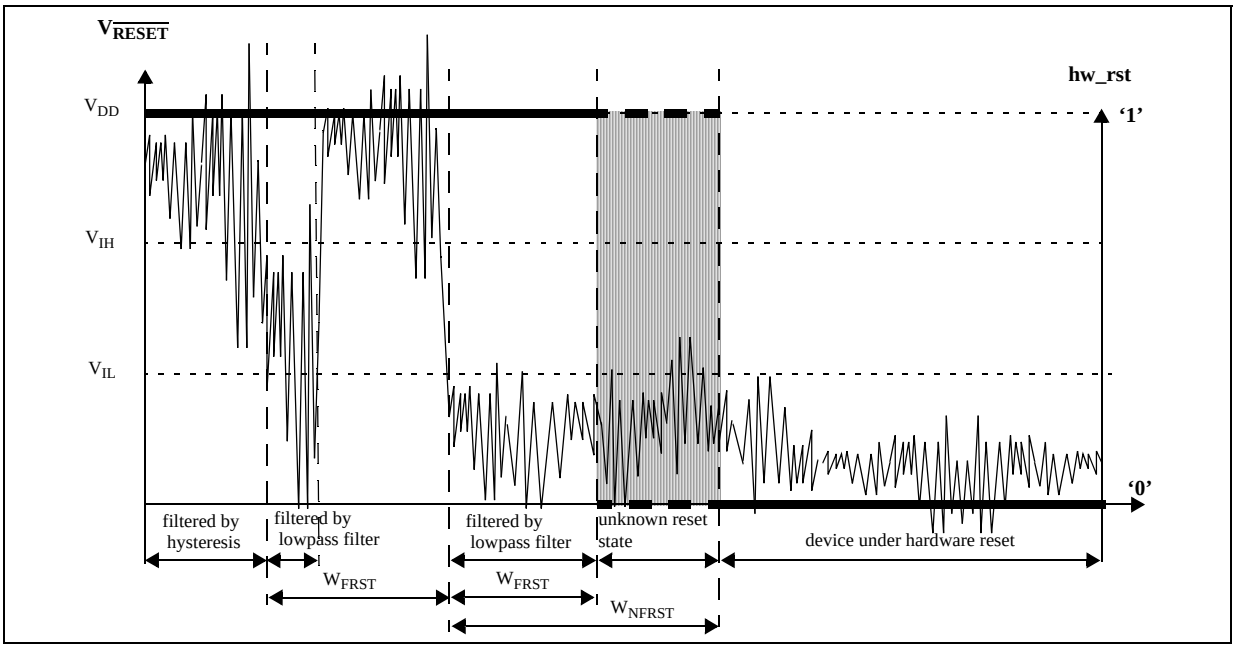
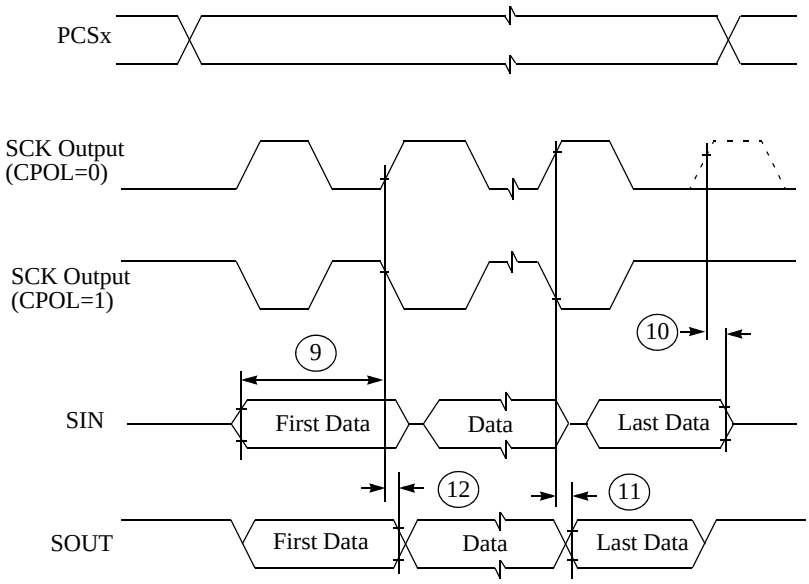


Table 36. RESET electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	nRESET input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	nRESET input not filtered pulse	—	500	—	—	ns

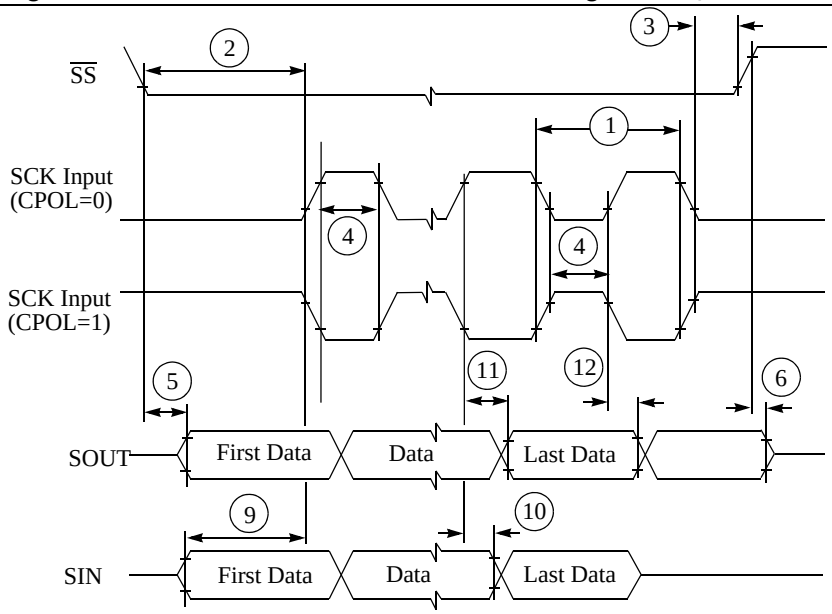
1. V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified.

Figure 37. DSPI modified transfer format timing — master, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 38. DSPI modified transfer format timing – slave, CPHA = 0



Note: The numbers shown are referenced in *Table 41*.

5 Ordering information

Figure 44. Commercial product code structure

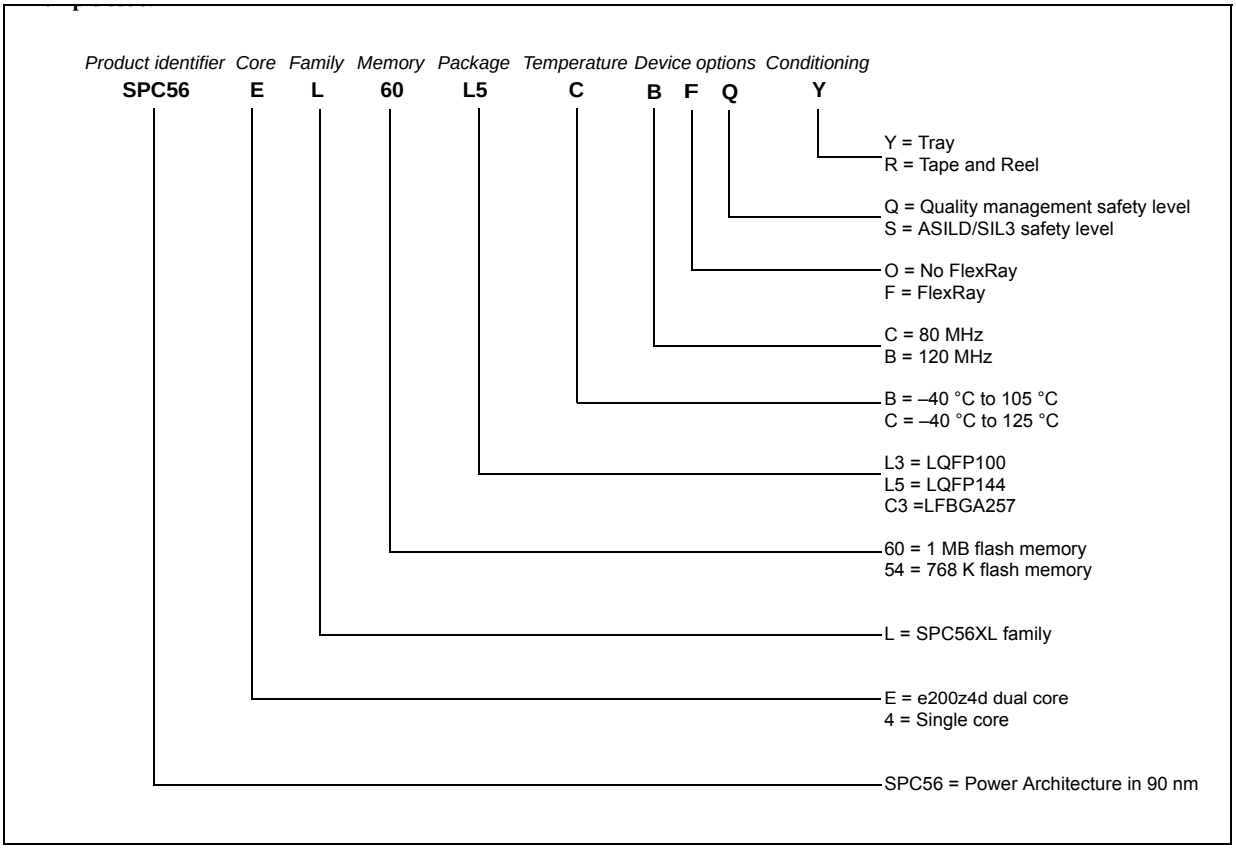


Table 45. Document revision history

Date	Revision	Changes
23-Nov-2010	5 (continued)	In the “BCP68 board schematic example” figure, removed the resistor at the base of the BCP68 transistor. In the “DC electrical characteristics” table: – Changed the guarantee parameter for I_{INJ} (was P, is T). – Added a specification for input leakage current for shared ADC input-only ports. Revised the “Flash memory module life” table. In the “FMPLL electrical characteristics” table, revised the footnote defining f_{SCM} and f_{VCO}. In the “Main oscillator electrical characteristics” table: – Changed the max specification for $g_{mXOSCHS}$ (was 11.8 mA/V, is 13.25 mA/V). – Revised the conditions for $T_{XOSCHSSU}$. In the ‘RC oscillator electrical characteristics” table, deleted the specification for $\Delta_{RCMTRIM}$. Revised the “ADC conversion characteristics” table. In the “$\overline{\text{RESET}}$ pin characteristics” section, changed “n$\overline{\text{RSTIN}}$” to “$\overline{\text{RESET}}$”. Added the “Reset sequence” section. Revised the footnotes in the “Nexus debug port timing” table. Added the mechanical drawing for the 100-pin package. In the “Order codes” table, added a footnote about frequency modulation to the “Speed (MHz)” column heading.
23-Mar-2011	6	Editorial changes. In the “Document overview” section, added information about how content specific to silicon versions (“cut1” and “cut2”) is presented. In the isometric miniature package drawings on the front page, removed the third dimension. Changed Symbol from P to D for “Conversion Time” in “ADC conversion characteristics” table. Added classification symbol “D” to seven entries in “Voltage regulator electrical specifications“ table. Removed irrelevant FlexCAN specs. Updated Table “Voltage Thresholds” to reference values specified in Table “Voltage Regulator Electrical Specifications”. RDY pin added for cut2. In the “System pins” table, added a footnote about the MDO0 pad speed. Updated Rsw1 values. Added TUE-related spec information for single and double ADC channels. Added AC Test Timing Conditions to the “AC timing characteristics” section. Added a statement on the first page describing cut1 versus cut2. Moved the first paragraph from the “Description” section to the beginning of the “Document overview” section. Changed pad speed from “M” to “SYM” for FlexRay pins in the “Pin Muxing” table and added this pad type to the footnote. Moved the newly added device current specification entries from the “DC electrical characteristics“ table into a newly created “Supply current characteristics“ table.

Table 45. Document revision history

Date	Revision	Changes
01-Aug-2012	8 (cont.)	– In *Table 20: Voltage regulator electrical specifications*, changed the “Digital supply high voltage detector upper threshold low limit (After a destructive reset initialization phase completion)” from 1.43V to 1.38V. – Added *Table 20: Voltage regulator electrical specifications*. – Updated the IDD values in *Table 22: Current consumption characteristics*. Changed conditions text from “1.2 supplies during LBIST (full LBIST configuration)” to “1.2 V supplies” for all the IDD parameters except $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. Added footnote in “Conditions” for the DPM mode. – Removed Cut references from the whole document. In *Table 27: ADC conversion characteristics*, changed the sampling frequency value from ‘1 MHz’ to ‘983.6 KHz’.
31-Jul-2013	9	– Updated *Table 20: Voltage regulator electrical specifications* (Voltage regulator electrical specifications) – Added Digital supply low voltage detector lower threshold and Digital supply low voltage detector upper threshold – Updated Main High Voltage Power-Low Voltage Detection value to 2.93 V – Replaced IEC with ISO26262 in *Section 1.1: Document overview*, – *Table 1* (SPC56XL60/54 device summary)-removed KGD – *Table 26* (16 MHz RC oscillator electrical characteristics) modified fRC values – Updated*Table 28* (Flash memory program and erase electrical specifications) – Updated *Table 27* (ADC conversion characteristics)-tconv to teval and associated footnote – Updated *Table 21* (DC electrical characteristics) – added VIH footnote – Updated IOL, IOH value for Fast pads – Updated *Table 33* (RESET sequences)-TDRB and TELRB – Updated *Table 20* (Voltage regulator electrical specifications)-combined ESR of external capacitor values – Updated *Section 3.16.1: Input Impedance and ADC Accuracy* -replaced fc by fs – *Table 7* (System pins)s-added footnote to RESET pin about weak pull down – Updated Injection current information in *Table 21* (DC electrical characteristics)-IINJ, *Table 9* (Absolute maximum ratings)-footnote 4 – Updated *Table 22* (Current consumption characteristics) for the following: – specified oscillator bypass mode and crystal oscillator mode – Updated STOP and HALT mode values – Added IDD_HV_PMU – footnote 2, footnote 3 – Added footnote $V_{DD\_HV\_ADRx}$ must always be applied and should be stable before LBIST starts. to *Table 10* (Recommended operating conditions (3.3 V)). – Added footnote to *Section 5: Ordering information* – Edit changes to *Section 3.6: Electromagnetic Interference (EMI) characteristics* – Updated *Equation 11*.