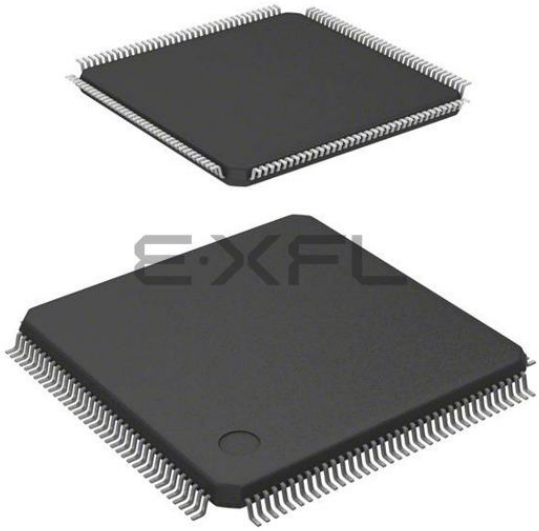

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el60l5ccosr

Table 1. SPC56ELx/SPC564Lx device summary (continued)

Feature		SPC56EL60	SPC56EL54
Modules	Interrupt Controller (INTC)	16 interrupt levels, replicated module	
	Periodic Interrupt Timer (PIT)	1 × 4 channels	
	System Timer Module (STM)	1 × 4 channels, replicated module	
	Software Watchdog Timer (SWT)	Yes, replicated module	
	eDMA	16 channels, replicated module	
	FlexRay	1 × 64 message buffers, dual channel	
	FlexCAN	2 × 32 message buffers	
	LINFlexD (UART and LIN with DMA support)	2	
	Clock out	Yes	
	Fault Collection and Control Unit (FCCU)	Yes	
	Cross Triggering Unit (CTU)	Yes	
	eTimer	3 × 6 channels(1)	
	FlexPWM	2 Module 4 × (2 + 1) channels(2)	
	Analog-to-Digital Converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)	
	Sine Wave Generator (SWG)	32 point	
Modules (cont.)	Deserial Serial Peripheral Interface (DSPI)	3 × DSPI as many as 8 chip selects	
	Cyclic Redundancy Checker (CRC) unit	Yes	
	Junction temperature sensor (TSENS)	Yes, replicated module	
	Digital I/Os	≥ 16	
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die	
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V	
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4 – 40 MHz	
Debug	Nexus	Level 3+	
Packages	LQFP	100 pins 144 pins	
	LBGA(3)	LBGA257	

Table 1. SPC56ELx/SPC564Lx device summary (continued)

Feature		SPC56EL60	SPC56EL54
Temperature	Temperature range (junction)	–40 to 150 °C	
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C	

1. The third eTimer (eTimer_2) is available with external I/O access only in the BGA package, on the LQFP package eTimer_2 is available internally only without any external I/O access.
2. The second FlexPWM module is available only in the BGA package.
3. LBGA257 available only as development package.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56ELx/SPC564Lx device.

- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as 8 chip select lines available, depending on package and pin multiplexing
- 4 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.30 FlexPWM

The pulse width modulator module (FlexPWM) contains four PWM channels, each of which is configured to control a single half-bridge power stage. Two modules are included on LFBGA257 devices; on the LQFP144 package, only one module is present. Additionally, four fault input channels are provided per FlexPWM module.

This PWM is capable of controlling most motor types, including:

- AC induction motors (ACIM)
- Permanent Magnet AC motors (PMAC)
- Brushless (BLDC) and brush DC motors (BDC)
- Switched (SRM) and variable reluctance motors (VRM)
- Stepper motors

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via secondary FMPLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
48	$V_{DD\_LV\_COR}$	—		
49	$V_{SS\_LV\_COR}$	—		
50	$V_{DD\_HV\_PMU}$	—		
51	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
52	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
53	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
54	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
55	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
56	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
57	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
58	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
59	TMS	—		
60	TCK	—		
61	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
83	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
84	JCOMP	—	—	JCOMP
85	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
86	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
87	$V_{DD\_HV\_IO}$	—		
88	$V_{SS\_HV\_IO}$	—		
89	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
90	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
91	$V_{DD\_HV\_REG\_2}$	—		
92	$V_{DD\_LV\_COR}$	—		
93	$V_{SS\_LV\_COR}$	—		
94	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD\_HV\_REG\_0}$	—		
17	$V_{SS\_LV\_COR}$	—		
18	$V_{DD\_LV\_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	MSEO[1]	—
21	$V_{DD\_HV\_IO}$	—		
22	$V_{SS\_HV\_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	MSEO[0]	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	EVTO	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	EVTI
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD\_HV\_OSC}$	—		
28	$V_{SS\_HV\_OSC}$	—		
29	XTAL	—		
30	EXTAL	—		
31	RESET	—		
32	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
33	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
34	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
35	$V_{SS\_LV\_PLL0\_PLL1}$	—		
36	$V_{DD\_LV\_PLL0\_PLL1}$	—		
37	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	analog output	—
38	FCCU_F[0]	FCCU	F[0]	F[0]
39	$V_{DD\_LV\_COR}$	—		
40	$V_{SS\_LV\_COR}$	—		
41	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
42	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
43	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
44	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
45	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
46	E[6]	SIUL	—	GPIO[70]
		ADC_0	—	AN[4]
47	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
48	E[7]	SIUL	—	GPIO[71]
		ADC_0	—	AN[6]
49	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
50	$V_{DD\_HV\_ADR0}$	—		
51	$V_{SS\_HV\_ADR0}$	—		

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD\_HV\_IO}$	—		
127	$V_{SS\_HV\_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD\_HV\_REG\_2}$	—		
131	$V_{DD\_LV\_COR}$	—		
132	$V_{SS\_LV\_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD\_LV\_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS\_LV\_COR}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
B11	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]
B12	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
B13	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
B14	F[13]	SIUL	GPIO[93]	GPIO[93]
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[31]
B15	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
B16	$V_{DD\_HV\_IO\_RING}$	—		
B17	$V_{SS\_HV\_IO\_RING}$	—		
C1	$V_{DD\_HV\_IO\_RING}$	—		
C2	Not connected	—		
C3	$V_{SS\_HV\_IO\_RING}$	—		
C4	FCCU_F[1]	FCCU	F[1]	F[1]
C5	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
C6	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
C7	$V_{DD\_HV\_REG\_2}$	—		
C8	$V_{DD\_HV\_REG\_2}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C9	I[0]	SIUL	GPIO[128]	GPIO[128]
		eTimer_2	ETC[0]	ETC[0]
		DSPI_0	CS4	—
		FlexPWM_1	—	FAULT[0]
C10	JCOMP	—	—	JCOMP
C11	H[11]	SIUL	GPIO[123]	GPIO[123]
		FlexPWM_1	A[2]	A[2]
C12	I[1]	SIUL	GPIO[129]	GPIO[129]
		eTimer_2	ETC[1]	ETC[1]
		DSPI_0	CS5	—
		FlexPWM_1	—	FAULT[1]
C13	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
C14	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
C15	$V_{SS\_HV\_IO\_RING}$	—		
C16	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
C17	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
D1	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
D2	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—

Table 6. Supply pins (continued)

Supply		Pin #		
Symbol	Description	100 pkg	144 pkg	257 pkg
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132	VSS_LV(2)
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	135	VDD_LV(1)
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	137	VSS_LV(2)

1. VDD_LV balls are tied together on the LFBGA257 substrate.
2. VSS_LV balls are tied together on the LFBGA257 substrate.
3. VDD_HV balls are tied together on the LFBGA257 substrate.
4. VSS_HV balls are tied together on the LFBGA257 substrate.

2.3 System pins

Table 7. System pins

Symbol	Description	Direction	Pin #		
			100 pkg	144 pkg	257 pkg
Dedicated pins					
MDO0(1)	Nexus Message Data Output — line	Output only	—	9	E1
NMI(2)	Non Maskable Interrupt	Input only	1	1	E4
XTAL	Input for oscillator amplifier circuit and internal clock generator	Input only	18	29	N1
EXTAL(3)	Oscillator amplifier output	Input/Output (4)	19	30	R1
TMS(2)	JTAG state machine control	Input only	59	87	M16
TCK(2)	JTAG clock	Input only	60	88	L15
JCOMP(5)	JTAG compliance select	Input only	84	123	C10
Reset pin					
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength. Output drive is open drain and must be terminated by an external resistor of value 1KOhm.(6)	Bidirectional	20	31	P2
Test pin					
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.		74	107	D15

1. This pad is configured for Fast (F) pad speed.

Table 8. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
Port A												
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	—	M	S	51	73	T14
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0						
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0						
		SIUL	—	—	EIRQ[0]	—						
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	—	M	S	52	74	R14
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0						
		DSPI_2	SOUT	ALT2	—	—						
		SIUL	—	—	EIRQ[1]	—						
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S	57	84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$= junction to case thermal resistance (°C/W)

$R_{\theta CA}$= case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T= thermocouple temperature on top of the package (°C)

Ψ_{JT}= thermal characterization parameter (°C/W)

P_D= power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.5.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB on JEDEC site.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

SPC56XL60/54 makes a transition from HPREG1 to HPREG2. This transition is dynamic. Once HPREG2 is fully operational, the controller part of HPREG1 is switched off.

The following bipolar transistors are supported:

- BCP68 from ON Semiconductor
- BCX68 from Infineon

Table 19. Characteristics

Symbol	Parameter	Value	Unit
$h_{FE}(\beta)$	DC current gain (Beta)	85 - 375	—
P_D	Maximum power dissipation @ T_A=25°C(1)	1.5	W
I_{CMaxDC}	Maximum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage (Max)	600(2)	mV
V_{BE}	Base-to-emitter voltage (Max)	1.0	V

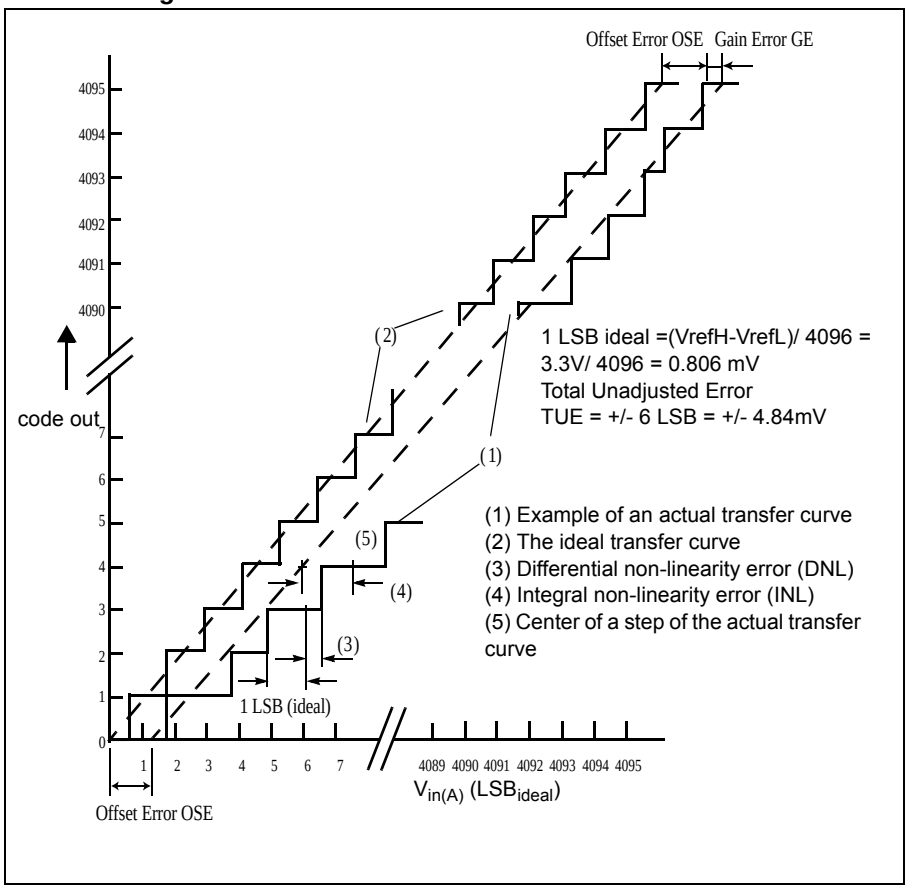
1. Derating factor 12mW/degC.
2. Adjust resistor at bipolar transistor collector for 3.3V to avoid VCE<VCE_{SAT}.

The recommended external ballast transistor is the bipolar transistor BCP68 with the gain range of 85 up to 375 (for IC=500mA, VCE=1V) provided by several suppliers. This includes the gain variations BCP68-10, BCP68-16 and BCP68-25.The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter. SPC56XL60/54 Voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

Table 20. Voltage regulator electrical specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
C_{ext}		External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
	SR	Combined ESR of external capacitor	—	1	—	100	mΩ
	SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	300	—	900	nF
t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms

Figure 9. ADC characteristics and error definitions



3.16.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the *Equation 4*:

Table 34. Reset sequence trigger — reset sequence (continued)

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive Reset Sequence, BIST enabled(1)	***Destructive Reset Sequence, BIST disabled***(1)	***External Reset Sequence Long, BIST enabled***	***Functional Reset Sequence Long***	***Functional Reset Sequence Short***
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$(7)	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1. Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.
2. End of the internal reset sequence (as specified in *Table 33*) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till $\overline{\text{RESET}}$ is released externally.
3. The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).
4. If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is enabled via chip configuration data stored in the shadow sector of the NVM.
5. If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is disabled via chip configuration data stored in the shadow sector of the NVM.
6. If $\overline{\text{RESET}}$ is configured for short reset
7. Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.20.4 Reset sequence — start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence becomes important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.20.4.1 Destructive reset

Figure 19 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*.

Figure 22. Start-up reset requirements

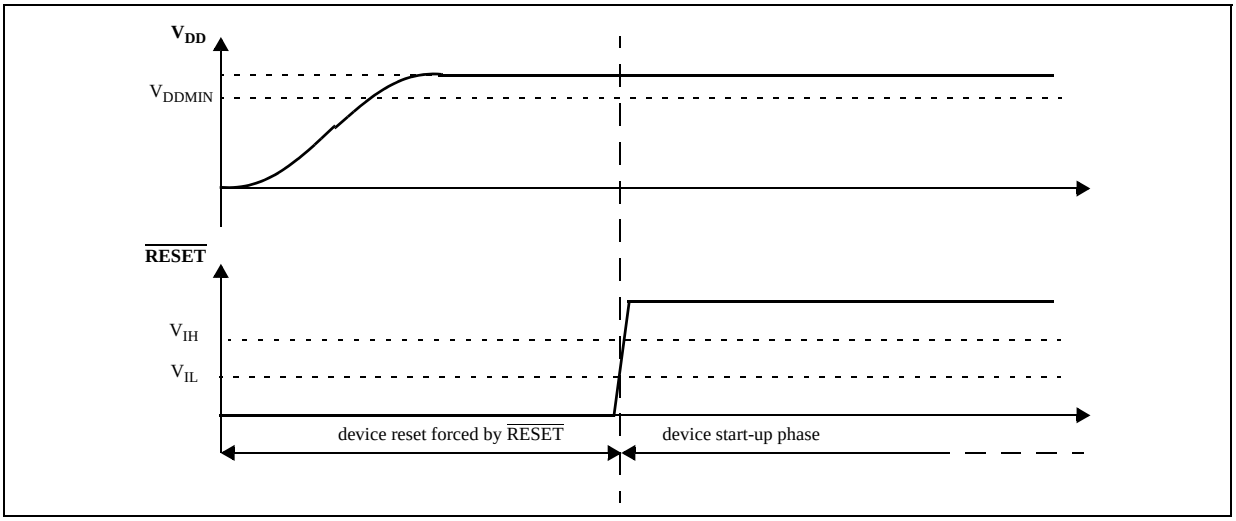


Figure 23. Noise filtering on reset signal

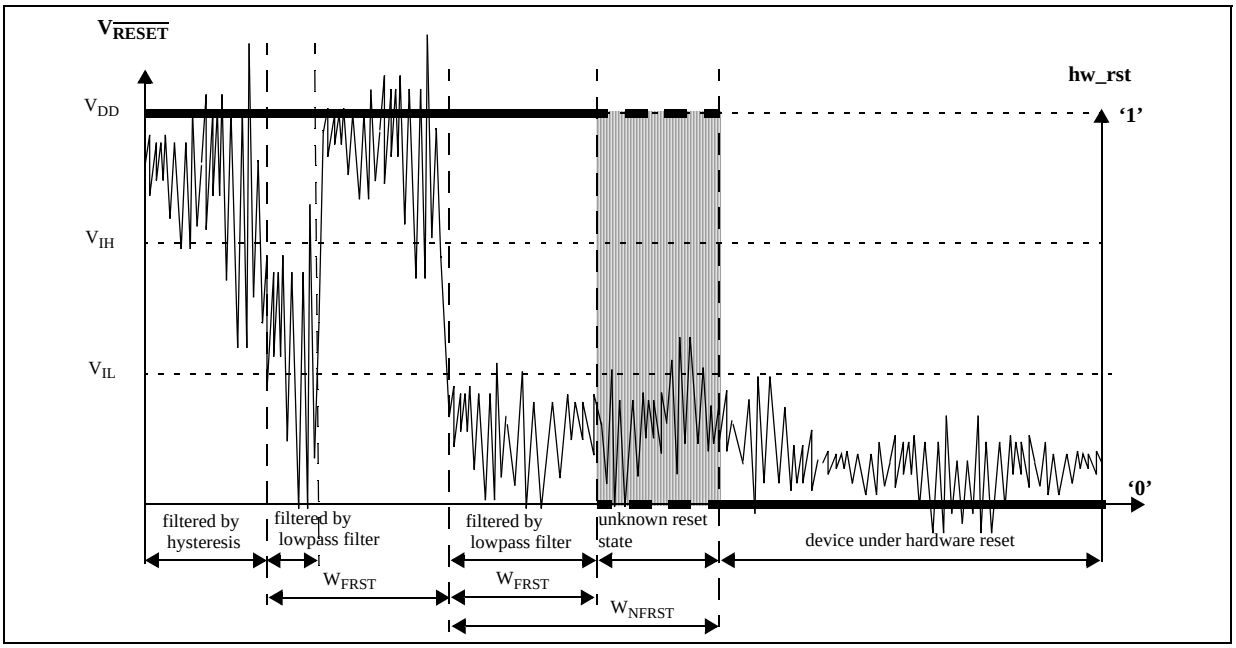
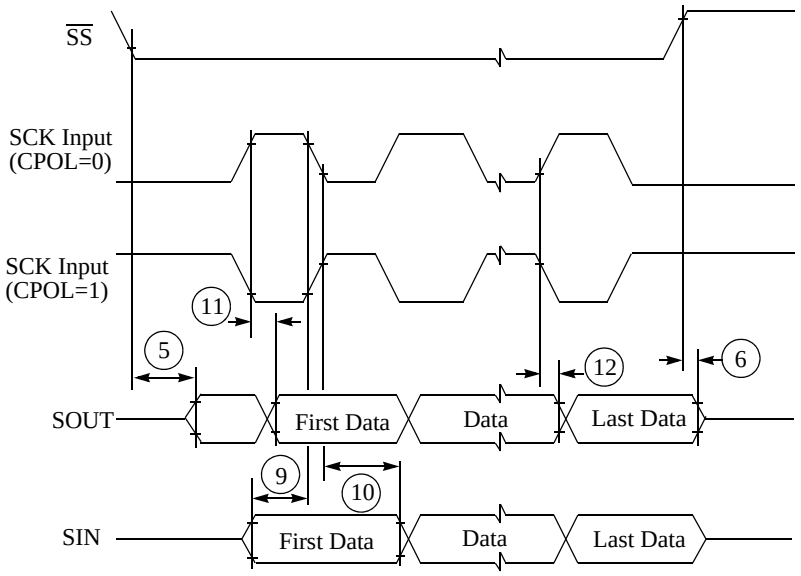


Table 36. RESET electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	nRESET input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	nRESET input not filtered pulse	—	500	—	—	ns

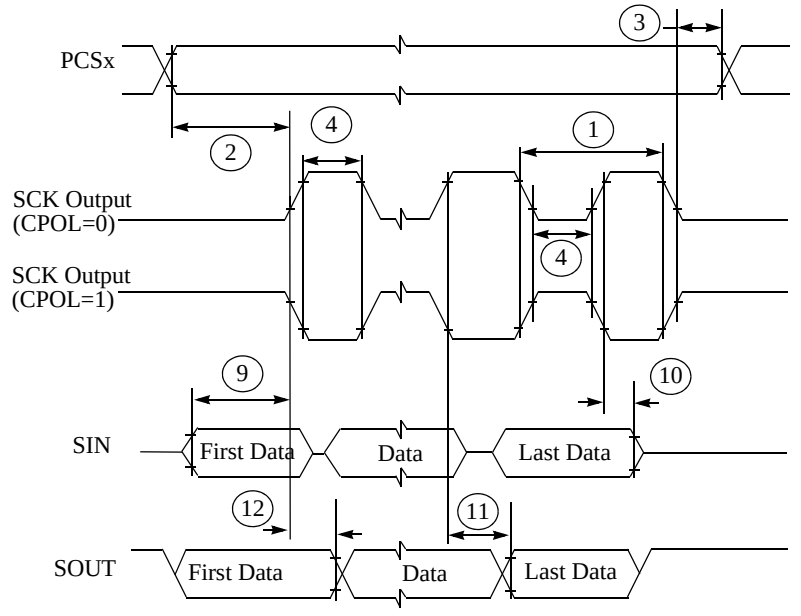
1. V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified.

Figure 35. DSPI classic SPI timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 36. DSPI modified transfer format timing — master, CPHA = 0



Note: The numbers shown are referenced in *Table 41*.

Table 45. Document revision history

Date	Revision	Changes
14-Jun-2010	4 (continued)	In the “Main oscillator electrical characteristics” table, changed the maximum specification for $g_{mXOSCHS}$ (was 11 mA/V, is 11.8 mA/V). Revised the “ADC electrical characteristics” section.In the “ADC conversion characteristics” table: – Changed the t_{ADC_S} specification (was TBD, is minimum of 383 ns). – Added the footnote “No missing codes” to the DNL specification. – Added specifications for SNR, THD, SINAD, and ENOB. Revised the “Ordering information” section.
23-Nov-2010	5	Editorial changes and improvements. Revised the Overview section. Replaced references to PowerPC with references to Power Architecture. In the feature summary, changed “As much as 128 KB on-chip SRAM” to “128 KB on-chip SRAM”. In the “Feature details” section: – In the “On-chip SRAM with ECC” section, added information about required RAM wait states. – In the PIT section, deleted “32-bit counter for real time interrupt, clocked from main external oscillator” (not supported on this device). – In the flash-memory section, changed “16 KB Test” to “16 KB test sector”, revised the wait state information, and deleted the associated Review_Q&A content. – In the SRAM section, revised the wait state information. In the 100-pin pinout diagram: – Renamed pin 41 (was VDD_HV_ADV0_ADV1, is VDD_HV_ADV). – Renamed pin 42 (was VSS_HV_ADV0_ADV1, is VSS_HV_ADV). In the 144-pin pinout diagram: – Renamed pin 58 (was VDD_HV_ADV0_ADV1, is VDD_HV_ADV). – Renamed pin 59 (was VSS_HV_ADV0_ADV1, is VSS_HV_ADV). Added the “LQFP100 pin function summary” table. In the “LQFP144 pin function summary” table, for pin 39, changed $V_{SS\_LV\_COR}$ to $V_{DD\_LV\_COR}$. In the “Supply pins” table: – Changed the description for $V_{DD\_LV\_COR}$ (was “Voltage regulator supply voltage”, is “Core logic supply”). – Changed the description for $V_{DD\_HV\_PMU}$ (was “Core regulator supply”, is “Voltage regulator supply”). In the “Pin muxing” table: – In the “Pad speed” column headings, changed “SRC = 0” to “SRC = 1” and “SRC = 1” to “SRC = 0” – For port B[6], changed the pad speed for SRC=0 (was M, is F). In the “Thermal characteristics” section, added meaningful values to the thermal-characteristics tables. Added the “SWG electrical specifications” section. In the “Voltage regulator electrical characteristics” section, changed the table title (was “HPREG1, HPREG2, Main LVDs, Digital HVD, and Digital LVD electrical specifications”, is “Voltage regulator electrical characteristics”) and revised the table.

Table 45. Document revision history

Date	Revision	Changes
18-Sep-2013	10	– Updated Disclaimer.
07-Feb-2014	11	– Removed “TBC” symbol in *Table 9* and *Table 22* – Resolved some cross references.
08-Jul-2015	12	Editorial and formatting changes throughout document. *Chapter 1: Introduction*: – In *Table 1: SPC56ELx/SPC564Lx device summary* added the column for SPC56EL54 device *Chapter 3: Electrical characteristics*: – In *Table 9: Absolute maximum ratings*, added condition “Valid only for ADC pins” for V_{IN} Symbol. – Added *Section 3.4: Decoupling capacitors*. – *Figure 10: Input Equivalent Circuit*: changed “V_{DD}” to “V_{REF}” in Internal circuit scheme – In *Table 32: Pad AC specifications (3.3 V, IPP_HVE = 0)* updated footnote 1 and footnote 2. – Updated *Figure 13: Pad output delay* Updated Disclaimer.