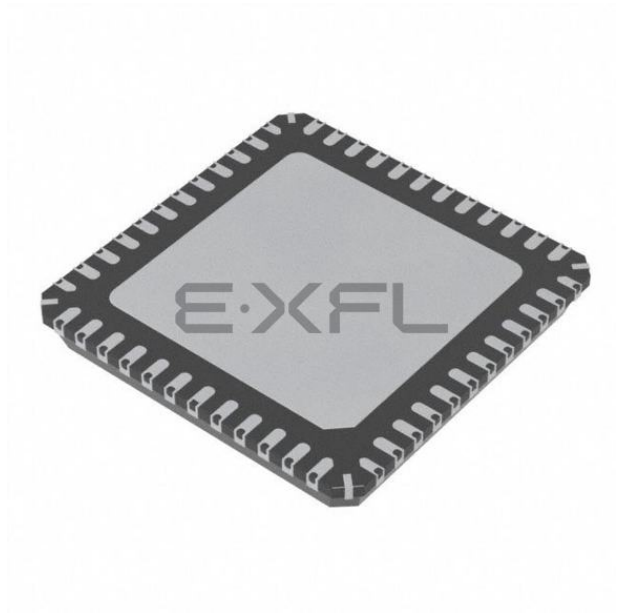

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9879qxa20xuma2

1.1 Abbreviations

The following acronyms and terms are used within this document. List see in Table 1.

Table 1 Acronyms

Acronyms	Name
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
CP	Charge Pump for MOSFET driver
CSA	Current Sense Amplifier
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EIM	Exceptional Interrupt Measurement
FSM	Finite State Machine
GPIO	General Purpose Input Output
H-Bridge	Half Bridge
ICU	Interrupt Control Unit
IEN	Interrupt Enable
IIR	Infinite Impulse Response
LDM	Load Instruction
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
LTI	Lead Tip Inspection
MCU	Memory Control Unit
MF	Measurement Functions
MSB	Most Significant Bit
MPU	Memory Protection Unit
MRST	Master Receive Slave Transmit
MTSR	Master Transmit Slave Receive
MU	Measurement Unit
NMI	Non Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
OTP	One Time Programmable
OSC	Oscillator
PBA	Peripheral Bridge

8.2 Introduction

The ARM Cortex-M3 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Cortex family processors, the Cortex-M3 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Cortex-M3 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block Diagram

Figure 12 shows the functional blocks of the Cortex-M3.

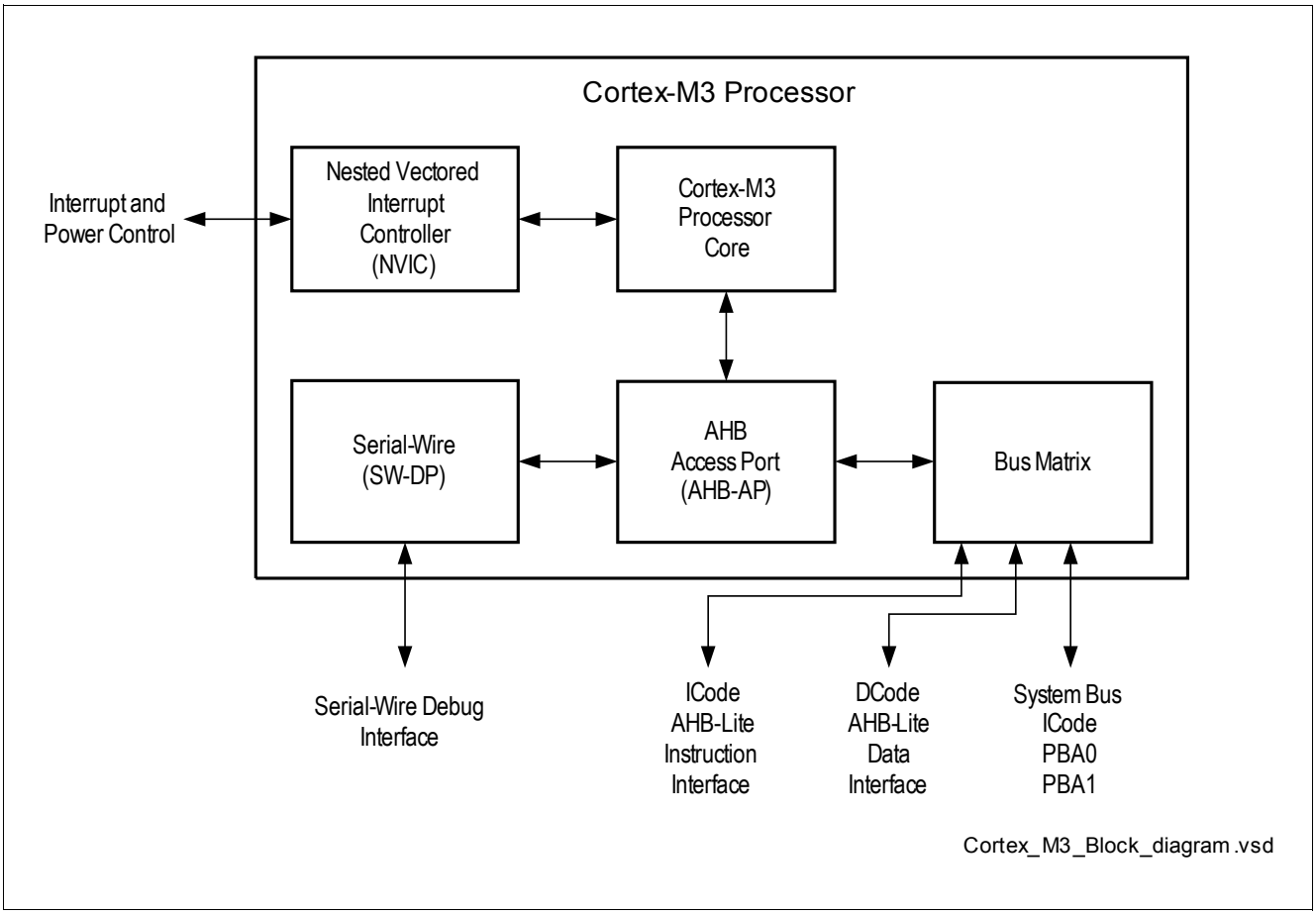

Figure 12 Cortex-M3 Block Diagram

Table 7 NMI Interrupt Table

Service Request	Node	Description
Oscillator Watchdog NMI	NMI	Oscillator Watchdog / MI_CLK Watchdog Timer Overflow
NVM Map Error NMI	NMI	NVM Map Error
ECC Error NMI	NMI	RAM / NVM Uncorrectable ECC Error
Supply Prewarning NMI	NMI	Supply Prewarning

14.3 TLE9879QXA20 Port Module

14.3.1 Port 0

14.3.1.1 Port 0 Functions

Table 8 Port 0 Input/Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.0	Input	GPI	P0_DATA.P0	
		INP1	SWCLK / TCK_0	SW
		INP2	T12HR_0	CCU6
		INP3	T4INA	GPT12T4
		INP4	T2_0	Timer 2
		INP5	–	–
		INP6	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	
		ALT1	T3OUT	GPT12T3
		ALT2	EXF21_0	Timer 21
		ALT3	RXDO_2	UART2
P0.1	Input	GPI	P0_DATA.P1	
		INP2	T13HR_0	CCU6
		INP3	TxD1	LIN_TxD
		INP4	CAPINA	GPT12CAP
		INP5	T21_0	Timer 21
		INP6	T4INC	GPT12T4
		INP7	MRST_1_2	SSC1
		INP8	EXINT0_2	SCU
	Output	GPO	P0_DATA.P1	
		ALT1	TxD1	UART1 / LIN_TxD
		ALT2	–	–
		ALT3	T6OUT	GPT12T6

14.3.3 Port 2

14.3.3.1 Port 2 Functions

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.0	Input	GPI	P2_DATA.P0	
		INP1	CCPOS0_3	CCU6
		INP2	-	-
		INP3	T12HR_2	CCU6
		INP4	EXINT0_0	SCU
		INP5	CC61_2	CCU6
		ANALOG	AN0	ADC
			XTAL (in)	XTAL
P2.2	Input	GPI	P2_DATA.P2	
		INP1	CCPOS2_3	CCU6
		INP2	T13HR_2	CCU6
		INP3	–	
		INP4	CC62_2	CCU6
		ANALOG	AN2	ADC
		OUT	XTAL (out)	XTAL
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	CTRAP#_1	CCU6
		INP3	T21EX_2	Timer 21
		INP4	CC60_1	CCU6
		INP5	EXINT0_3	SCU
		ANALOG	AN3	ADC
P2.4	Input	GPI	P2_DATA.P4	
		INP1	$\overline{\text{CTRAP\#}}$_0	CCU6
		INP2	T2EUDB	GPT12T2
		INP3	MRST_1_1	SSC1
		INP4	EXINT1_3	SCU
		ANALOG	AN4	ADC
P2.5	Input	GPI	P2_DATA.P5	
		INP1	RXD2_1	UART2
		INP2	T3EUDB	GPT12T3
		INP3	MRST_2_1	SSC2
		INP4	T2_1	Timer 2
		ANALOG	AN5	ADC

16 Timer2 and Timer21

16.1 Features

- 16-bit auto-reload mode
  - selectable up or down counting
- One channel 16-bit capture mode

16.2 Introduction

The timer modules are general-purpose 16-bit timers. Timer 2/21 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{PCLK}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{PCLK}/24$ (if prescaler is disabled).

16.2.1 Timer2 and Timer21 Modes Overview

Table 11 Timer2 and Timer21 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events.
Auto-reload	**Up/Down Count Enabled** • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated by reload or capture events

17 Timer3

17.1 Features

- 16-bit incremental timer/counter (counting up)
- Counting frequency up to f_{sys}
- Selectable clock prescaler
- 6 modes of operation
- Interrupt up on overflow
- Interrupt on compare

17.2 Introduction

The possible applications for the timer include measuring the time interval between events, counting events and generating a signal at regular intervals.

Timer3 can function as timer or counter. When functioning as a timer, Timer3 is incremented in periods based on the MI_CLK or LP_CLK clock. When functioning as a counter, Timer3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer3 can be configured in four different operating modes to use in a variety of applications, see **Table 12**.

Several operating modes can be used for different tasks such as the following:

- simple time measurement between two events
- triggering of the measuring unit upon PWM/CCU6 unit
- measurement of the 100kHz LP_CLK2

17.3 Functional Description

Six modes of operation are provided to fulfill various tasks using this timer. In every mode the clocking source can be selected between MI_CLK and LP_CLK. A prescaler provides in addition capability to divide the selected clock source by 2, 4 or 8. The timer counts upwards, starting with the value in the timer count registers, until the maximum count value which depends on the selected mode of operation. Timer 3 provides two individual interrupts upon counter overflow, one for the low-byte and one for the high-byte counter register.

17.3.1 Timer3 Modes Overview

The following table provides an overview of the timer modes together with the reasonable configuration options in **Table 12**.

Table 12 Timer3 Modes

Mode	Sub-Mode	Operation
0	**No Sub-Mode**	**13-bit Timer** The timer is essentially an 8-bit counter with a divide-by-32 prescaler.
1	**a**	**16-bit Timer** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter.
1	**b**	**16-bit Timer triggered by an event** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter, which is triggered by an event to enable a single shot measurement on a preset channel with the measurement unit.

Table 12 Timer3 Modes (cont'd)

Mode	Sub-Mode	Operation
2	**No Sub-Mode**	**8-bit Timer with auto-reload** The timer register TL3 is reloaded with a user-defined 8-bit value in TH3 upon overflow.
3	**a**	**Timer3 operates as two 8-bit timers** The timer registers TL3 and TH3, operate as two separate 8-bit counters.
3	**b**	**Timer3 operates as Two 8-bit timers for clock measurement** The timer registers, TL3 and TH3 operate as two separate 8-bit counters. In this mode the LP_CLK2 Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as a counter which counts the time between the edges.

20.2 Introduction

The LIN Module is a transceiver for the Local Interconnect Network (LIN) compliant to the LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kBaud and 20 kBaud. Additionally baud rates up to 115.2 kBaud are implemented.

The LIN Module offers several different operation modes, including a LIN Sleep Mode and the LIN Normal Mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115.2 kBaud is implemented. This Flash Mode can be used for data transfer under special conditions for up to 250 kbit/s (in production environment, point-to-point communication with reduced wire length and limited supply voltage).

20.2.1 Block Diagram

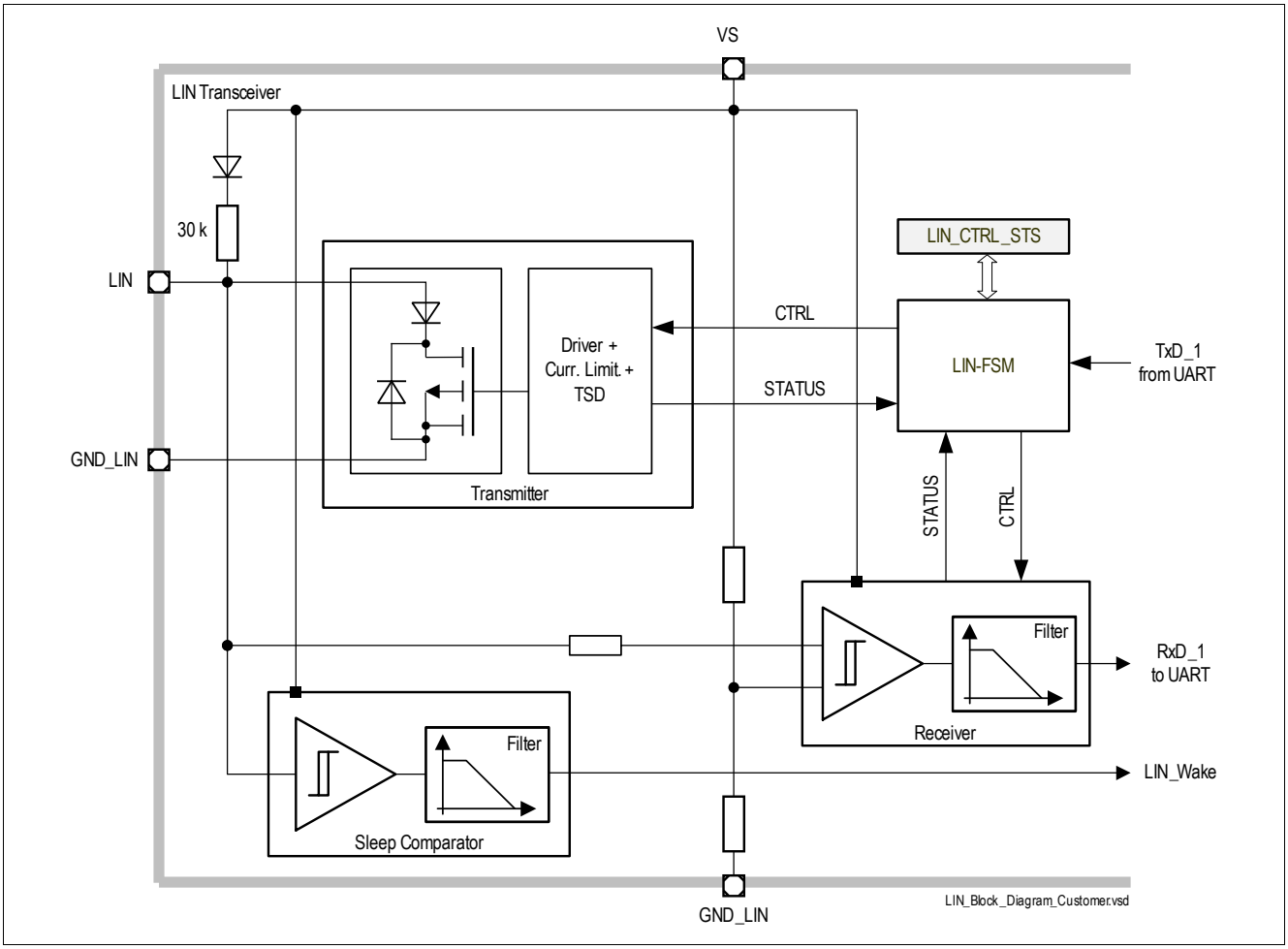

Figure 23 LIN Transceiver Block Diagram

21 High-Speed Synchronous Serial Interface (SSC1/SSC2)

21.1 Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: Least Significant Bit (LSB) or Most Significant Bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a “receiver full” condition
  - On an error condition (receive, phase, baud rate, transmission error)

28 Application Information

28.1 BLDC Driver

Figure 32 shows the TLE9879QXA20 in an electric drive application setup controlling a BLDC motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

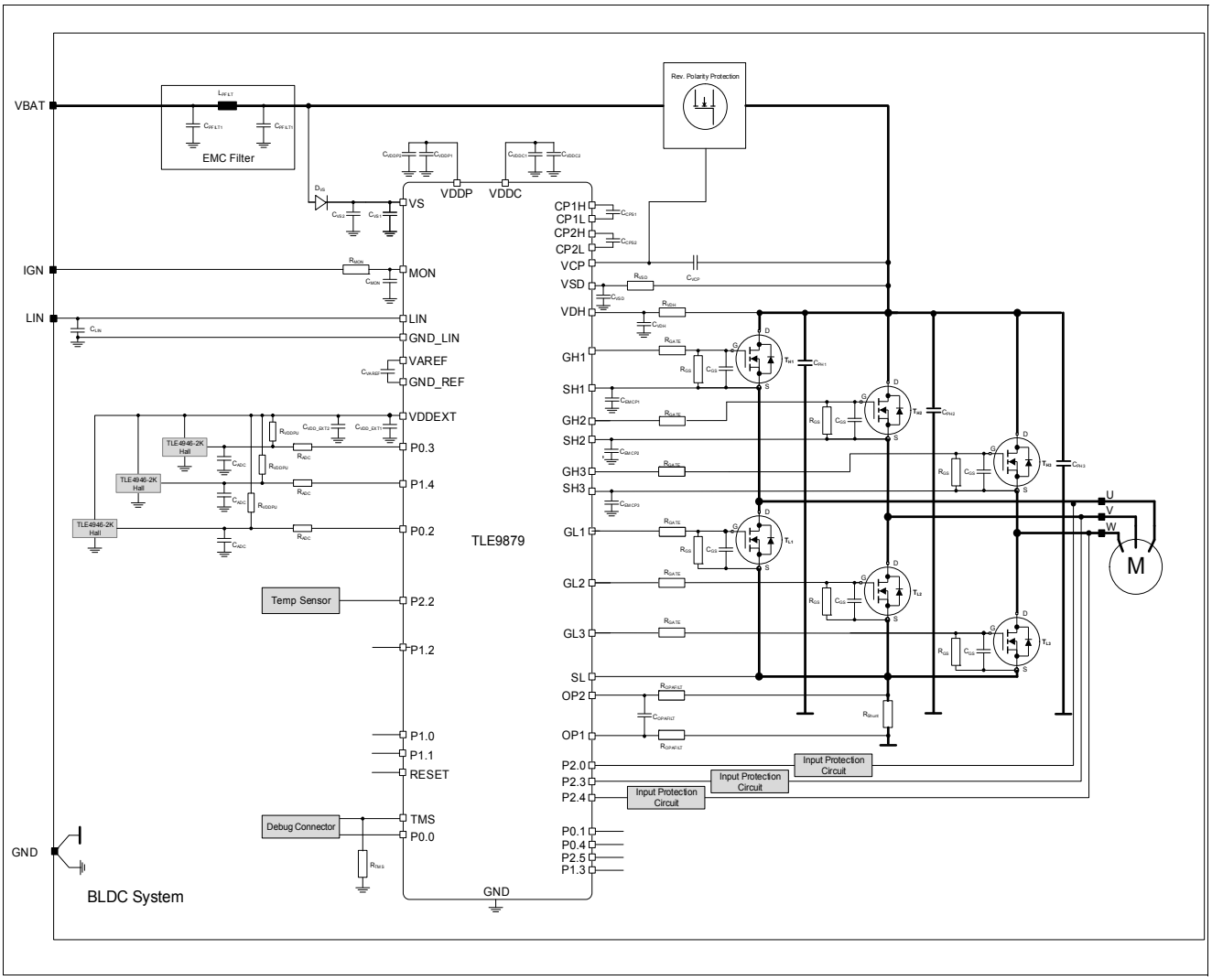

Figure 32 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

28.2 ESD Immunity According to IEC61000-4-2

Note: Tests for ESD immunity according to IEC61000-4-2 “Gun test” (150pF, 330Ω) has been performed. The results and test condition will be available in a test report.

Table 16 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin LIN, versus GND[1)]	> 6	kV	[2)]positive pulse
ESD at pin LIN, versus GND[1)]	< -6	kV	[2)]negative pulse

1) ESD test “ESD GUN” is specified with external components; see application diagram: C_{MON} = 100 nF, R_{MON} = 1 kΩ, C_{LIN} = 220 pF, C_{VS} = >20 µF ELCO + 100 nF ESR < 1 Ω, C_{VSD} = 1 µF, R_{VSD} = 2 Ω.

2) ESD susceptibility “ESD GUN” according to LIN EMC Test Specification, Section 4.3 (IEC 61000-4-2). To be tested by external test house (IBEE Zwickau)

29.2.5 Power Down Voltage Regulator (PMU Subblock) Parameters

The PMU Power Down voltage regulator consists of two subblocks:

- Power Down Pre regulator: VDD5VPD
- Power Down Core regulator: VDD1V5_PD (Supply used for GPUDATAxy registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameters:

Table 26 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VDD1V5_PD							
Power-On Reset Threshold	$V_{DD1V5\_PD\_RSTTH}$	1.2	–	1.5	V	1)	P_2.5.1

1) Not subject to production test, specified by design

1) The typical oscillator frequency is 5 MHz
2) V_{DDC} = 1.5 V, T_j = 25°C
3) Not subject to production test, specified by design.
4) This parameter is valid for PLL operation with an external clock source and thus reflects the real PLL performance.

29.3.2 External Clock Parameters XTAL1, XTAL2

Table 28 Functional Range

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range limits for signal on XTAL1	V_{IX1_SR}	-1.7 + V_{DDC}	–	1.7	V	[2)]	P_3.2.1
Input voltage (amplitude) on XTAL1	V_{AX1_SR}	0.3 x V_{DDC}	–	–	V	[3)] Peak-to-peak voltage	P_3.2.2
XTAL1 input current	I_{IL}	–	–	±20	µA	0 V < V_{IN} < V_{DDI}	P_3.2.3
Oscillator frequency	f_{OSC}	4	–	24	MHz	Clock signal	P_3.2.4
Oscillator frequency	f_{OSC}	4	–	16	MHz	Crystal or Resonator	P_3.2.5
High time	t_1	6	–	–	ns	–	P_3.2.6
Low time	t_2	6	–	–	ns	–	P_3.2.7
Rise time	t_3	–	8	8	ns	–	P_3.2.8
Fall time	t_4	–	8	8	ns	–	P_3.2.9

1) This parameter table is not subject to production test, specified by design.
2) Overload conditions must not occur on pin XTAL1.
3) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

29.5 Parallel Ports (GPIO)

29.5.1 Description of Keep and Force Current

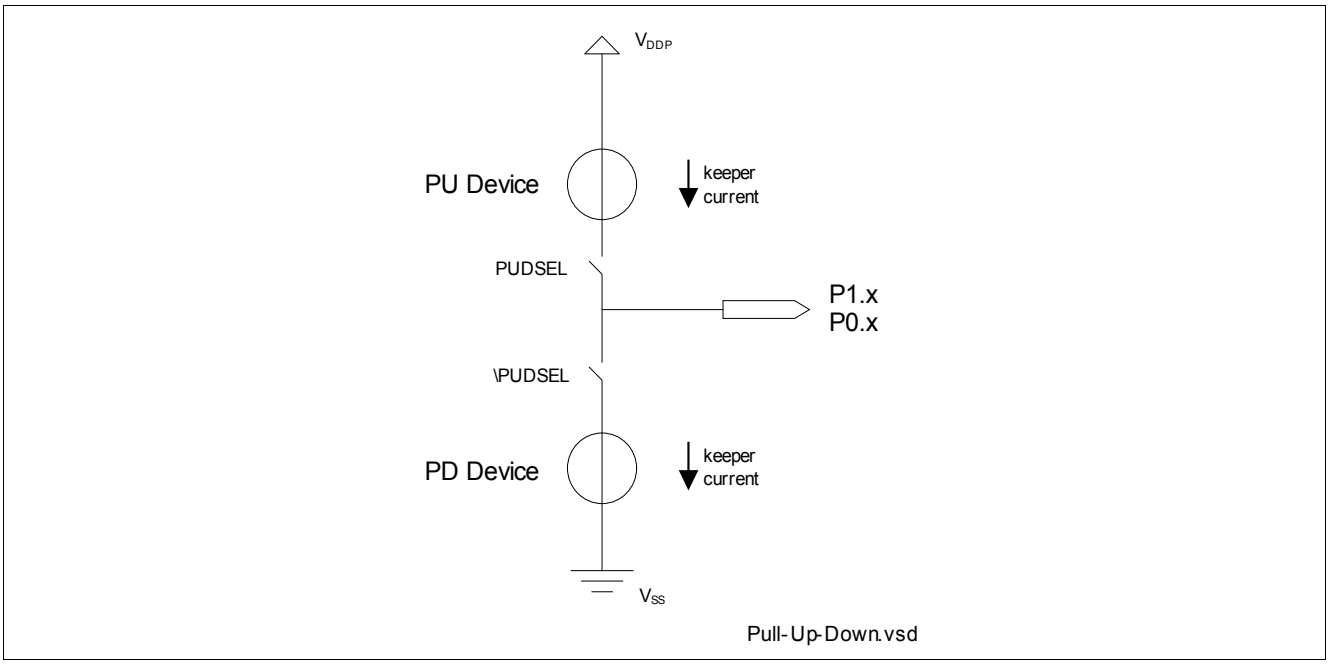

Figure 34 Pull-Up/Down Device

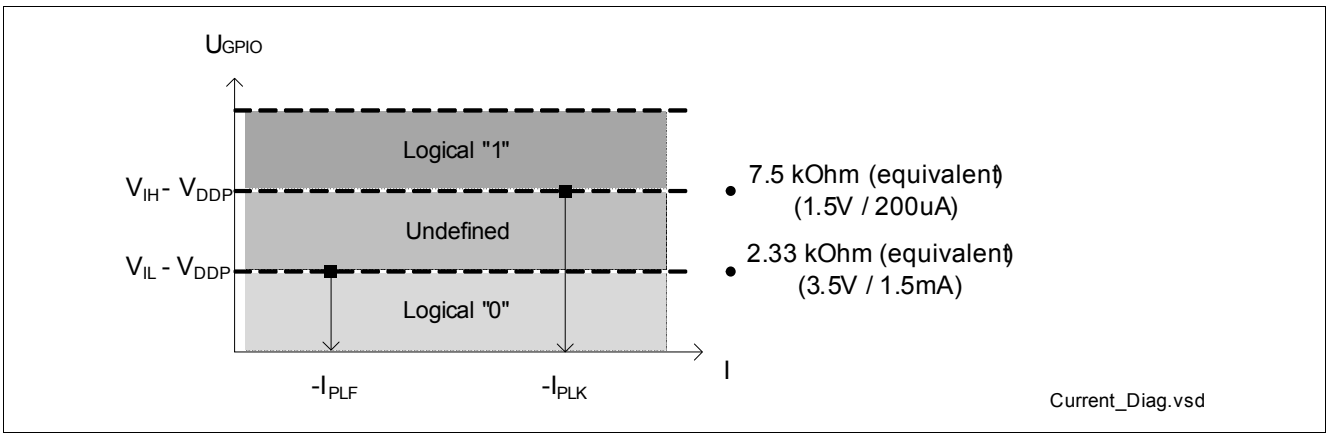

Figure 35 Pull-Up Keep and Forced Current

Table 31 DC Characteristics Port0, Port1 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.3
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.17
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.4
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.18
Output low voltage	V_{OL}	–	–	1.0	V	3) 4) $I_{OL} \leq I_{OLmax}$	P_5.1.6
Output low voltage	V_{OL}	–	–	0.4	V	3) 5) $I_{OL} \leq I_{OLnom}$	P_5.1.7
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	3) 4) $I_{OH} \geq I_{OHmax}$	P_5.1.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	3) 5) $I_{OH} \geq I_{OHnom}$	P_5.1.9
Input leakage current	$I_{OZ\_extend1}$	-500	–	+500	nA	-40°C ≤ T_J ≤ 25°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.20
Input leakage current	I_{OZ1}	-5	–	+5	µA	6) 25°C < T_J ≤ 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.10
Input leakage current	$I_{OZ\_extend2}$	-15	–	+15	µA	85°C < T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.11
Pull level keep current	I_{PLK}	-200	–	+200	µA	7) $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (dn)	P_5.1.12
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	7) $V_{PIN} \leq V_{IL}$ (up) $V_{PIN} \geq V_{IH}$ (dn)	P_5.1.13
Pin capacitance	C_{IO}	–	–	10	pF	1)	P_5.1.14
Reset Pin Timing							
Reset Pin Input Filter Time	t_{filt_RESET}	–	5	–	µs	1)	P_5.1.19

1) Not subject to production test, specified by design.

2) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

4) Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 4mA, I_{OH} = -4mA, specified for 4.5V < V_{DDP} < 5.5V.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow GND$, $V_{OH} \rightarrow V_{DDP}$). Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 1mA, I_{OH} = -1mA.

Table 35 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Charge Pump Voltage Measurement V_{CP}							
Input to output voltage attenuation: V_{CP}	ATT_{VCP}	–	0.023	–		–	P_8.1.56
Nominal operating input voltage range V_{CP}	$V_{CP,range}$	2.5	–	52	V	1)	P_8.1.7
Accuracy of V_{CP} sense after calibration	ΔV_{CP}	-747	–	747	mV	V_S = 5.5V to 18V	P_8.1.62
Monitoring Input Voltage Measurement V_{MON}							
Input to output voltage attenuation: V_{MON}	ATT_{VMON}	–	0.039	–		–	P_8.1.49
Nominal operating input voltage range V_{MON}	$V_{MON,range}$	2.5	–	31	V	1)	P_8.1.8
Accuracy of V_{MON} sense after calibration	ΔV_{MON}	-440	–	440	mV	V_S = 5.5V to 18V	P_8.1.68
Pad Supply Voltage Measurement V_{VDDP}							
Input-to-output voltage attenuation: V_{DDP}	ATT_{VDDP}	–	0.164	–		–	P_8.1.33
Nominal operating input voltage range V_{DDP}	$V_{DDP,range}$	0	–	7.50	V	1)	P_8.1.50
Accuracy of V_{DDP} sense after calibration	ΔV_{DDP_SENSE}	-105	–	105	mV	2) V_S = 5.5 to 18V	P_8.1.5
10-Bit ADC Reference Voltage Measurement V_{AREF}							
Input to output voltage attenuation: V_{AREF}	ATT_{VAREF}	–	0.219	–		–	P_8.1.22
Nominal operating input voltage range V_{AREF}	$V_{AREF,range}$	0	–	5.62	V	1)	P_8.1.51
Accuracy of V_{AREF} sense after calibration	ΔV_{AREF}	-79	–	79	mV	V_S = 5.5V to 18V	P_8.1.48
8-Bit ADC Reference Voltage Measurement V_{BG}							
Input-to-output voltage attenuation: V_{BG}	ATT_{VBG}	–	0.75	–		–	P_8.1.57
Nominal operating input voltage range V_{BG}	$V_{BG,range}$	0.8	–	1.64	V	1)	P_8.1.52

29.9 ADC1 Reference Voltage - VAREF

29.9.1 Electrical Characteristics VAREF

Table 39 Electrical Characteristics VAREF

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Required buffer capacitance	C_{VAREF}	0.1	–	1	µF	ESR < 1Ω	P_9.1.1
Reference output voltage	V_{AREF}	4.95	5	5.05	V	V_S > 5.5V	P_9.1.2
DC supply voltage rejection	$DC_{PSRVAREF}$	30	–	–	dB	1) –	P_9.1.3
Supply voltage ripple rejection	$AC_{PSRVAREF}$	26	–	–	dB	1) V_S = 13.5V; f = 0 ... 1KHz; V_r = 2Vpp	P_9.1.4
Turn ON time	t_{so}	–	–	200	µs	1) C_{ext} = 100nF PD_N to 99.9% of final value	P_9.1.5
Input resistance at VAREF Pin	$R_{IN,VAREF}$	–	100	–	kΩ	1)input impedance in case of VAREF is applied from external	P_9.1.20

1) Not subject to production test, specified by design.

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Resistor between SHx and GND	R_{SHGN}	30	40	50	kΩ	1)3) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to 0,6V typ. before it is discharged through the resistor.	P_12.1.10
Low RDSON mode (boosted discharge mode)	R_{ONCCP}	–	9	12	Ω	V_{VSD} = 13.5 V, V_{VCP} = V_{VSD} + 14.0 V; I_{CHARGE} = I_{DISCHG} = 31(max); 50mA forced into Gx, Sx grounded	P_12.1.50
Resistance between VDH and VSD	I_{BSH}	–	4	–	kΩ	1)	P_12.1.24
Input propagation time (LS on)	$t_{P(ILN)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, I_{Charge} =3(min), 25% of V_{Gxx1}	P_12.1.37
Input propagation time (LS off)	$t_{P(ILF)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, $I_{Discharge}$ =3(min), 75% of V_{Gxx1}	P_12.1.38
Input propagation time (HS on)	$t_{P(IHN)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, I_{Charge} =3(min) 25% of V_{Gxx1}	P_12.1.39
Input propagation time (HS off)	$t_{P(IHF)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, $I_{Disharge}$ =3(min), 75% of V_{Gxx1}	P_12.1.40
Input propagation time (LS on)	$t_{P(ILN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.26
Input propagation time (LS off)	$t_{P(ILF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.27
Input propagation time (HS on)	$t_{P(IHN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.28
Input propagation time (HS off)	$t_{P(IHF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.29

30 Package Outlines

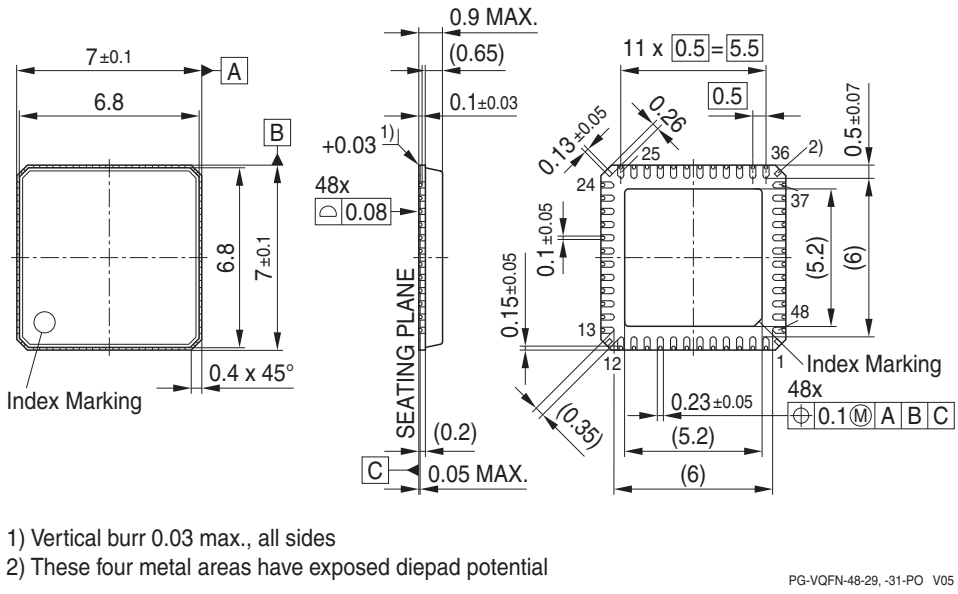

Figure 38 Package outline VQFN-48-31 (with LTI)

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.*
2. *Dimensions in mm.*