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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C, SPI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	176 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc924t-04-l

1.0 GENERAL DESCRIPTION

The PIC16C9XX is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers with an integrated LCD Driver module, in the PIC16CXXX mid-range family.

All PICmicro™ microcontrollers employ an advanced RISC architecture. The PIC16CXXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C923** devices have 176 bytes of RAM and 25 I/O pins. In addition several peripheral features are available including: three timer/counters, one Capture/Compare/PWM module, one serial port and one LCD module. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The LCD module features programmable multiplex mode (static, 1/2, 1/3 and 1/4) and drive bias (static and 1/3). It is capable of driving up to 32 segments and up to 4 commons. It can also drive the LCD panel while in SLEEP mode.

The **PIC16C924** devices have 176 bytes of RAM and 25 I/O pins. In addition several peripheral features are available including: three timer/counters, one Capture/Compare/PWM module, one serial port and one LCD module. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The LCD module features programmable multiplex mode (static, 1/2, 1/3 and 1/4) and drive bias (static and 1/3). It is capable of driving up to 32 segments and up to 4 commons. It can also drive the LCD panel while in SLEEP mode. The PIC16C924 also has an 5-channel high-speed 8-bit A/D. The 8-bit resolution is ideally suited for applications requiring low-cost analog interface, e.g. thermostat control, pressure sensing, and meters.

The PIC16C9XX family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) feature provides a power saving mode. The user can wake up the chip from SLEEP through several external and internal interrupts and reset(s).

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides recovery in the event of a software lock-up.

A UV erasable CERQUAD (compatible with PLCC) packaged version is ideal for code development while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C9XX family fits perfectly in applications ranging from handheld meters, thermostats, to home security products. The EPROM technology makes customization of application programs (LCD panels, calibration constants, sensor interfaces, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16C9XX very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, capture and compare, PWM functions and coprocessor applications).

1.1 Family and Upward Compatibility

Users familiar with the PIC16C5X microcontroller family will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for the PIC16C5X can be easily ported to the PIC16CXXX family of devices (Appendix B).

1.2 Development Support

PIC16C9XX devices are supported by the complete line of Microchip Development tools.

Please refer to Section 16.0 for more details about Microchip's development tools.

FIGURE 3-1: PIC16C923 BLOCK DIAGRAM

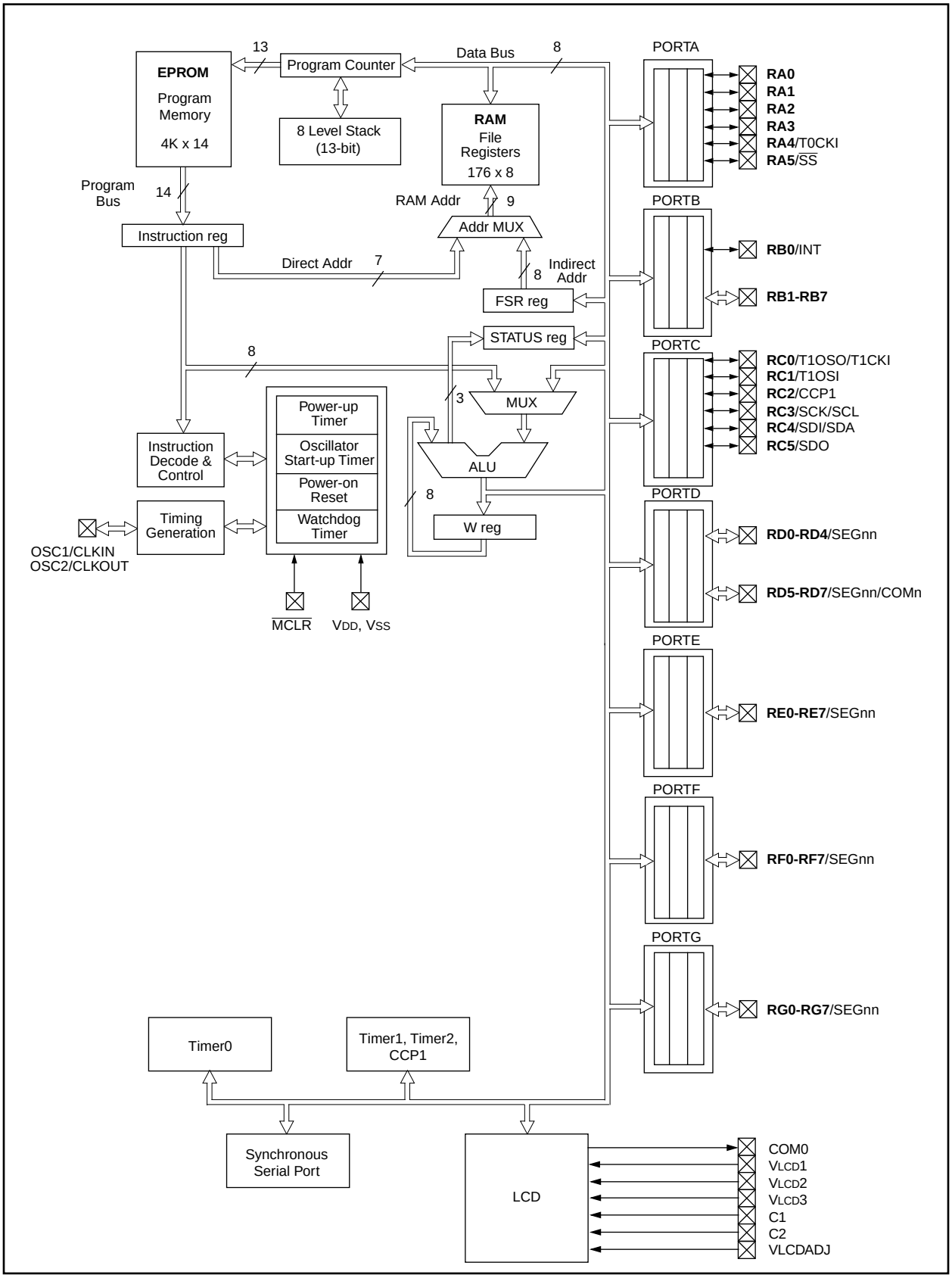
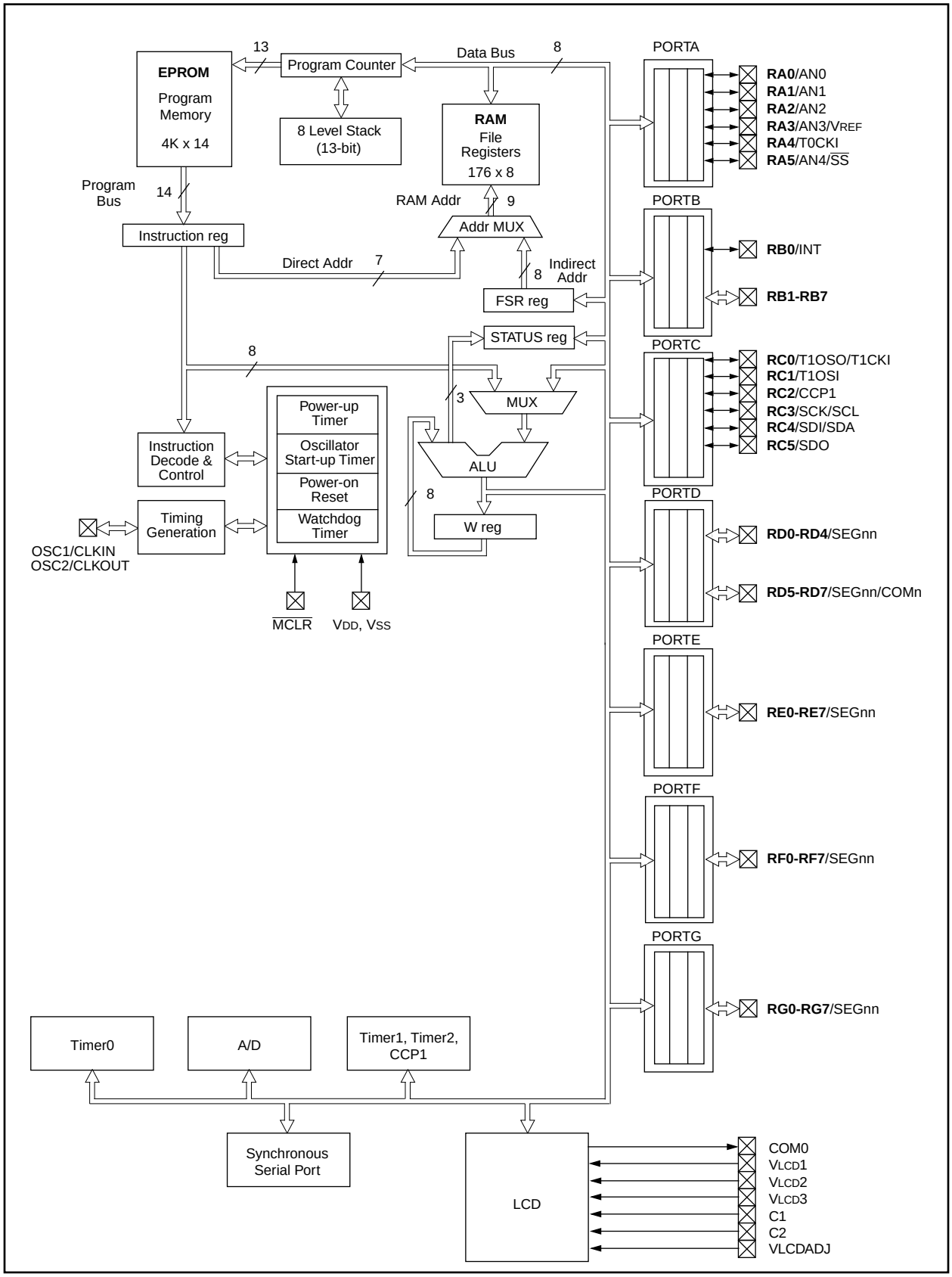


FIGURE 3-2: PIC16C924 BLOCK DIAGRAM



5.7 PORTG and TRISG Register

PORTG is an digital input only port. Each pin is multiplexed with an LCD segment driver. These pins have Schmitt Trigger input buffers.

Note 1: On a Power-on Reset these pins are configured as LCD segment drivers.

Note 2: To configure the pins as a digital port, the corresponding bits in the LCDSE register must be cleared. Any bit set in the LCDSE register overrides any bit settings in the corresponding TRIS register.

EXAMPLE 5-7: INITIALIZING PORTG

```
BCF STATUS,RP0    ;Select Bank2
BSF STATUS,RP1    ;
BCF LCDSE,SE27    ;Make all PORTG
BCF LCDSE,SE20    ;and PORTE<7>
                  ;digital inputs
```

FIGURE 5-10: PORTG BLOCK DIAGRAM

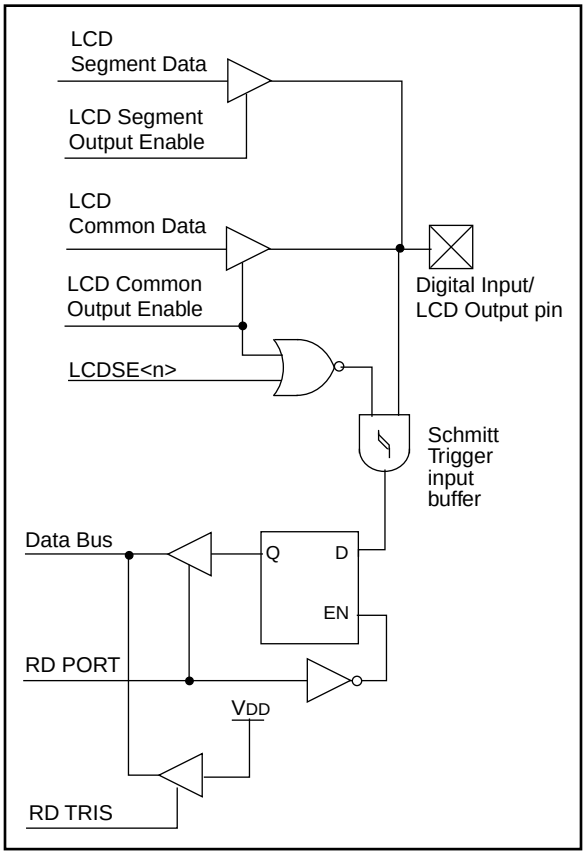


TABLE 5-13: PORTG FUNCTIONS

Name	Bit#	Buffer Type	Function
RG0/SEG20	bit0	ST	Digital input or Segment Driver20
RG1/SEG21	bit1	ST	Digital input or Segment Driver21
RG2/SEG22	bit2	ST	Digital input or Segment Driver22
RG3/SEG23	bit3	ST	Digital input or Segment Driver23
RG4/SEG24	bit4	ST	Digital input or Segment Driver24
RG5/SEG25	bit5	ST	Digital input or Segment Driver25
RG6/SEG26	bit6	ST	Digital input or Segment Driver26
RG7/SEG28	bit7	ST	Digital input or Segment Driver28 (not available on 64-pin devices)

Legend: ST = Schmitt Trigger input

TABLE 5-14: SUMMARY OF REGISTERS ASSOCIATED WITH PORTG

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
108h	PORTG	RG7	RG6	RG5	RG4	RG3	RG2	RG1	RG0	0000 0000	0000 0000
188h	TRISG	PORTG Data Direction Control Register								1111 1111	1111 1111
10Dh	LCDSE	SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0	1111 1111	1111 1111

Legend: Shaded cells are not used by PORTG.

The $\overline{SS}$ pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set for the synchronous slave mode to be enabled. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/ pull-down resistors may be desirable, depending on the application.

Note:	When the SPI is in Slave Mode with $\overline{SS}$ pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the $\overline{SS}$ pin is set to V_{DD}.
Note:	If the SPI is used in Slave Mode with CKE = '1', then the $\overline{SS}$ pin control must be enabled.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-5: SPI MODE TIMING, MASTER MODE

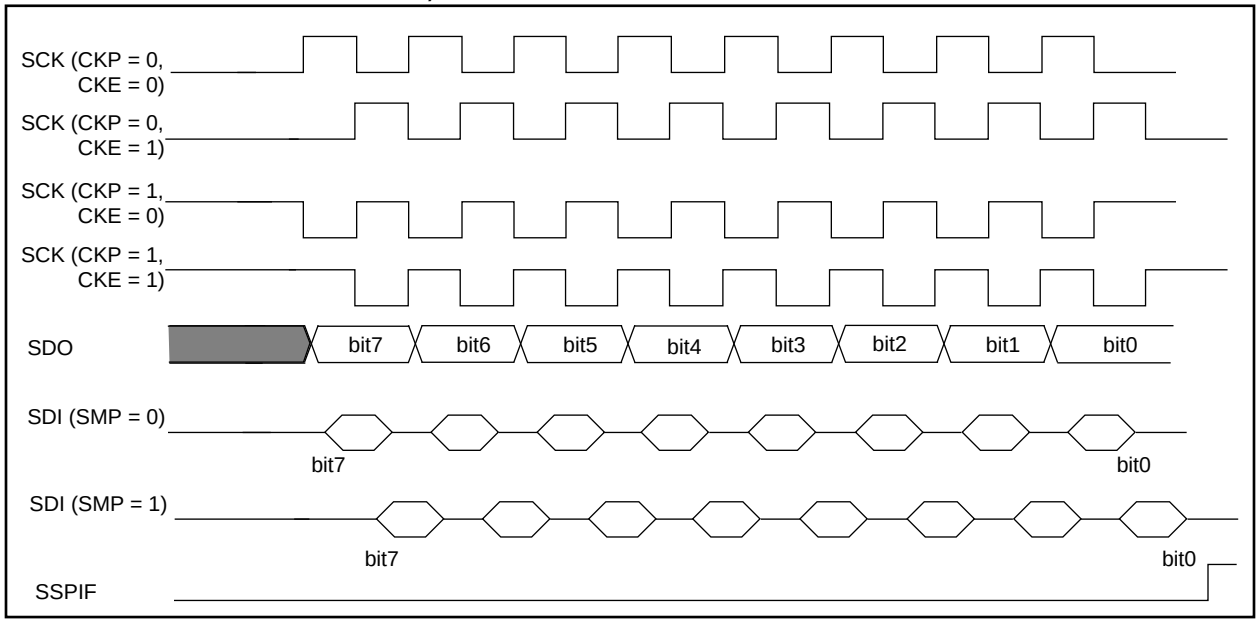
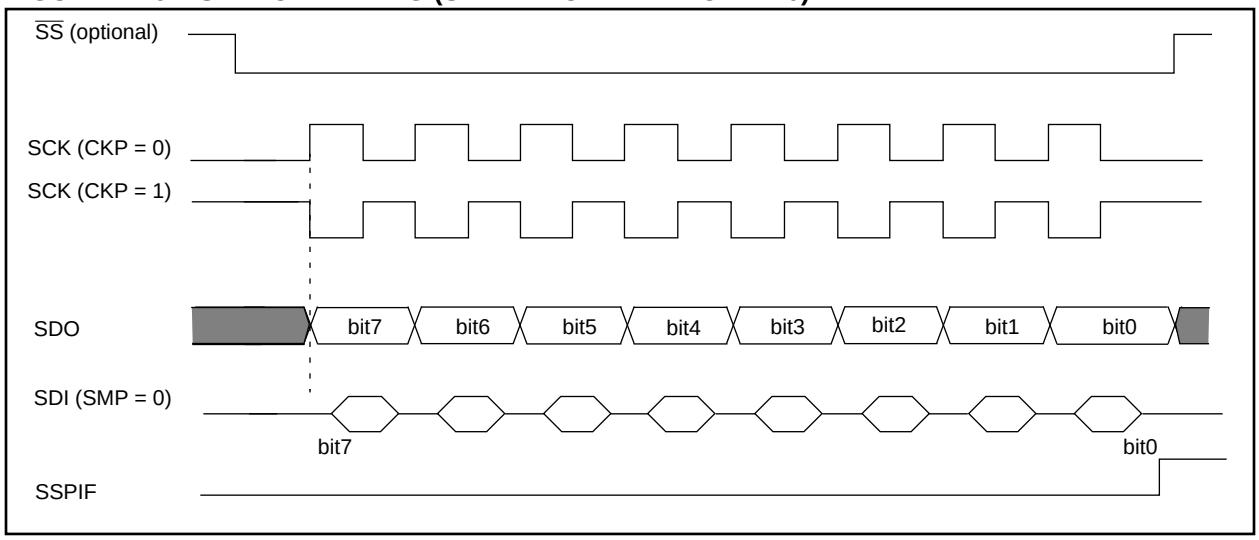


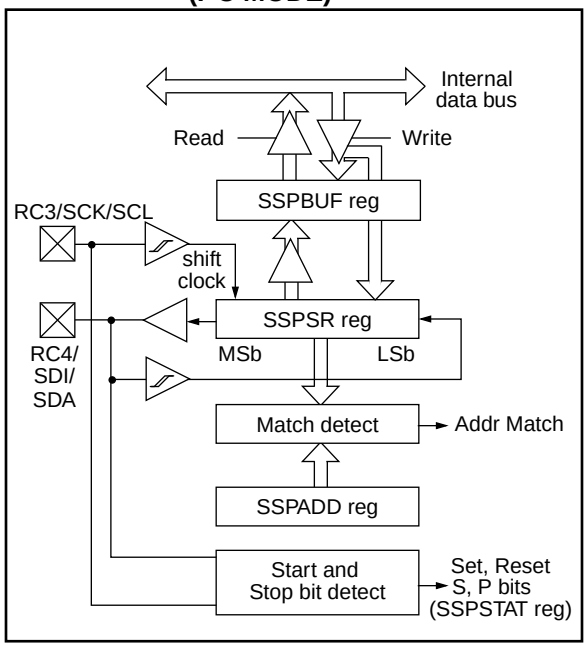
FIGURE 11-6: SPI MODE TIMING (SLAVE MODE WITH CKE = 0)



11.3 SSP I²C Operation

The SSP module in I²C mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

FIGURE 11-18: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
- I²C Firmware controlled Master Mode, slave is idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

FIGURE 12-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-3: **Unimplemented:** Read as '0'

bit 2-0: **PCFG2:PCFG0**: A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA5	RA3	VREF
000	A	A	A	A	A	AVDD
001	A	A	A	A	VREF	RA3
010	A	A	A	A	A	AVDD
011	A	A	A	A	VREF	RA3
100	A	A	D	D	A	AVDD
111	D	D	D	D	D	—

A = Analog input

D = Digital I/O

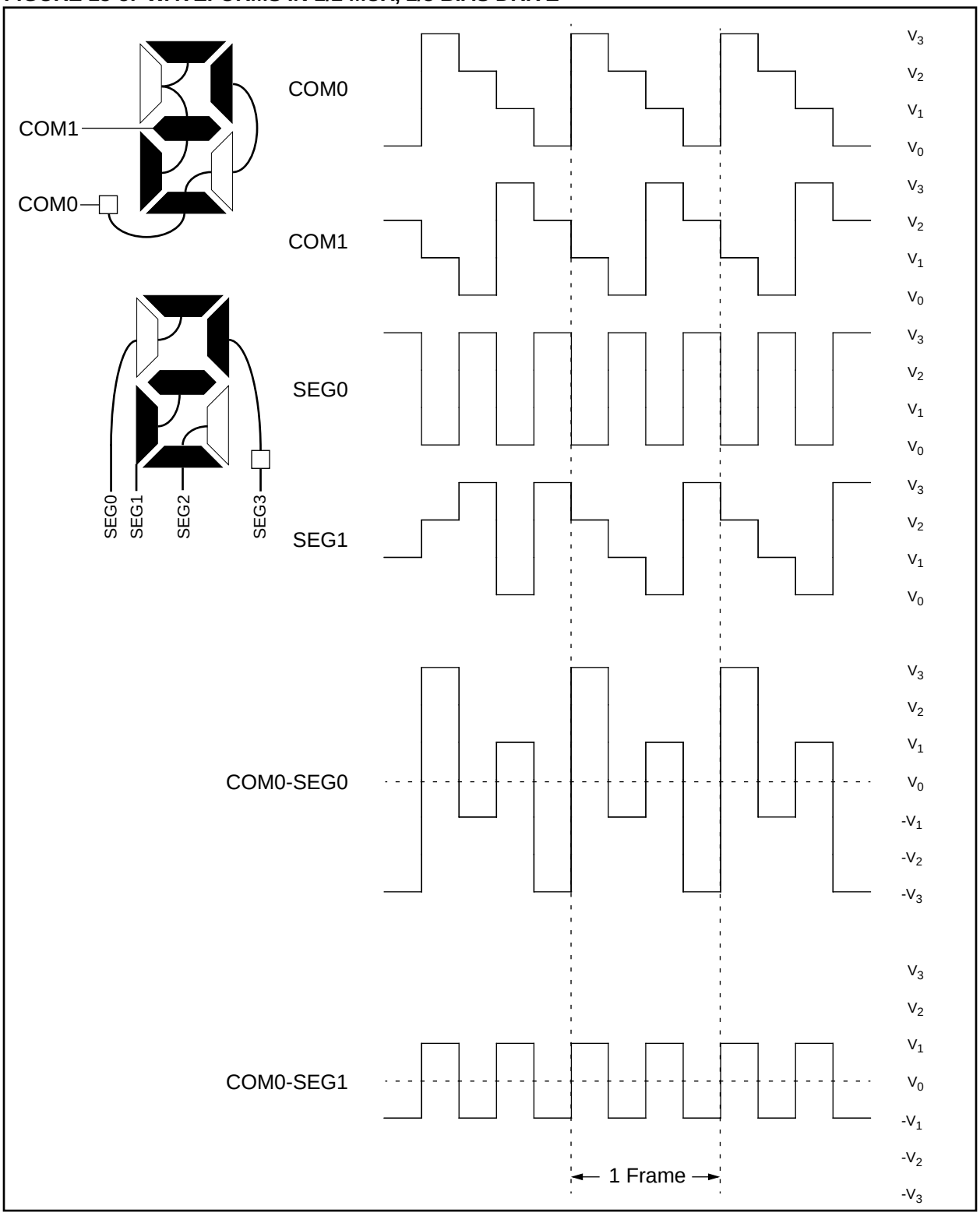
The ADRES register contains the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 12-3.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Section 12.1. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins / voltage reference / and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

FIGURE 13-5: WAVEFORMS IN 1/2 MUX, 1/3 BIAS DRIVE

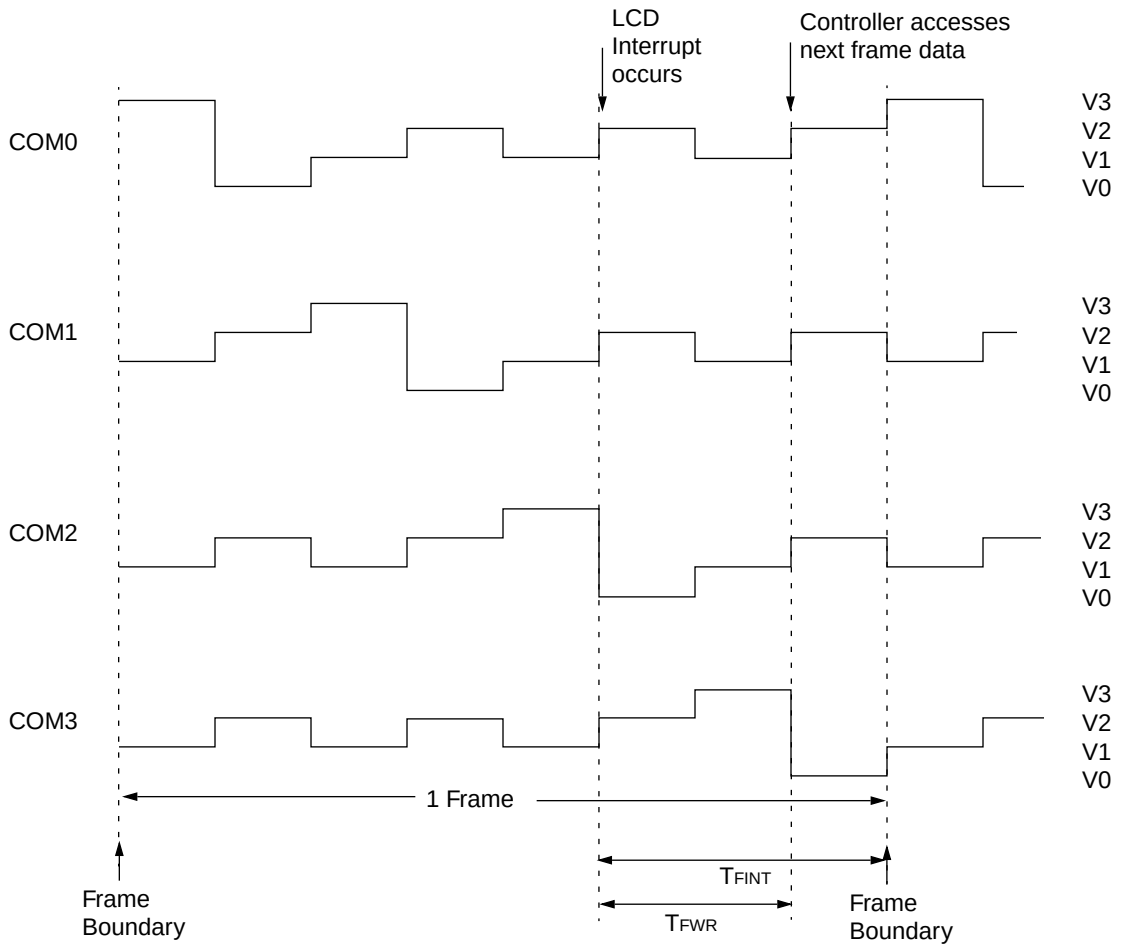


13.2 LCD Interrupts

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame. Writing pixel data at the frame boundary allows a visually crisp transition of the image. This interrupt can also be used to synchronize external events to the LCD. For example, the interface to an external segment driver, such as a Microchip AY0438, can be synchronized for segment data update to the LCD frame.

A new frame is defined to begin at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a certain fixed time before the frame boundary as shown in Figure 13-9. The LCD controller will begin to access data for the next frame within T_{FWR} after the interrupt.

FIGURE 13-9: EXAMPLE WAVEFORMS IN 1/4 MUX DRIVE



$T_{FWR} = T_{FRAME}/(LMUX1:LMUX0 + 1)$

$T_{FINT} = (T_{FWR}/2 - (2T_{CY} + 40\ ns)) \rightarrow min.$
$(T_{FWR}/2 - (1T_{CY} + 40\ ns)) \rightarrow max.$

13.5 Voltage Generation

There are two methods for LCD voltage generation, internal charge pump, or external resistor ladder.

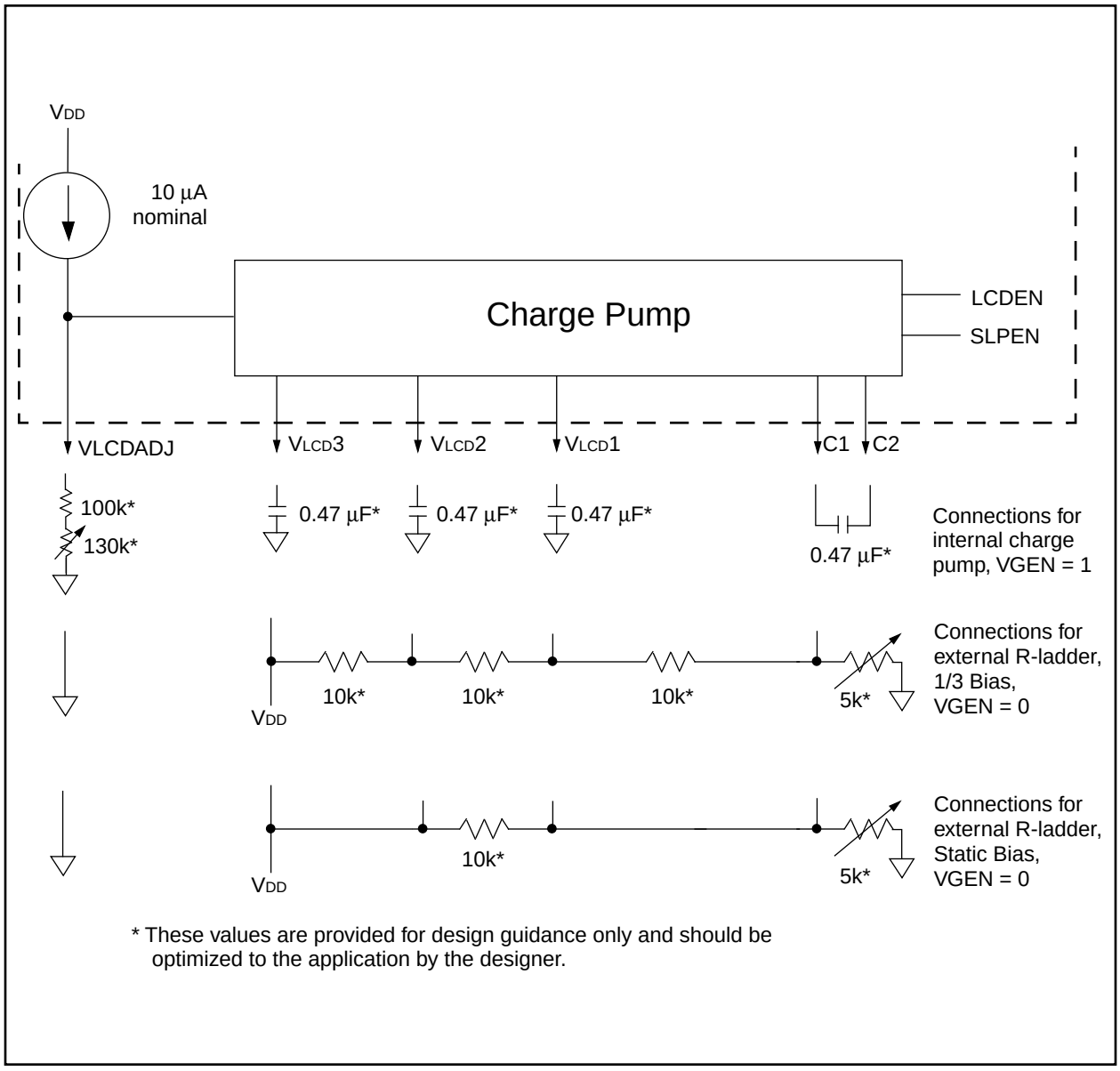
13.5.1 CHARGE PUMP

The LCD charge pump is shown in Figure 13-13. The 1.0V - 2.3V regulator will establish a stable base voltage from the varying battery voltage. This regulator is adjustable through the range by connecting a variable external resistor from VLCDADJ to ground. The potentiometer provides contrast adjustment for the LCD. This base voltage is connected to $V_{LCD}1$ on the charge pump. The charge pump boosts $V_{LCD}1$ into $V_{LCD}2$ = 2*$V_{LCD}1$ and $V_{LCD}3$ = 3 * $V_{LCD}1$. When the charge pump is not operating, Vlcd3 will be internally tied to V_{DD}. See the Electrical Specifications section for charge pump capacitor and potentiometer values.

13.5.2 EXTERNAL R-LADDER

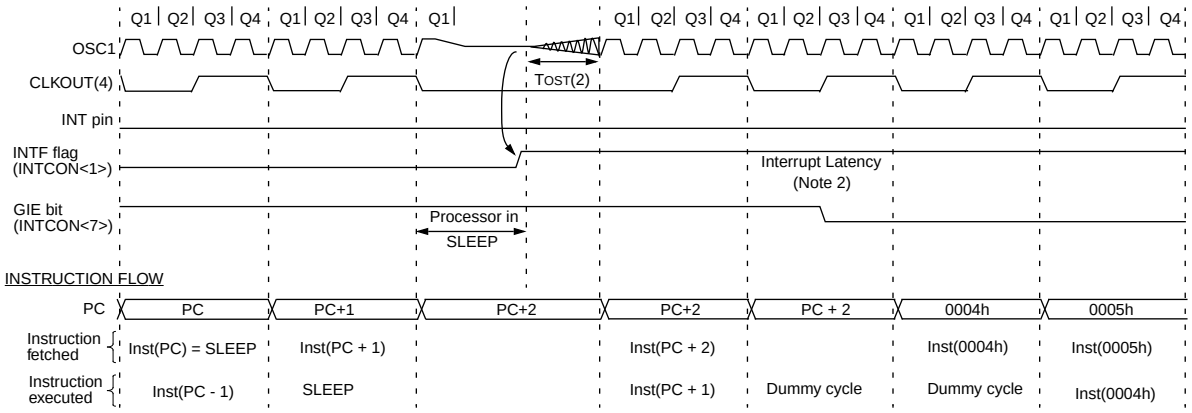
The LCD module can also use an external resistor ladder (R-Ladder) to generate the LCD voltages. Figure 13-13 shows external connections for static and 1/3 bias. The VGEN (LCDCON<4>) bit must be cleared to use an external R-Ladder.

FIGURE 13-13:CHARGE PUMP AND RESISTOR LADDER



* These values are provided for design guidance only and should be optimized to the application by the designer.

FIGURE 14-18:WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

14.9 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices.

14.10 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

14.11 In-Circuit Serial Programming

PIC16CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into program/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

FIGURE 14-19:TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION

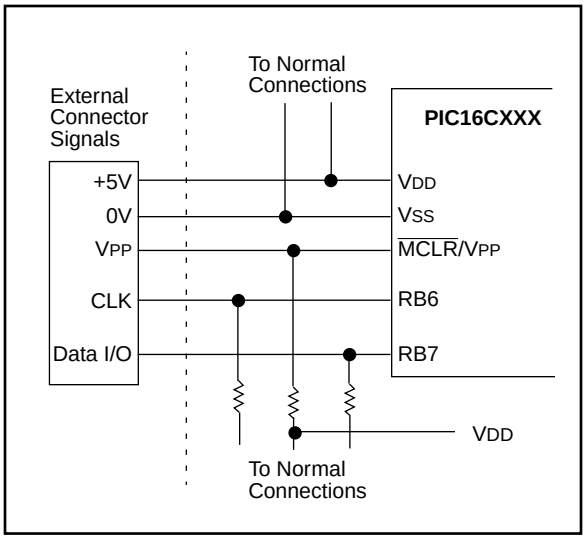


TABLE 15-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb	LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	**f, d**	Add W and f	1	00 0111 dfff ffff		C,DC,Z	1,2
ANDWF	**f, d**	AND W with f	1	00 0101 dfff ffff		Z	1,2
CLRF	**f**	Clear f	1	00 0001 lfff ffff		Z	2
CLRW	**-**	Clear W	1	00 0001 0xxx xxxx		Z	
COMF	**f, d**	Complement f	1	00 1001 dfff ffff		Z	1,2
DECF	**f, d**	Decrement f	1	00 0011 dfff ffff		Z	1,2
DECFSZ	**f, d**	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff			1,2,3
INCF	**f, d**	Increment f	1	00 1010 dfff ffff		Z	1,2
INCFSZ	**f, d**	Increment f, Skip if 0	1(2)	00 1111 dfff ffff			1,2,3
IORWF	**f, d**	Inclusive OR W with f	1	00 0100 dfff ffff		Z	1,2
MOVF	**f, d**	Move f	1	00 1000 dfff ffff		Z	1,2
MOVWF	**f**	Move W to f	1	00 0000 lfff ffff			
NOP	**-**	No Operation	1	00 0000 0xx0 0000			
RLF	**f, d**	Rotate Left f through Carry	1	00 1101 dfff ffff		C	1,2
RRF	**f, d**	Rotate Right f through Carry	1	00 1100 dfff ffff		C	1,2
SUBWF	**f, d**	Subtract W from f	1	00 0010 dfff ffff		C,DC,Z	1,2
SWAPF	**f, d**	Swap nibbles in f	1	00 1110 dfff ffff			1,2
XORWF	**f, d**	Exclusive OR W with f	1	00 0110 dfff ffff		Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	**f, b**	Bit Clear f	1	01 00bb bfff ffff			1,2
BSF	**f, b**	Bit Set f	1	01 01bb bfff ffff			1,2
BTFSC	**f, b**	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff			3
BTFSS	**f, b**	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff			3
LITERAL AND CONTROL OPERATIONS							
ADDLW	**k**	Add literal and W	1	11 111x kkkk kkkk		C,DC,Z	
ANDLW	**k**	AND literal with W	1	11 1001 kkkk kkkk		Z	
CALL	**k**	Call subroutine	2	10 0kkk kkkk kkkk			
CLRWDT	**-**	Clear Watchdog Timer	1	00 0000 0110 0100		$\overline{TO}$,$\overline{PD}$	
GOTO	**k**	Go to address	2	10 1kkk kkkk kkkk			
IORLW	**k**	Inclusive OR literal with W	1	11 1000 kkkk kkkk		Z	
MOVLW	**k**	Move literal to W	1	11 00xx kkkk kkkk			
RETFIE	**-**	Return from interrupt	2	00 0000 0000 1001			
RETLW	**k**	Return with literal in W	2	11 01xx kkkk kkkk			
RETURN	**-**	Return from Subroutine	2	00 0000 0000 1000			
SLEEP	**-**	Go into standby mode	1	00 0000 0110 0011		$\overline{TO}$,$\overline{PD}$	
SUBLW	**k**	Subtract W from literal	1	11 110x kkkk kkkk		C,DC,Z	
XORLW	**k**	Exclusive OR literal with W	1	11 1010 kkkk kkkk		Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

17.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55˚C to +125˚C
Storage temperature ..... -65˚C to +150˚C
Voltage on any pin with respect to VSS (except VDD, $\overline{MCLR}$, and RA4) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... -0.3V to +7.5V
Voltage on $\overline{MCLR}$ with respect to VSS ..... 0V to +14V
Voltage on RA4 with respect to Vss ..... 0V to +14V
Total power dissipation (Note 1) 1.0W
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin ..... 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ± 20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 10 mA
Maximum output current sourced by any I/O pin ..... 10 mA
Maximum current sunk by all Ports combined ..... 200 mA
Maximum current sourced by all Ports combined ..... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

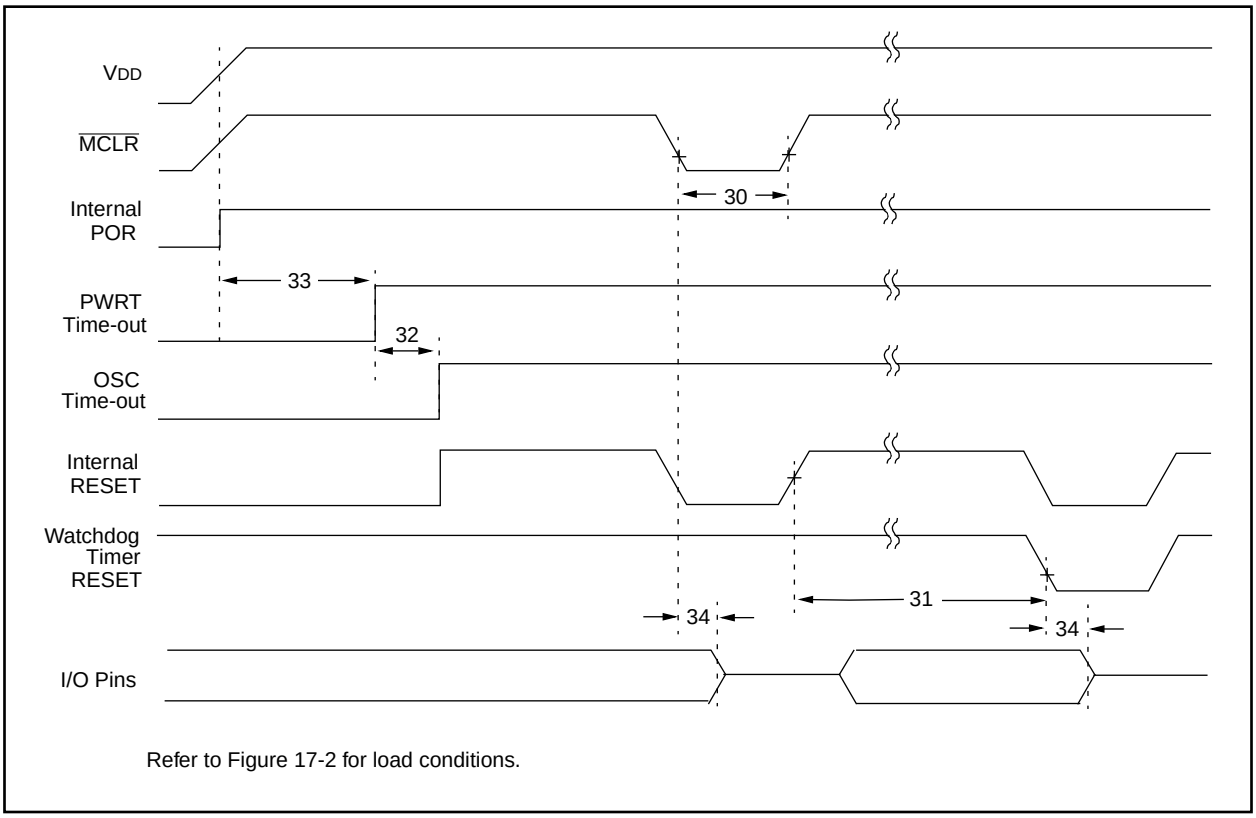
† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 17-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C923-04 PIC16C924-04	PIC16C923-08 PIC16C924-08	PIC16LC923-04 PIC16LC924-04	CL Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 3.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 7 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 8 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 7 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 8 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 22.5 µA typ. at 32 kHz, 4.0V IPD: 1.5 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	VDD: 2.5V to 6.0V IDD: 30 µA max. at 32 kHz, 3.0V IPD: 5 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 30 µA max. at 32 kHz, 3.0V IPD: 5 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications.
It is recommended that the user select the device type that ensures the specifications required.

FIGURE 17-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Refer to Figure 17-2 for load conditions.

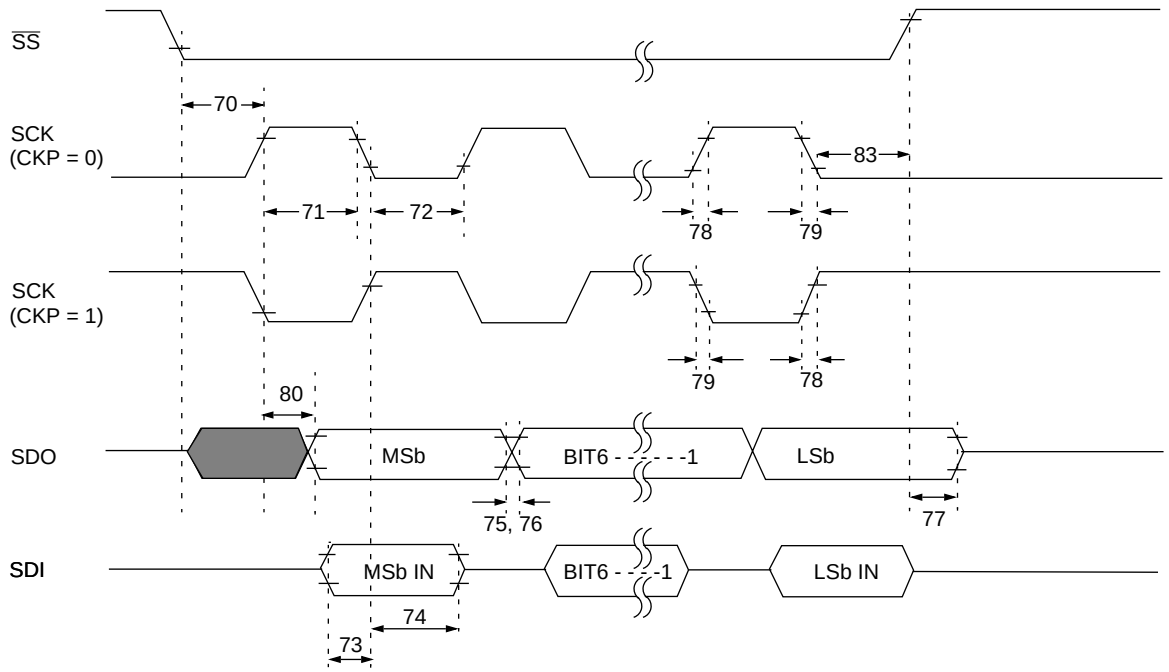
TABLE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40˚C to +85˚C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40˚C to +85˚C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.1	µs	

* These parameters are characterized but not tested.

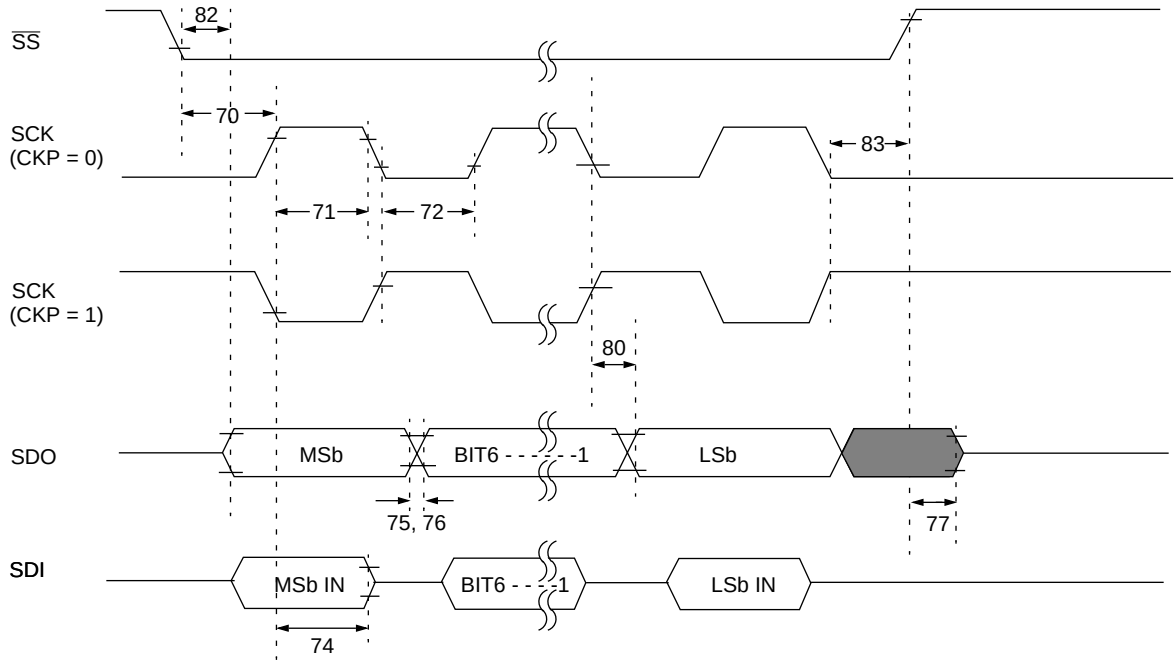
† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-10:SPI SLAVE MODE TIMING (CKE = 0)



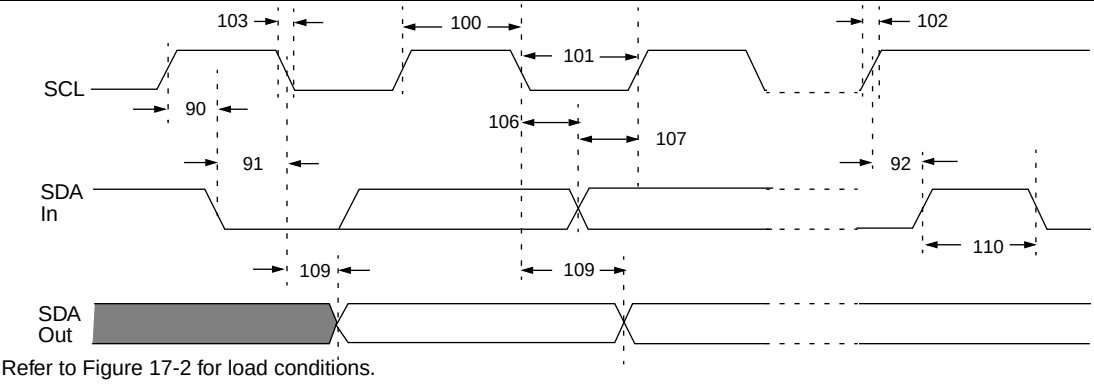
Refer to Figure 17-2 for load conditions.

FIGURE 17-11:SPI SLAVE MODE TIMING (CKE = 1)



Refer to Figure 17-2 for load conditions.

FIGURE 17-13:I²C BUS DATA TIMING



Refer to Figure 17-2 for load conditions.

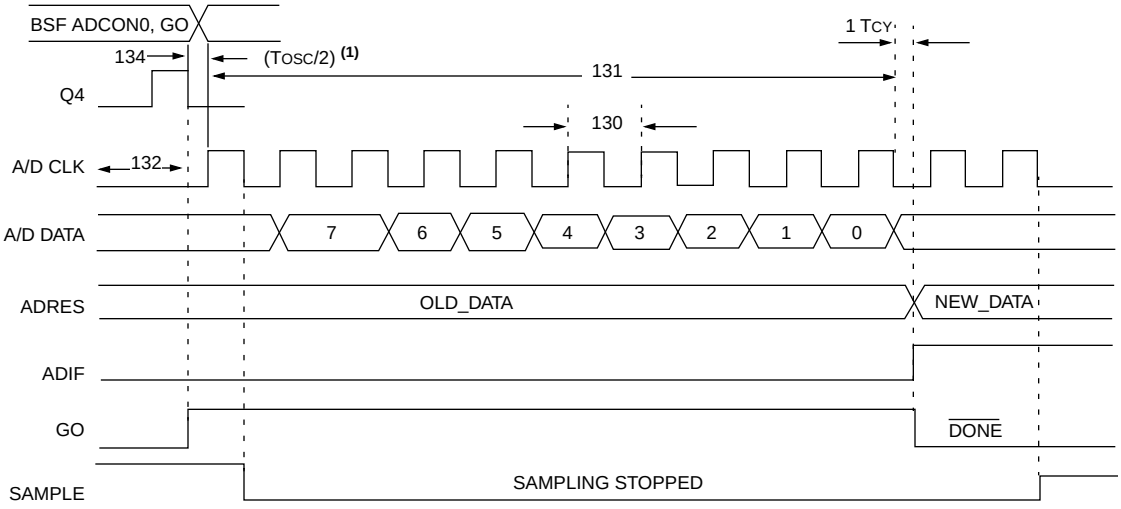
TABLE 17-11:I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
90*	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
91*	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	
92*	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
D102*	Cb	Bus capacitive loading		—	400	pF	

* Characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

FIGURE 17-14: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 17-13: A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16**C**924	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16**LC**924	2.0	—	—	µs	TOSC based, VREF full range
			PIC16**C**924	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16**LC**924	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	9.5	—	TAD	
132	TACQ	Acquisition time		Note 2	20	—	µs	
				5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D clock start		—	TOSC/2 §	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
135	TSWC	Switching from convert → sample time		1.5 §	—	—	TAD	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 12.1 for min conditions.

APPENDIX C: WHAT'S NEW

Figure 13-13 (Resistor Ladder and Charge Pump) in LCD Section.

Parameter D150 - Open Drain High Voltage.

DC and AC Characterization Graphs and Tables.

APPENDIX D: WHAT'S CHANGED

Various descriptions for clarity.

Example code for Changing prescaler assignment between Timer0 and the WDT.

The A/D section has many changes that provide greater clarification of A/D operation.

The Instruction Set has Q-cycle activity listings for every instruction.

The following Electrical Characteristic Parameter values have changed to:

D011 (Standard Voltage Devices, C)
Typical 22.5 µA
Max 48 µA

D022 (Standard Voltage Devices)
Typical 40 µA
Max 55 µA

D024 (Standard Voltage Devices)
Typical 33 µA
Max 60 µA

D001 (Extended Voltage Devices, LC)
Min 2.5 V

D011 (Extended Voltage Devices, LC)
Typical 13.5 µA
Max 30 µA

D022 (Extended Voltage Devices, LC)
Typical 36 µA
Max 50 µA

D024 (Extended Voltage Devices, LC)
Typical 15 µA
Max 29 µA

D030 (with TTL)
Max $0.5V_{DD}$ V (ENTIRE RANGE)
Max 0.8V V ($4.5V \leq V_{DD} \leq 5.5V$)

D201, D202

Deleted D210 and D211, D251, D253, D260, D271

D222
Min 5 kHz
Typical 15 kHz
Max 50 kHz

D223, D224 - units to ns.

Added D265 (VLCDADJ voltage limits.

Changed parameters:

12 - TckR 35 ns Typical

13 - TckF 35 ns Typical

15 - TioV2ckH Tosc + 200 ns Min

18 - TosH2ioL 200 ns Min (LC devices)

30 - TmcL 2 µs Min

34 - Tioz 2.1 µs Max

Timer0 and Timer1 External Clock Timings - Various.

53 - TccR,
54 - TccF

73 - TdiV2scH 50 ns Min

74 - TscH2diL 50 ns Min

Combined A/D specification tables for Standard and Extended Voltage devices.

PIC16C9XX PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery refer to the factory or the listed sales office.

PART NO. -XX X /XX XXX

Pattern:	QTP, SQTP, ROM Code or Special Requirements	
Package:	SP	= 64-pin Shrink PDIP
	PT	= TQFP
	CL	= 68-pin Windowed CERQUAD
	L	= PLCC
Temperature Range:	-	= 0°C to +70°C (T for Tape/Reel)
	I	= -40°C to +85°C (S for Tape/Reel)
Frequency Range:	04	= 200 kHz (PIC16C9XX-04)
	04	= 4 MHz
	08	= 8 MHz
Device	PIC16C9XX	:VDD range 4.0V to 6.0V
	PIC16C9XXT	:VDD range 4.0V to 6.0V (Tape/Reel)
	PIC16LC9XX	:VDD range 2.5V to 6.0V
	PIC16LC9XT	:VDD range 2.5V to 6.0V (Tape/Reel)

Examples

a) PIC16C924 - 04/P 301 Commercial Temp., PDIP Package, 4 MHz, normal VDD limits, QTP pattern #301

b) PIC16LC923 - 04/PT Commercial Temp., TQFP package, 4 MHz, extended VDD limits

c) PIC16C923 - 08I/CL Industrial Temp., Windowed CERQUAD package, 8 MHz, normal VDD limits

* CL Devices are UV erasable and can be programmed to any device configuration. CL Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.