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Details

Product Status	Not For New Designs
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08gt32acfbe

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3.6.4 Active BDM Enabled in Stop Mode

Entry into the active background mode from run mode is enabled if the ENBDM bit in BDCSCR is set. This register is described in the Chapter 15, "Development Support," section of this data sheet. If ENBDM is set when the CPU executes a STOP instruction, the system clocks to the background debug logic remain active when the MCU enters stop mode so background debug communication is still possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation. If the user attempts to enter either stop1 or stop2 with ENBDM set, the MCU will instead enter stop3.

Most background commands are not available in stop mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from stop and enter active background mode if the ENBDM bit is set. After the device enters background debug mode, all background commands are available. The table below summarizes the behavior of the MCU in stop when entry into the background debug mode is enabled.

Mode	PDC	PPDC	CPU, Digital Peripherals, Flash	RAM	ICG	ATD	Regulator	I/O Pins	RTI ¹
Stop3	Don't care	Don't care	Standby	Standby	Active	Disabled ²	Active	States held	Optionally on

Table 3-2. BDM Enabled Stop Mode Behavior

¹ The 1 kHz internal RTI clock is not available in stop3 with active BDM enabled.

² Either ATD stop mode or power-down mode depending on the state of ATDPU.

3.6.5 LVD Enabled in Stop Mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. If the LVD is enabled in stop by setting the LVDE and the LVDSE bits in SPMSC1 when the CPU executes a STOP instruction, then the voltage regulator remains active during stop mode. If the user attempts to enter either stop1 or stop2 with the LVD enabled for stop (LVDSE = 1), the MCU will instead enter stop3. The table below summarizes the behavior of the MCU in stop when the LVD is enabled.

Mode	PDC	PPDC	CPU, Digital Peripherals, Flash	RAM	ICG	ATD	Regulator	I/O Pins	RTI
Stop3	Don't care	Don't care	Standby	Standby	Standby	Disabled ¹	Active	States held	Optionally on

Either ATD stop mode or power-down mode depending on the state of ATDPU.

3.6.6 On-Chip Peripheral Modules in Stop Modes

When the MCU enters any stop mode, system clocks to the internal peripheral modules are stopped. Even in the exception case (ENBDM = 1), where clocks to the background debug logic continue to operate,

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to program the entire array through the single-wire background debug interface. Because no special voltages are needed for flash erase and programming operations, in-application programming is also possible through other software-controlled communication paths. For a more detailed discussion of in-circuit and in-application programming, refer to the *HCS08 Family Reference Manual, Volume I*, Freescale Semiconductor document order number HCS08RMv1/D.

4.4.1 Features

Features of the flash memory include:

- Flash Size
 - MC9S08GB60A/MC9S08GT60A 61268 bytes (120 pages of 512 bytes each)
 - MC9S08GB32A/MC9S08GT32A— 32768 bytes (64 pages of 512 bytes each)
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature
- Flexible block protection
- Security feature for flash and RAM
- Auto power-down for low-frequency read accesses

4.4.2 Program and Erase Times

Before any program or erase command can be accepted, the flash clock divider register (FCDIV) must be written to set the internal clock for the flash module to a frequency (f_{FCLK}) between 150 kHz and 200 kHz (see Table 4.6.1). This register can be written only once, so normally this write is done during reset initialization. FCDIV cannot be written if the access error flag, FACCERR in FSTAT, is set. The user must ensure that FACCERR is not set before writing to the FCDIV register. One period of the resulting clock ($1/f_{FCLK}$) is used by the command processor to time program and erase pulses. An integer number of these timing pulses is used by the command processor to complete a program or erase command.

Table 4-5 shows program and erase times. The bus clock frequency and FCDIV determine the frequency of FCLK (f_{FCLK}). The time for one cycle of FCLK is $t_{FCLK} = 1/f_{FCLK}$. The times are shown as a number of cycles of FCLK and as an absolute time for the case where $t_{FCLK} = 5 \ \mu$ s. Program and erase times shown include overhead for the command state machine and enabling and disabling of program and erase voltages.

Parameter	Cycles of FCLK	Time if FCLK = 200 kHz
Byte program	9	45 μs
Byte program (burst)	4	20 μs ¹
Page erase	4000	20 ms
Mass erase	20,000	100 ms

Table 4-5	. Program	and	Erase	Times
14010 1.0		~	=	

¹ Excluding start/end overhead



Chapter 5 Resets, Interrupts, and System Configuration

- Illegal opcode detect
- Background debug forced reset
- The reset pin ($\overline{\text{RESET}}$)
- Clock generator loss of lock and loss of clock reset

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status register. Whenever the MCU enters reset, the internal clock generator (ICG) module switches to self-clocked mode with the frequency of f_{Self} reset selected. The reset pin is driven low for 34 internal bus cycles where the internal bus frequency is half the ICG frequency. After the 34 cycles are completed, the pin is released and will be pulled up by the internal pullup resistor, unless it is held low externally. After the pin is released, it is sampled after another 38 cycles to determine whether the reset pin is the cause of the MCU reset.

5.4 Computer Operating Properly (COP) Watchdog

The COP watchdog is intended to force a system reset when the application software fails to execute as expected. To prevent a system reset from the COP timer (when it is enabled), application software must reset the COP timer periodically. If the application program gets lost and fails to reset the COP before it times out, a system reset is generated to force the system back to a known starting point. The COP watchdog is enabled by the COPE bit in SOPT (see Section 5.8.4, "System Options Register (SOPT)" for additional information). The COP timer is reset by writing any value to the address of SRS. This write does not affect the data in the read-only SRS. Instead, the act of writing to this address is decoded and sends a reset signal to the COP timer.

After any reset, the COP timer is enabled. This provides a reliable way to detect code that is not executing as intended. If the COP watchdog is not used in an application, it can be disabled by clearing the COPE bit in the write-once SOPT register. Also, the COPT bit can be used to choose one of two timeout periods (2¹⁸ or 2¹³ cycles of the bus rate clock). Even if the application will use the reset default settings in COPE and COPT, the user should still write to write-once SOPT during reset initialization to lock in the settings. That way, they cannot be changed accidentally if the application program gets lost.

The write to SRS that services (clears) the COP timer should not be placed in an interrupt service routine (ISR) because the ISR could continue to be executed periodically even if the main application program fails.

When the MCU is in active background mode, the COP timer is temporarily disabled.

5.5 Interrupts

Interrupts provide a way to save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so processing resumes where it left off before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such as an edge on the IRQ pin or a timer-overflow event. The debug module can also generate an SWI under certain circumstances.

If an event occurs in an enabled interrupt source, an associated read-only status flag will become set. The CPU will not respond until and unless the local interrupt enable is set to 1 to enable the interrupt. The I bit



Chapter 5 Resets, Interrupts, and System Configuration

5.8.2 System Reset Status Register (SRS)

This register includes six read-only status flags to indicate the source of the most recent reset. When a debug host forces reset by writing 1 to BDFR in the SBDFR register, none of the status bits in SRS will be set. Writing any value to this register address clears the COP watchdog timer without affecting the contents of this register. The reset state of these bits depends on what caused the MCU to reset.

	7	6	5	4	3	2	1	0					
R	POR	PIN	COP	ILOP	0	ICG	LVD	0					
W	Writing any value to SIMRS address clears COP watchdog timer.												
Power-on reset:	1	0	0	0	0	0	1	0					
Low-voltage reset:	U	0	0	0	0	0	1	0					
Any other reset:	0	Note ⁽¹⁾	Note ⁽¹⁾	Note ⁽¹⁾	0	Note ⁽¹⁾	0	0					

U = Unaffected by reset

¹ Any of these reset sources that are active at the time of reset will cause the corresponding bit(s) to be set; bits corresponding to sources that are not active at the time of reset will be cleared.

Figure 5-3. System Reset Status (SRS)

Table 5-3	. SRS	Field	Descri	ptions
-----------	-------	-------	--------	--------

Field	Description
7 POR	 Power-On Reset — Reset was caused by the power-on detection logic. Because the internal supply voltage was ramping up at the time, the low-voltage reset (LVD) status bit is also set to indicate that the reset occurred while the internal supply was below the LVD threshold. 0 Reset not caused by POR. 1 POR caused reset.
6 PIN	 External Reset Pin — Reset was caused by an active-low level on the external reset pin. 0 Reset not caused by external reset pin. 1 Reset came from external reset pin.
5 COP	 Computer Operating Properly (COP) Watchdog — Reset was caused by the COP watchdog timer timing out. This reset source may be blocked by COPE = 0. 0 Reset not caused by COP timeout. 1 Reset caused by COP timeout.
4 ILOP	 Illegal Opcode — Reset was caused by an attempt to execute an unimplemented or illegal opcode. The STOP instruction is considered illegal if stop is disabled by STOPE = 0 in the SOPT register. The BGND instruction is considered illegal if active background mode is disabled by ENBDM = 0 in the BDCSC register. 0 Reset not caused by an illegal opcode. 1 Reset caused by an illegal opcode.



Chapter 6 Parallel Input/Output

	7	6	5	4	3	2	1	0
R W	PTBSE7	PTBSE6	PTBSE5	PTBSE4	PTBSE3	PTBSE2	PTBSE1	PTBSE0
Reset	0	0	0	0	0	0	0	0

Figure 6-15. Data Direction for Port A (PTBSE)

Table 6-7. PTBSE Field Descriptions

Field	Description
7:0 PTBSE[7:0]	 Slew Rate Control Enable for Port B Bits — For port B pins that are outputs, these read/write control bits determine whether the slew rate controlled outputs are enabled. For port B pins that are configured as inputs, these bits are ignored. 0 Slew rate control disabled. 1 Slew rate control enabled.

_	7	6	5	4	3	2	1	0
R	PTBDD7	PTBDD6			PTBDD3			PTRODA
w		TTDDD0	T TOODS	T T D D D 4	1 10005	TTDDD2	וששטוו	
Reset	0	0	0	0	0	0	0	0

Figure 6-16. Data Direction for Port B (PTBDD)

Table 6-8. PTBDD Field Descriptions

Field	Description
7:0 PTBDD[7:0]	Data Direction for Port B Bits — These read/write bits control the direction of port B pins and what is read for PTBD reads.
	 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port B bit n and PTBD reads return the contents of PTBDn.



Chapter 6 Parallel Input/Output

	7	6	5	4	3	2	1	0
R W	PTGD7	PTGD6	PTGD5	PTGD4	PTGD3	PTGD2	PTGD1	PTGD0
Reset	0	0	0	0	0	0	0	0

Figure 6-33. Port PTG Data Register (PTGD)

Table 6-25. PTGD Field Descriptions

Field	Description
7:0 PTGD[7:0]	Port PTG Data Register Bits — For port G pins that are inputs, reads return the logic level on the pin. For port G pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port G pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTGD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

_	7	6	5	4	3	2	1	0
R W	PTGPE7	PTGPE6	PTGPE5	PTGPE4	PTGPE3	PTGPE2	PTGPE1	PTGPE0
Reset	0	0	0	0	0	0	0	0

Figure 6-34. Pullup Enable for Port G (PTGPE)

Table 6-26. PTGPE Field Descriptions

Field	Description
7:0	Pullup Enable for Port G Bits — For port G pins that are inputs, these read/write control bits determine whether
PTGPE[7:0]	internal pullup devices are enabled. For port G pins that are configured as outputs, these bits are ignored and
	the internal pullup devices are disabled.
	0 Internal pullup device disabled.
	1 Internal pullup device enabled.



8.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, all memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte linear address space so a 16-bit binary address can uniquely identify any memory location. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

8.3.1 Inherent Addressing Mode (INH)

In this addressing mode, operands needed to complete the instruction (if any) are located within CPU registers so the CPU does not need to access memory to get any operands.

8.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed 8-bit offset value is located in the memory location immediately following the opcode. During execution, if the branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address.

8.3.3 Immediate Addressing Mode (IMM)

In immediate addressing mode, the operand needed to complete the instruction is included in the object code immediately following the instruction opcode in memory. In the case of a 16-bit immediate operand, the high-order byte is located in the next memory location after the opcode, and the low-order byte is located in the next memory location after that.

8.3.4 Direct Addressing Mode (DIR)

In direct addressing mode, the instruction includes the low-order eight bits of an address in the direct page (0x0000-0x00FF). During execution a 16-bit address is formed by concatenating an implied 0x00 for the high-order half of the address and the direct address from the instruction to get the 16-bit address where the desired operand is located. This is faster and more memory efficient than specifying a complete 16-bit address for the operand.



Chapter 8 Central Processor Unit (S08CPUV2)

8.5 HCS08 Instruction Set Summary

Instruction Set Summary Nomenclature

The nomenclature listed here is used in the instruction descriptions in Table 8-2.

Operators

- () = Contents of register or memory location shown inside parentheses
- \leftarrow = Is loaded with (read: "gets")
- **&** = Boolean AND
- \mid = Boolean OR
- \oplus = Boolean exclusive-OR
- \times = Multiply
- \div = Divide
- : = Concatenate
- + = Add
- = Negate (two's complement)

CPU registers

- A = Accumulator
- CCR = Condition code register
 - H = Index register, higher order (most significant) 8 bits
 - X = Index register, lower order (least significant) 8 bits
 - PC = Program counter
- PCH = Program counter, higher order (most significant) 8 bits
- PCL = Program counter, lower order (least significant) 8 bits
 - SP = Stack pointer

Memory and addressing

- M = A memory location or absolute data, depending on addressing mode
- M:M + 0x0001= A 16-bit value in two consecutive memory locations. The higher-order (most significant) 8 bits are located at the address of M, and the lower-order (least significant) 8 bits are located at the next higher sequential address.

Condition code register (CCR) bits

- V = Two's complement overflow indicator, bit 7
- H = Half carry, bit 4
- I = Interrupt mask, bit 3
- N = Negative indicator, bit 2
- Z = Zero indicator, bit 1
- **C** = Carry/borrow, bit 0 (carry out of bit 7)

CCR activity notation

- = Bit not affected



Source	0	-	Effect on CCR						ess de	ode	and	rcles ¹
Form	Operation			н	I	N	z	С	Addr Mog	Opco	Opera	Bus Cy
ROR opr8a RORA RORX ROR oprx8,X ROR ,X ROR oprx8,SP	Rotate Right through Carry	b7 b0	¢	_	_	¢	\$	¢	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	5 1 1 5 4 6
RSP	Reset Stack Pointer	SP ← 0xFF (High Byte Not Affected)	-	-	-	-	-	-	INH	9C		1
RTI	Return from Interrupt	$\begin{array}{l} SP \leftarrow (SP) + 0x0001; \ Pull \ (CCR) \\ SP \leftarrow (SP) + 0x0001; \ Pull \ (A) \\ SP \leftarrow (SP) + 0x0001; \ Pull \ (X) \\ SP \leftarrow (SP) + 0x0001; \ Pull \ (PCH) \\ SP \leftarrow (SP) + 0x0001; \ Pull \ (PCL) \end{array}$	¢	¢	¢	\$	\$	¢	INH	80		9
RTS	Return from Subroutine	$SP \leftarrow SP + 0x0001; Pull (PCH)$ $SP \leftarrow SP + 0x0001; Pull (PCL)$	-	-	-	-	-	-	INH	81		6
SBC #opr8i SBC opr8a SBC opr16a SBC oprx16,X SBC oprx8,X SBC ,X SBC ,X SBC oprx16,SP SBC oprx8,SP	Subtract with Carry	$A \leftarrow (A) - (M) - (C)$	¢	_	_	¢	¢	¢	IMM DIR EXT IX2 IX1 IX SP2 SP1	A2 B2 C2 D2 E2 F2 9ED2 9EE2	ii dd hh II ee ff ff ee ff ff	2 3 4 3 3 5 4
SEC	Set Carry Bit	C ← 1	-	-	-	-	-	1	INH	99		1
SEI	Set Interrupt Mask Bit	l ← 1	-	-	1	-	-	-	INH	9B		1
STA opr8a STA opr16a STA oprx16,X STA oprx8,X STA ,X STA oprx16,SP STA oprx8,SP	Store Accumulator in Memory	M ← (A)	0	_	_	¢	¢		DIR EXT IX2 IX1 IX SP2 SP1	87 C7 D7 E7 F7 9ED7 9EE7	dd hh II ee ff ff ee ff ff	344 325 4
STHX opr8a STHX opr16a STHX oprx8,SP	Store H:X (Index Reg.)	(M:M + 0x0001) ← (H:X)	0	-	-	\$	¢	-	DIR EXT SP1	35 96 9EFF	dd hh ll ff	4 5 5
STOP	Enable Interrupts: Stop Processing Refer to MCU Documentation	I bit \leftarrow 0; Stop Processing	_	_	0	_	_	_	INH	8E		2+
STX opr8a STX opr16a STX oprx16,X STX oprx8,X STX ,X STX oprx16,SP STX oprx8,SP	Store X (Low 8 Bits of Index Register) in Memory	M ← (X)	0	_	_	\$	\$	Ι	DIR EXT IX2 IX1 IX SP2 SP1	BF CF DF EF 9EDF 9EEF	dd hh II ee ff ff ee ff ff	3 4 3 2 5 4
SUB #opr8i SUB opr8a SUB opr16a SUB oprx16,X SUB oprx8,X SUB ,X SUB oprx16,SP SUB oprx8,SP	Subtract	A ← (A) – (M)	¢	_	_	\$	\$	\$	IMM DIR EXT IX2 IX1 IX SP2 SP1	A0 B0 C0 D0 E0 F0 9ED0 9EE0	ii dd hh II ee ff ff ee ff ff	2 3 4 3 3 5 4
SWI	Software Interrupt	$\begin{array}{c} PC \leftarrow (PC) + 0x0001 \\ Push \ (PCL); \ SP \leftarrow (SP) - 0x0001 \\ Push \ (PCH); \ SP \leftarrow (SP) - 0x0001 \\ Push \ (X); \ SP \leftarrow (SP) - 0x0001 \\ Push \ (A); \ SP \leftarrow (SP) - 0x0001 \\ Push \ (CCR); \ SP \leftarrow (SP) - 0x0001 \\ I \leftarrow I; \\ PCH \leftarrow Interrupt \ Vector \ High \ Byte \\ PCL \leftarrow Interrupt \ Vector \ Low \ Byte \end{array}$	_	_	1	_	_	_	INH	83		11

Table 8-2	2. HCS08 In	struction	Set Summary	(Sheet	6 of 7)
				10	/

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Chapter 9 Keyboard Interrupt (S08KBIV1)



Note: Not all pins are bonded out in all packages. See Table 2-2 for complete details.



Figure 9-2. Block Diagram Highlighting KBI Module

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Timer/PWM (TPM)

Because the HCS08 MCU is an 8-bit architecture, a coherency mechanism is built into the timer counter for read operations. Whenever either byte of the counter is read (TPMxCNTH or TPMxCNTL), both bytes are captured into a buffer so when the other byte is read, the value will represent the other byte of the count at the time the first byte was read. The counter continues to count normally, but no new value can be read from either byte until both bytes of the old count have been read.

The main timer counter can be reset manually at any time by writing any value to either byte of the timer count TPMxCNTH or TPMxCNTL. Resetting the counter in this manner also resets the coherency mechanism in case only one byte of the counter was read before resetting the count.

10.5.2 Channel Mode Selection

Provided CPWMS = 0 (center-aligned PWM operation is not specified), the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and buffered edge-aligned PWM.

10.5.2.1 Input Capture Mode

With the input capture function, the TPM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TPM latches the contents of the TPM counter into the channel value registers (TPMxCnVH:TPMxCnVL). Rising edges, falling edges, or any edge may be chosen as the active edge that triggers an input capture.

When either byte of the 16-bit capture register is read, both bytes are latched into a buffer to support coherent 16-bit accesses regardless of order. The coherency sequence can be manually reset by writing to the channel status/control register (TPMxCnSC).

An input capture event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.

10.5.2.2 Output Compare Mode

With the output compare function, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter reaches the value in the channel value registers of an output compare channel, the TPM can set, clear, or toggle the channel pin.

In output compare mode, values are transferred to the corresponding timer channel value registers only after both 8-bit bytes of a 16-bit register have been written. This coherency sequence can be manually reset by writing to the channel status/control register (TPMxCnSC).

An output compare event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.

10.5.2.3 Edge-Aligned PWM Mode

This type of PWM output uses the normal up-counting mode of the timer counter (CPWMS = 0) and can be used when other channels in the same TPM are configured for input capture or output compare functions. The period of this PWM signal is determined by the setting in the modulus register (TPMxMODH:TPMxMODL). The duty cycle is determined by the setting in the timer channel value



Timer/PWM (TPM)

generation of 100 percent duty cycle is not necessary). This is not a significant limitation because the resulting period is much longer than required for normal applications.

TPMxMODH:TPMxMODL = 0000 is a special case that should not be used with center-aligned PWM mode. When CPWMS = 0, this case corresponds to the counter running free from 0000 through \$FFFF, but when CPWMS = 1 the counter needs a valid match to the modulus register somewhere other than at 0000 in order to change directions from up-counting to down-counting.

Figure 10-4 shows the output compare value in the TPM channel registers (multiplied by 2), which determines the pulse width (duty cycle) of the CPWM signal. If ELSnA = 0, the compare match while counting up forces the CPWM output signal low and a compare match while counting down forces the output high. The counter counts up until it reaches the modulo setting in TPMxMODH:TPMxMODL, then counts down until it reaches zero. This sets the period equal to two times TPMxMODH:TPMxMODL.



Figure 10-4. CPWM Period and Pulse Width (ELSnA = 0)

Center-aligned PWM outputs typically produce less noise than edge-aligned PWMs because fewer I/O pin transitions are lined up at the same system clock edge. This type of PWM is also required for some types of motor drives.

Because the HCS08 is a family of 8-bit MCUs, the settings in the timer channel registers are buffered to ensure coherent 16-bit updates and to avoid unexpected PWM pulse widths. Writes to any of the registers, TPMxMODH, TPMxMODL, TPMxCnVH, and TPMxCnVL, actually write to buffer registers. Values are transferred to the corresponding timer channel registers only after both 8-bit bytes of a 16-bit register have been written and the timer counter overflows (reverses direction from up-counting to down-counting at the end of the terminal count in the modulus register). This TPMxCNT overflow requirement only applies to PWM channels, not output compares.

Optionally, when TPMxCNTH:TPMxCNTL = TPMxMODH:TPMxMODL, the TPM can generate a TOF interrupt at the end of this count. The user can choose to reload any number of the PWM buffers, and they will all update simultaneously at the start of a new period.

Writing to TPMxSC cancels any values written to TPMxMODH and/or TPMxMODL and resets the coherency mechanism for the modulo registers. Writing to TPMxCnSC cancels any values written to the channel value registers and resets the coherency mechanism for TPMxCnVH:TPMxCnVL.

program has one full character time after RDRF is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (RDRF = 1), it gets the data from the receive data register by reading SCIxD. The RDRF flag is cleared automatically by a 2-step sequence which is normally satisfied in the course of the user's program that handles receive data. Refer to Section 11.3.4, "Interrupts and Status Flags," for more details about flag clearing.

11.3.3.1 Data Sampling Technique

The SCI receiver uses a 16× baud rate clock for sampling. The receiver starts by taking logic level samples at 16 times the baud rate to search for a falling edge on the RxD1 serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The 16× baud rate clock is used to divide the bit time into 16 segments labeled RT1 through RT16. When a falling edge is located, three more samples are taken at RT3, RT5, and RT7 to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a receive character.

The receiver then samples each bit time, including the start and stop bits, at RT8, RT9, and RT10 to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. In the case of the start bit, the bit is assumed to be 0 if at least two of the samples at RT3, RT5, and RT7 are 0 even if one or all of the samples taken at RT8, RT9, and RT10 are 1s. If any sample in any bit time (including the start and stop bits) in a character frame fails to agree with the logic level for that bit, the noise flag (NF) will be set when the received character is transferred to the receive data buffer.

The falling edge detection logic continuously looks for falling edges, and if an edge is detected, the sample clock is resynchronized to bit times. This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

In the case of a framing error, the receiver is inhibited from receiving any new characters until the framing error flag is cleared. The receive shift register continues to function, but a complete character cannot transfer to the receive data buffer if FE is still set.

11.3.3.2 Receiver Wakeup Operation

Receiver wakeup is a hardware mechanism that allows an SCI receiver to ignore the characters in a message that is intended for a different SCI receiver. In such a system, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up (RWU) control bit in SCIxC2. When RWU = 1, it inhibits setting of the status flags associated with the receiver, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force RWU to 0 so all receivers wake up in time to look at the first character(s) of the next message.



Field	Description
7 SPRF	 SPI Read Buffer Full Flag — SPRF is set at the completion of an SPI transfer to indicate that received data may be read from the SPI data register (SPI1D). SPRF is cleared by reading SPRF while it is set, then reading the SPI data register. No data available in the receive data buffer Data available in the receive data buffer
5 SPTEF	SPI Transmit Buffer Empty Flag — This bit is set when there is room in the transmit data buffer. It is cleared by reading SPI1S with SPTEF set, followed by writing a data value to the transmit buffer at SPI1D. SPI1S must be read with SPTEF = 1 before writing data to SPI1D or the SPI1D write will be ignored. SPTEF generates an SPTEF CPU interrupt request if the SPTIE bit in the SPI1C1 is also set. SPTEF is automatically set when a data byte transfers from the transmit buffer into the transmit shift register. For an idle SPI (no data in the transmit buffer or the shift register and no transfer in progress), data written to SPI1D is transferred to the shifter almost immediately so SPTEF is set within two bus cycles allowing a second 8-bit data value to be queued into the transmit buffer. After completion of the transfer of the value in the shift register, the queued value from the transmit buffer will automatically move to the shifter and SPTEF will be set to indicate there is room for new data in the transmit buffer. If no new data is waiting in the transmit buffer, SPTEF simply remains set and no data moves from the buffer not empty 1 SPI transmit buffer not empty
4 MODF	Master Mode Fault Flag — MODF is set if the SPI is configured as a master and the slave select input goes low, indicating some other SPI device is also configured as a master. The \overline{SS} pin acts as a mode fault error input only when MSTR = 1, MODFEN = 1, and SSOE = 0; otherwise, MODF will never be set. MODF is cleared by reading MODF while it is 1, then writing to SPI control register 1 (SPI1C1). 0 No mode fault error 1 Mode fault error detected

12.4.5 SPI Data Register (SPI1D)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-9. SPI Data Register (SPI1D)

Reads of this register return the data read from the receive data buffer. Writes to this register write data to the transmit data buffer. When the SPI is configured as a master, writing data to the transmit data buffer initiates an SPI transfer.

Data should not be written to the transmit data buffer unless the SPI transmit buffer empty flag (SPTEF) is set, indicating there is room in the transmit buffer to queue a new transmit byte.

Data may be read from SPI1D any time after SPRF is set and before another transfer is finished. Failure to read the data out of the receive data buffer before a new transfer ends causes a receive overrun condition and the data from the new transfer is lost.



Appendix A Electrical Characteristics

A.1 Introduction

This section contains electrical and timing specifications.

A.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table A-1 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Rating	Symbol	Value	Unit
Supply voltage	V _{DD}	-0.3 to +3.8	V
Maximum current into V _{DD}	I _{DD}	120	mA
Digital input voltage	V _{In}	–0.3 to V _{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins) ¹ , ² , ³	I _D	± 25	mA
Storage temperature range	T _{stg}	-55 to 150	°C

Table A-1. Absolute Maximum Ratings

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

 $^2\,$ All functional non-supply pins are internally clamped to V_{SS} and V_{DD}

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.



Figure A-13. IRQ Timing

A.9.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Function	Symbol	Min	Мах	Unit
External clock frequency	f _{TPMext}	dc	f _{Bus} /4	MHz
External clock period	t _{TPMext}	4	—	t _{cyc}
External clock high time	t _{clkh}	1.5	—	t _{cyc}
External clock low time	t _{ciki}	1.5	—	t _{cyc}
Input capture pulse width	t _{ICPW}	1.5	—	t _{cyc}

Table A-11. TPM Input Timing



Figure A-14. Timer External Clock



Figure A-15. Timer Input Capture Pulse





A.10 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, "Memory."

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase	V _{prog/erase}	1.8		3.6	V
Supply voltage for read operation 0 < f _{Bus} < 8 MHz 0 < f _{Bus} < 20 MHz	V _{Read}	1.8 2.08		3.6 3.6	V
Internal FCLK frequency ¹	f _{FCLK}	150		200	kHz
Internal FCLK period (1/FCLK)	t _{Fcyc}	5		6.67	μs
Byte program time (random location) ⁽²⁾	t _{prog}	9			t _{Fcyc}
Byte program time (burst mode) ⁽²⁾	t _{Burst}	4			t _{Fcyc}
Page erase time ²	t _{Page}	4000			t _{Fcyc}
Mass erase time ⁽²⁾	t _{Mass}	20,000			t _{Fcyc}
Program/erase endurance ³ T_L to $T_H = -40^{\circ}C$ to + 85°C $T = 25^{\circ}C$		10,000	100,000		cycles
Data retention ⁴	t _{D_ret}	15	100	—	years

Table A-13. Flash Characteristics

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

- ³ Typical endurance for flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*
- ⁴ Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*





DETAIL M PIN 1 BACKSIDE IDENTIFIER OPTION

DETAIL M PIN 1 BACKSIDE IDENTIFIER OPTION



DETAIL T

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TITLE: THERMALLY ENHANCED	QUAD	DOCUMENT NO): 98ARH99048A	REV: E	
FLAT NON-LEADED PACKA	CASE NUMBER	: 1314–04	20 APR 2005		
48 IERMINAL, 0.5 PITCH (7	/ X 7 X 1)	STANDARD: JE	DEC-MO-220 VKKD-2	2	