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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	-
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2040nsn1flb

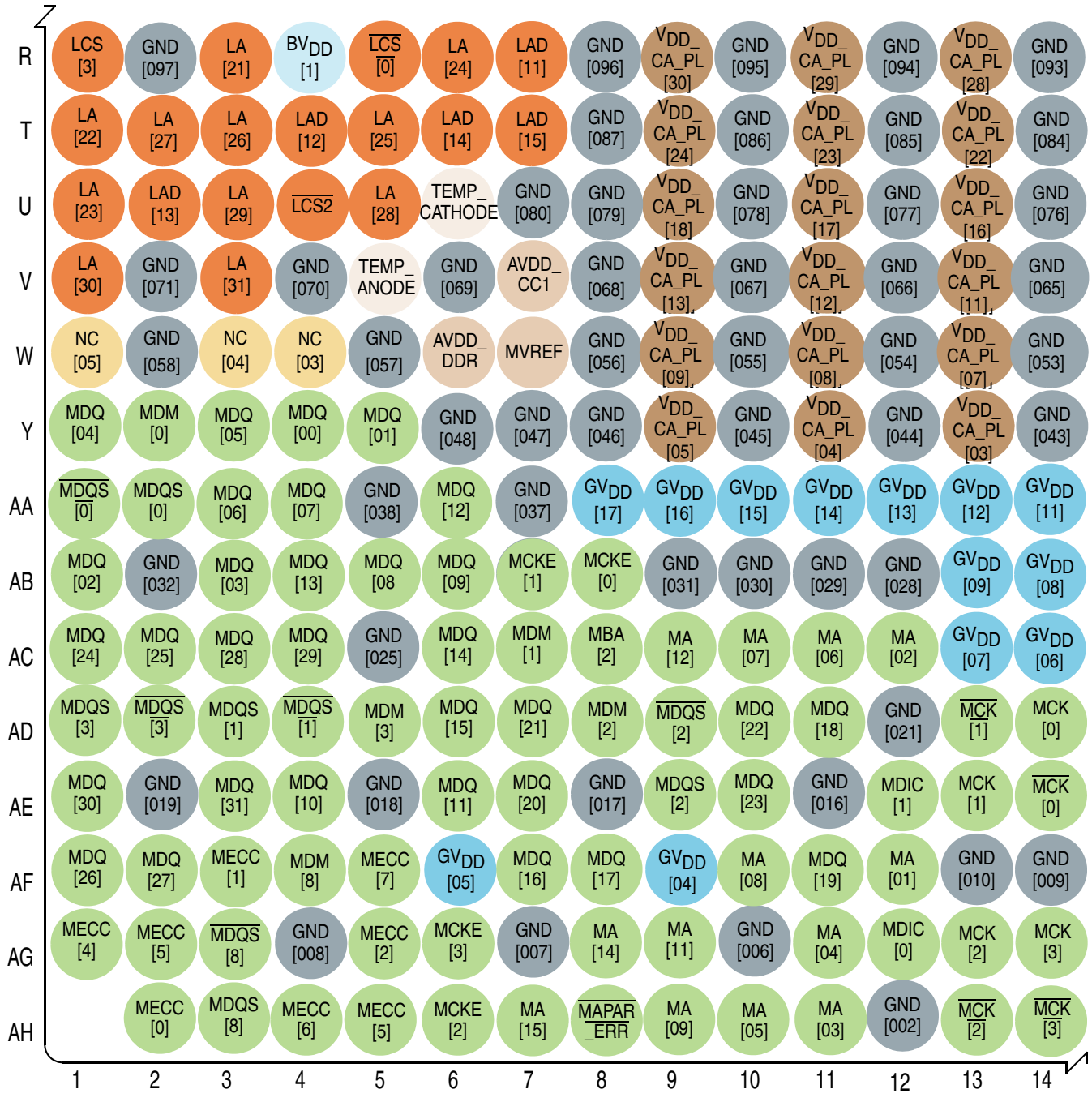


Figure 5. 780 BGA Ball Map Diagram (Detail View C)

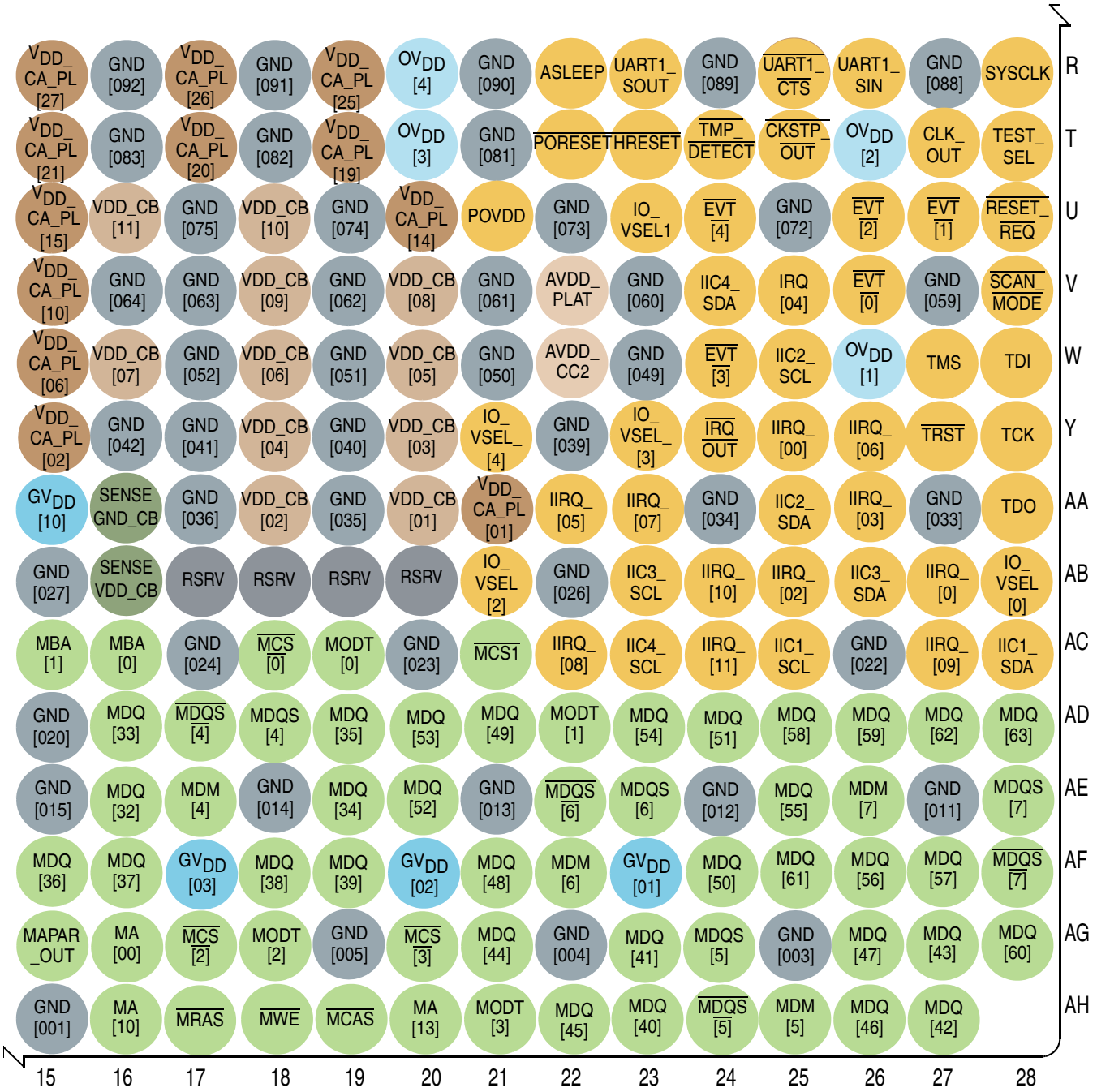


Figure 6. 780 BGA Ball Map Diagram (Detail View D)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ29	Data	AC4	I/O	GV_{DD}	—
MDQ30	Data	AE1	I/O	GV_{DD}	—
MDQ31	Data	AE3	I/O	GV_{DD}	—
MDQ32	Data	AE16	I/O	GV_{DD}	—
MDQ33	Data	AD16	I/O	GV_{DD}	—
MDQ34	Data	AE19	I/O	GV_{DD}	—
MDQ35	Data	AD19	I/O	GV_{DD}	—
MDQ36	Data	AF15	I/O	GV_{DD}	—
MDQ37	Data	AF16	I/O	GV_{DD}	—
MDQ38	Data	AF18	I/O	GV_{DD}	—
MDQ39	Data	AF19	I/O	GV_{DD}	—
MDQ40	Data	AH23	I/O	GV_{DD}	—
MDQ41	Data	AG23	I/O	GV_{DD}	—
MDQ42	Data	AH27	I/O	GV_{DD}	—
MDQ43	Data	AG27	I/O	GV_{DD}	—
MDQ44	Data	AG21	I/O	GV_{DD}	—
MDQ45	Data	AH22	I/O	GV_{DD}	—
MDQ46	Data	AH26	I/O	GV_{DD}	—
MDQ47	Data	AG26	I/O	GV_{DD}	—
MDQ48	Data	AF21	I/O	GV_{DD}	—
MDQ49	Data	AD21	I/O	GV_{DD}	—
MDQ50	Data	AF24	I/O	GV_{DD}	—
MDQ51	Data	AD24	I/O	GV_{DD}	—
MDQ52	Data	AE20	I/O	GV_{DD}	—
MDQ53	Data	AD20	I/O	GV_{DD}	—
MDQ54	Data	AD23	I/O	GV_{DD}	—
MDQ55	Data	AE25	I/O	GV_{DD}	—
MDQ56	Data	AF26	I/O	GV_{DD}	—
MDQ57	Data	AF27	I/O	GV_{DD}	—
MDQ58	Data	AD25	I/O	GV_{DD}	—
MDQ59	Data	AD26	I/O	GV_{DD}	—
MDQ60	Data	AG28	I/O	GV_{DD}	—
MDQ61	Data	AF25	I/O	GV_{DD}	—
MDQ62	Data	AD27	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LA19	Address	P3	I/O	BV_{DD}	31
LA20	Address	P2	I/O	BV_{DD}	31
LA21	Address	R3	I/O	BV_{DD}	31
LA22	Address	T1	I/O	BV_{DD}	31
LA23	Address	U1	I/O	BV_{DD}	3
LA24	Address	R6	I/O	BV_{DD}	3
LA25	Address	T5	I/O	BV_{DD}	31
LA26	Address	T3	I/O	BV_{DD}	3, 29
LA27	Address	T2	O	BV_{DD}	—
LA28	Address	U5	I/O	BV_{DD}	—
LA29	Address	U3	I/O	BV_{DD}	—
LA30	Address	V1	I/O	BV_{DD}	—
LA31	Address	V3	I/O	BV_{DD}	—
LDP0	Data Parity	L3	I/O	BV_{DD}	—
LDP1	Data Parity	M1	I/O	BV_{DD}	—
$\overline{\text{LCS0}}$	Chip Selects	R5	O	BV_{DD}	5
$\overline{\text{LCS1}}$	Chip Selects	P7	O	BV_{DD}	5
$\overline{\text{LCS2}}$	Chip Selects	U4	O	BV_{DD}	5
$\overline{\text{LCS3}}$	Chip Selects	R1	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write Enable	M6	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write Enable	M3	O	BV_{DD}	—
LBCTL	Buffer Control	P1	O	BV_{DD}	—
LALE	Address Latch Enable	N6	I/O	BV_{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	L5	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	K1	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	L6	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose LIne 3/ LFWP_B—FCM	J3	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	L2	I/O	BV_{DD}	36
LGPL5	UPM General Purpose Line 5 / Amux	J1	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	M4	O	BV_{DD}	—
LCLK1	Local Bus Clock	N7	O	BV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{EVT8}}$/GPIO29/IRQ11	Event 8	AC24	I/O	OV_{DD}	—
$\overline{\text{EVT9}}$/$\overline{\text{IRQ\_OUT}}$	Event 9	Y24	I/O	OV_{DD}	—
M1DVAL/LB_DVAL/IIC3_SCL/GPIO16/ $\overline{\text{SDHC\_CD}}$/$\overline{\text{DMA1\_DACK0}}$	Debug Data Valid	AB23	O	OV_{DD}	—
MSRCID0/LB_SRCID0/IIC3_SDA/GPIO17/ $\overline{\text{DMA\_DDONE0}}$/SDHC_WP	Debug Source ID 0	AB26	O	OV_{DD}	4, 31
MSRCID1/LB_MSRCID1/$\overline{\text{EVT5}}$/IIC4_SCL/ LB_SRCID1/GPIO18/$\overline{\text{DMA1\_DREQ0}}$	Debug Source ID 1	AC23	O	OV_{DD}	—
MSRCID2/LB_SRCID2/$\overline{\text{EVT6}}$/IIC4_SDA/ LB_SRCID2/GPIO19	Debug Source ID 2	V24	O	OV_{DD}	—
CLK_OUT	Clock Out	T27	O	OV_{DD}	6
Clock					
RTC	Real Time Clock	P28	I	OV_{DD}	—
SYSCLK	System Clock	R28	I	OV_{DD}	—
JTAG					
TCK	Test Clock	Y28	I	OV_{DD}	—
TDI	Test Data In	W28	I	OV_{DD}	7
TDO	Test Data Out	AA28	O	OV_{DD}	6
TMS	Test Mode Select	W27	I	OV_{DD}	7
$\overline{\text{TRST}}$	Test Reset	Y27	I	OV_{DD}	7
DFT					
$\overline{\text{SCAN\_MODE}}$	Scan Mode	V28	I	OV_{DD}	35
TEST_SEL	Test Mode Select	T28	I	OV_{DD}	12, 26
Power Management					
ASLEEP	Asleep	R22	O	OV_{DD}	31
Input /Output Voltage Select					
IO_VSEL0	I/O Voltage Select	AB28	I	OV_{DD}	27
IO_VSEL1	I/O Voltage Select	U23	I	OV_{DD}	27
IO_VSEL2	I/O Voltage Select	AB21	I	OV_{DD}	27
IO_VSEL3	I/O Voltage Select	Y23	I	OV_{DD}	27
IO_VSEL4	I/O Voltage Select	Y21	I	OV_{DD}	27
Power and Ground Signals					
GND168	Ground	A23	—	—	—
GND167	Ground	B23	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
USB1_AGND01	USB1 PHY Transceiver GND	M28	—	—	—
USB2_AGND06	USB2 PHY Transceiver GND	J22	—	—	—
USB2_AGND05	USB2 PHY Transceiver GND	J24	—	—	—
USB2_AGND04	USB2 PHY Transceiver GND	J26	—	—	—
USB2_AGND03	USB2 PHY Transceiver GND	K25	—	—	—
USB2_AGND02	USB2 PHY Transceiver GND	L25	—	—	—
USB2_AGND01	USB2 PHY Transceiver GND	M26	—	—	—
OVDD06	General I/O Supply	N20	—	OV_{DD}	—
OVDD05	General I/O Supply	P20	—	OV_{DD}	—
OVDD04	General I/O Supply	R20	—	OV_{DD}	—
OVDD03	General I/O Supply	T20	—	OV_{DD}	—
OVDD02	General I/O Supply	T26	—	OV_{DD}	—
OVDD01	General I/O Supply	W26	—	OV_{DD}	—
CVDD2	eSPI and eSDHC Supply	K20	—	CV_{DD}	—
CVDD1	eSPI and eSDHC Supply	M20	—	CV_{DD}	—
GVDD17	DDR Supply	AA8	—	GV_{DD}	—
GVDD16	DDR Supply	AA9	—	GV_{DD}	—
GVDD15	DDR Supply	AA10	—	GV_{DD}	—
GVDD14	DDR Supply	AA11	—	GV_{DD}	—
GVDD13	DDR Supply	AA12	—	GV_{DD}	—
GVDD12	DDR Supply	AA13	—	GV_{DD}	—
GVDD11	DDR Supply	AA14	—	GV_{DD}	—
GVDD10	DDR Supply	AA15	—	GV_{DD}	—
GVDD09	DDR Supply	AB13	—	GV_{DD}	—
GVDD08	DDR Supply	AB14	—	GV_{DD}	—
GVDD07	DDR Supply	AC13	—	GV_{DD}	—
GVDD06	DDR Supply	AC14	—	GV_{DD}	—
GVDD05	DDR Supply	AF6	—	GV_{DD}	—
GVDD04	DDR Supply	AF9	—	GV_{DD}	—
GVDD03	DDR Supply	AF17	—	GV_{DD}	—
GVDD02	DDR Supply	AF20	—	GV_{DD}	—
GVDD01	DDR Supply	AF23	—	GV_{DD}	—
BVDD07	Local Bus Supply	J7	—	BV_{DD}	—
BVDD06	Local Bus Supply	K7	—	BV_{DD}	—

While VDD is ramping, current may be supplied from VDD through the chip to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

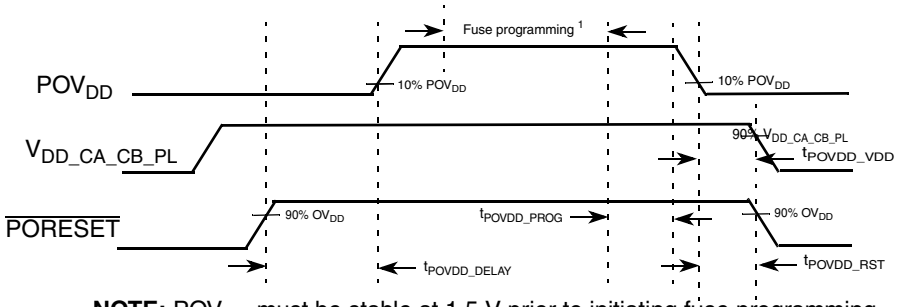
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to $V_{DD\_CA\_CB\_PL}$ ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before $V_{DD\_CA\_CB\_PL}$ is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{PORESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{PORESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the device PLLs, at allowable voltage levels.

Table 8. Device AV_{DD} Power Dissipation

AV_{DD}s	Typical	Maximum	Unit	Note
AV_{DD_DDR}	5	15	mW	1
AV_{DD_CC1}				
AV_{DD_CC2}				
AV_{DD_PLAT}				
AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}				
USB_V_{DD_1P0}	—	10	mW	3

Note:

1. $V_{DD\_CA\_CB\_PL}$, T_A = 80°C, T_J = 105°C
2. SV_{DD} = 1.0 V, T_A = 80°C, T_J = 105°C
3. USB_V_{DD_1P0} = 1.0V, T_A = 80°C, T_J = 105°C

This table shows the estimated power dissipation on the POV_{DD} supply for the chip at allowable voltage levels.

Table 9. POV_{DD} Power Dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the device, at allowable voltage levels.

Table 10. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Notes
V_{DD_LP} (Device on, 105C)	1.5	mW	1
V_{DD_LP} (Device off, 70C)	195	uW	2
V_{DD_LP} (Device off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When the device is off, V_{DD_LP} may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC, which switches V_{DD_LP} to battery when the SoC is powered down. See the Trust Architecture chapter in the device reference manual for more information.

2.5 Thermal

Table 11. Package Thermal Characteristics [6]

Rating	Board	Symbol	Value	Unit	Note
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	21	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	15	°C/W	1, 3

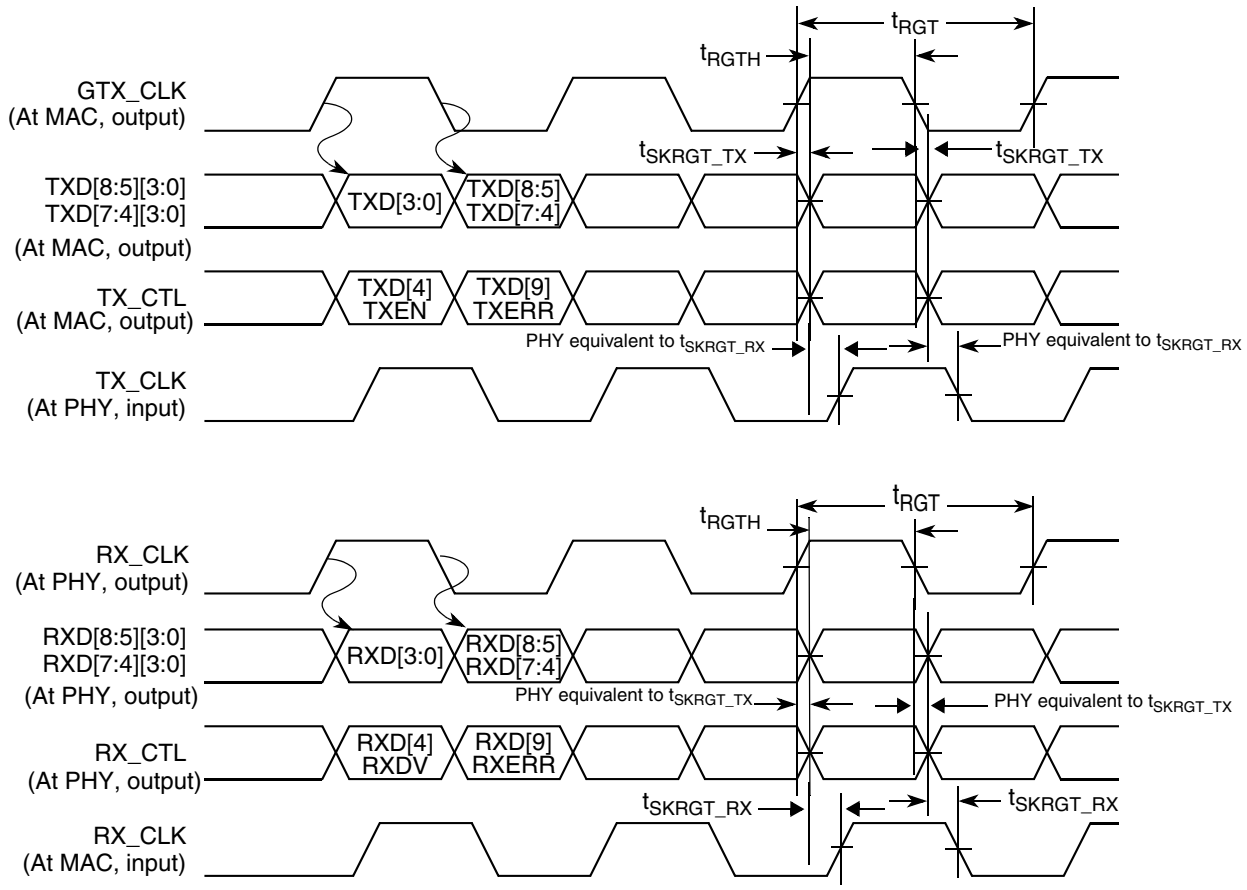


Figure 16. RGMII AC Timing and Multiplexing Diagrams

2.12.3 Ethernet Management Interface

This section discusses the electrical characteristics for the EMI1 interfaces. EMI1 is the PHY management interface controlled by the MDIO controller associated with Frame Manager 1 1GMAC–1.

2.12.3.1 Ethernet Management Interface DC Electrical Characteristics

The Ethernet management interface is defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 38. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

2.13 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.13.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface at USB_VDD_3P3 = 3.3 V.

Table 44. USB DC Electrical Characteristics (USB_V_{DD}_3P3 = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage[1]	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (USB_V_{IN}_3P3 = 0 V or USB_V_{IN}_3P3 = USB_V_{DD}_3P3)	I_{IN}	—	±40	μA	2
Output high voltage (USB_V_{DD}_3P3 = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	
Output low voltage (USB_V_{DD}_3P3 = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_V_{IN}_3P3 values found in Table 3.
2. The symbol USB_V_{IN}_3P3, in this case, represents the USB_V_{IN}_3P3 symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.13.2 USB AC Electrical Specifications

This table provides the USB clock input (USB*n*_CLKIN) AC timing specifications.

Table 45. USB_CLK_IN AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Note
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	—	MHz	—
Rise/Fall time	Measured between 10% and 90%	t_{USRF}	—	—	6	ns	1
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%	—
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%	—
Total input jitter/time interval error	RMS value measured with a second-order, high-pass filter of 500-kHz bandwidth	t_{CLK_PJ}	—	—	5	ps	—

Note:

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Table 56. I^2C DC Electrical Characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–40	40	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.18.2 I^2C AC Electrical Specifications

This table provides the I^2C AC timing specifications.

Table 57. I^2C AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V.

Table 58. GPIO DC Electrical Characteristics (CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max L/OV_{IN} respective values found in Table 3.
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} or LV_{DD} = 2.5 V.

Table 59. GPIO DC Electrical Characteristics (CV_{DD} or LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or a receiver input (SD_RX*n* and $\overline{\text{SD\_RX}n}$). Each signal swings between A volts and B volts where A > B.

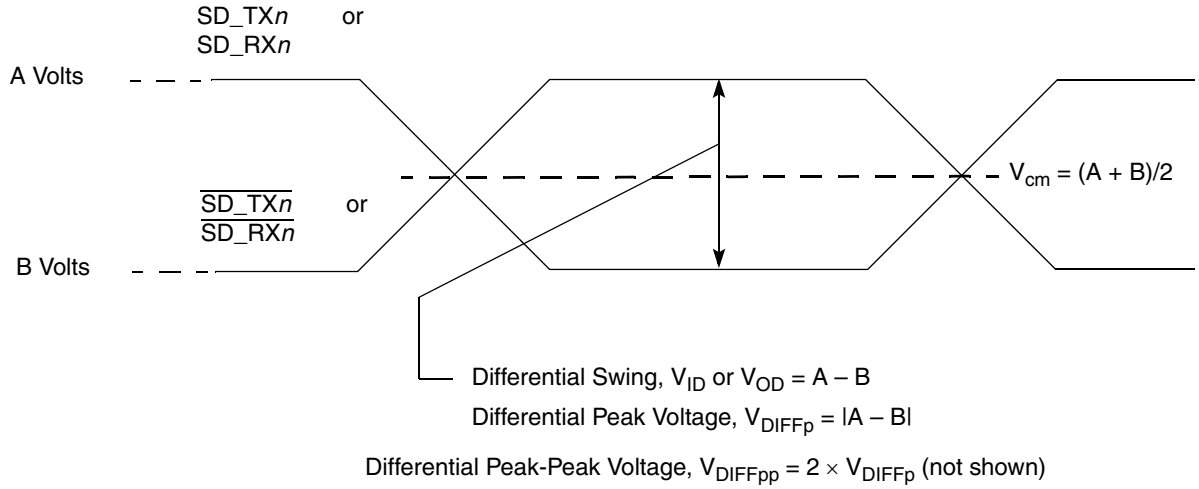


Figure 32. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX*n*, $\overline{\text{SD\_TX}n}$, SD_RX*n* and $\overline{\text{SD\_RX}n}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**):

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn} - V_{\overline{SD\_TXn}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**):

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn} - V_{\overline{SD\_RXn}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}n}$, for example) from the non-inverting signal ($\overline{\text{SD\_TX}n}$, for example) within a differential pair. There is

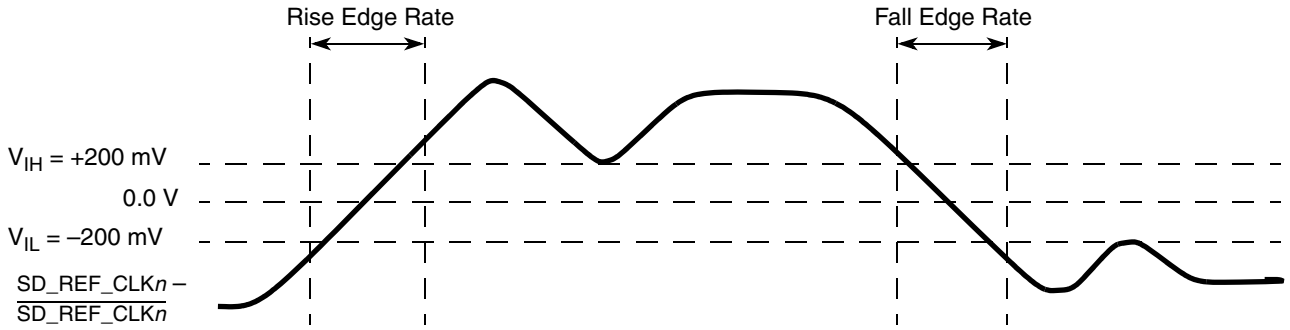


Figure 37. Differential Measurement Points for Rise and Fall Time

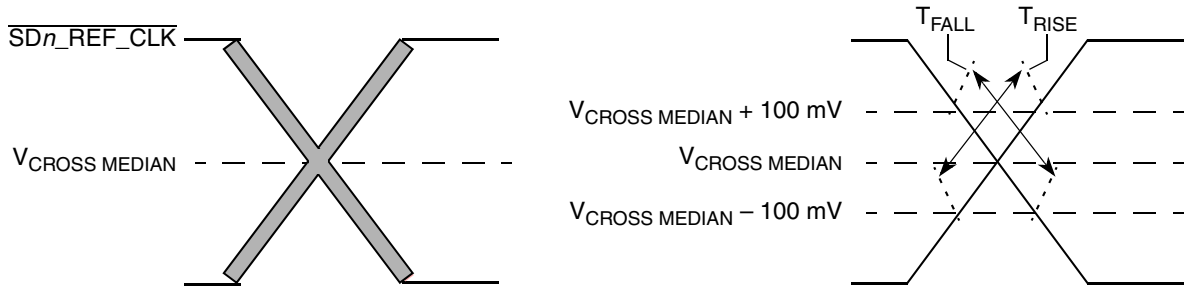


Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 Spread Spectrum Clock

SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

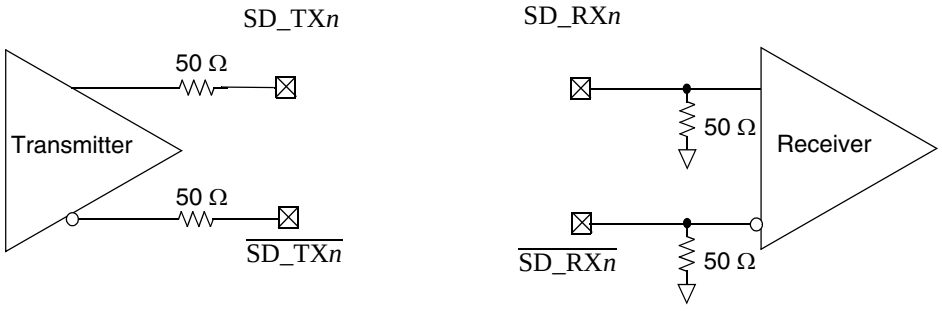


Figure 39. SerDes Transmitter and Receiver Reference Circuits

Table 69. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input AC Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture

Note:

1. No test load is necessarily associated with this value.

2.20.4.6 Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in this figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

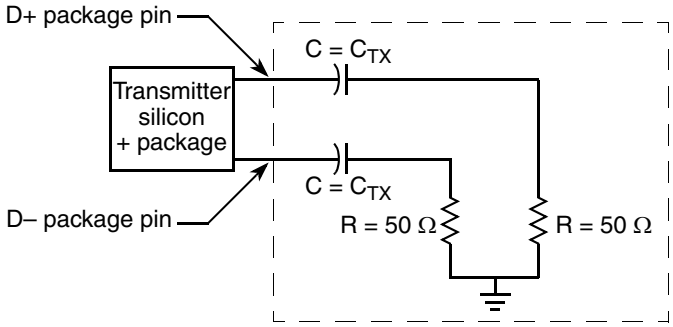


Figure 40. Test/Measurement Load

2.20.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125, and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

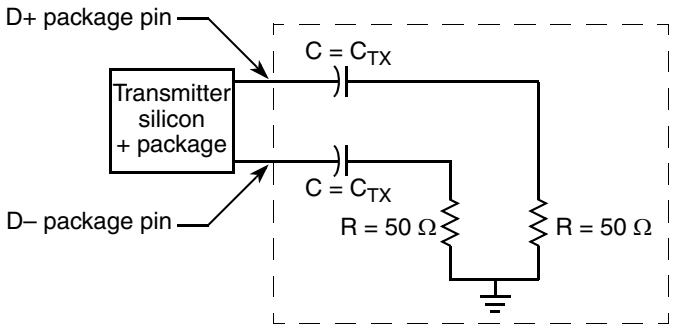


Figure 46. SGMII AC Test/Measurement Load

2.20.8.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 92. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Note:
1. Measured at receiver
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 System Clocking

This section describes the PLL configuration of the device.

This device includes six PLLs, as follows:

- There are two selectable core cluster PLLs that generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL; core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3,

EC*n*_GTX_CLK125 is a 125-MHz input clock on the dTSEC ports. If the dTSEC ports are not used for RGMII, the EC*n*_GTX_CLK125 input can be tied off to GND.

If RCW field I2C = 0b0100 or 0b0101 (RCW bits 354–357), the SDHC_WP and $\overline{\text{SDHC\_CD}}$ input signals are enabled for external use. If SDHC_WP and $\overline{\text{SDHC\_CD}}$ are selected and not used, they must be externally pulled low such that SDHC_WP = 0 (write enabled) and $\overline{\text{SDHC\_CD}}$ = 0 (card detected). If RCW field I2C ≠ 0b0100 or 0b0101, thereby selecting either I2C3 or GPIO functionality, SDHC_WP and $\overline{\text{SDHC\_CD}}$ are internally driven such that SDHC_WP = write enabled and $\overline{\text{SDHC\_CD}}$ = card detected and the selected I2C3 or GPIO external pin functionality may be used.

$\overline{\text{TMP\_DETECT}}$ pin and $\overline{\text{LP\_TMP DETECT}}$ pin are active low input to the Security Monitor (refer to the “Secure Boot and Trust Architecture” chapter of the chip reference manual). If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. A 1K pulldown resistor strongly recommended. If Trust is used without tamper sensors, tie high.VDD_LP must be connected even if Low Power features aren’t used. Otherwise, the LP_Section will generate internal errors that will prevent the high power trust section from reaching Trusted/Secure state.

3.6.1 Legacy JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 55. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 55 allows the COP port to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well.

The COP interface has a standard header, shown in Figure 54, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

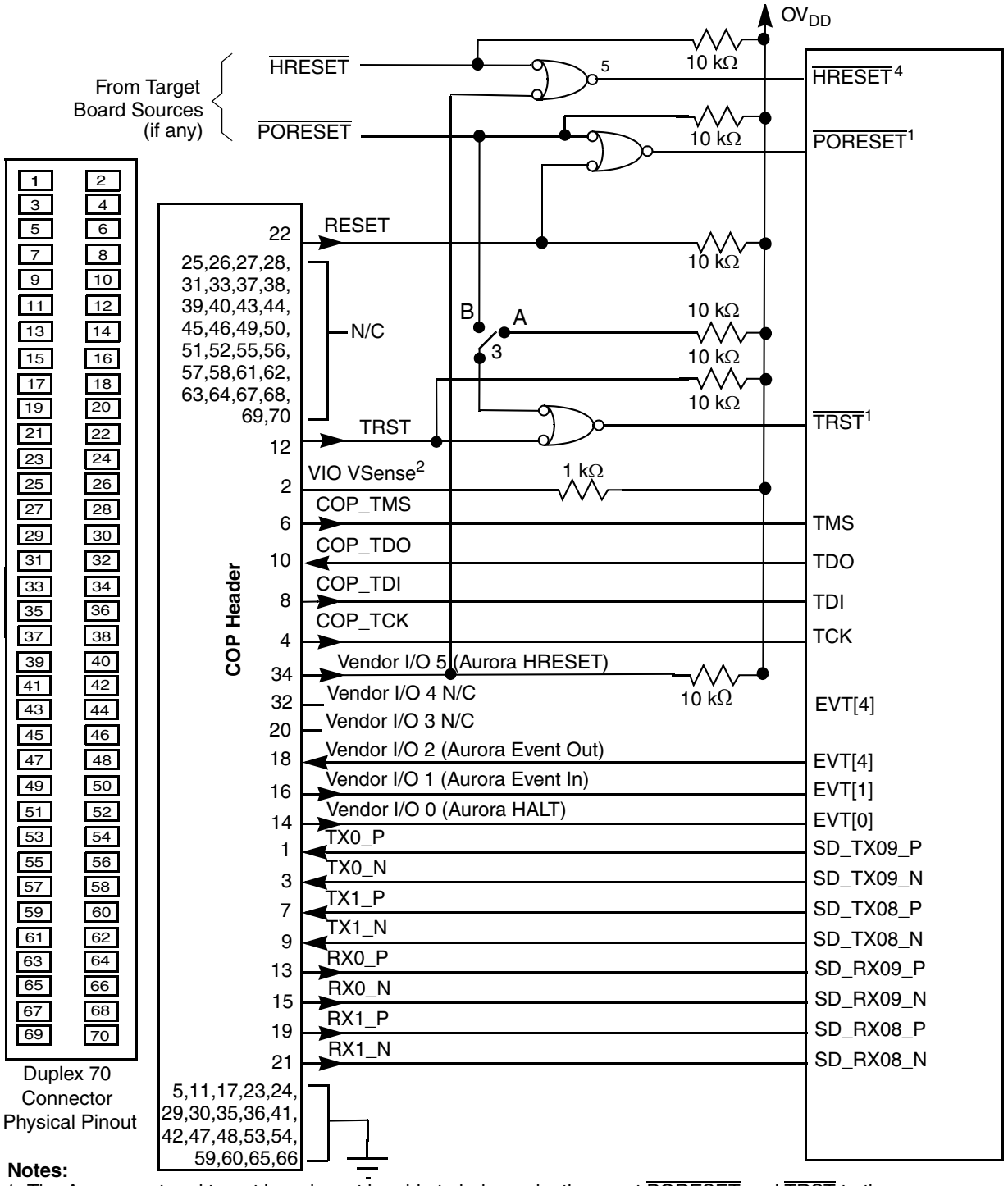
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 54 is common to all known emulators.

3.6.1.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{PORESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 55. If this is not possible, the



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.
5. This is an open-drain gate.

Figure 59. Aurora 70 Pin Connector Duplex Interface Connection

5 Security Fuse Processor

The device implements the QorIQ platform's Trust Architecture supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power Up Sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} must be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part Numbering Nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature. Not all possible combinations of part numbers implied by the part numbering scheme are supported. For a list of available part numbers, contact your Freescale Sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 107. Part Numbering Nomenclature

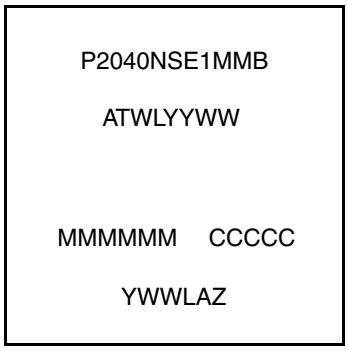
p	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temp. Range**	**Encryption**	**Package Type**	**CPU Freq**	**DDR Data Rate**	**Die Revision**
P = 45 nm	1–5	01 = 1 core 02 = 2 cores 04 = 4 cores	0–9	P = Prototype N = Industrial qualification	S = Std temp X = Extended temp (–40 to 105C)	E = SEC present N = SEC not present	1 = FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	F = 667 MHz H = 800 MHz K = 1000 MHz M = 1200 MHz	L = 1067 MT/s M = 1200 MT/s	A = Rev 1.0 B = Rev 1.1 C = Rev 2.0

6.2 Orderable Part Numbers Addressed by this Document

This table provides the Freescale orderable part numbers addressed by this document for the chip.

6.2.1 Part Marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Notes:

P2040NSE1MMB is the orderable part number. See Table 107 for details.

ATWLYYWW is the test traceability code.
MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

Figure 64. Part Marking for FC-PBGA Device

7 Revision History

This table provides a revision history for this document.

Table 108. Revision History

Rev. Number	Date	Description
2	02/2013	• In Table 7, “P2040 I/O Power Supply Estimated Values,” updated the USB power supply with USB_Vdd_3P3 and updated the typical value with “0.003” in the Others (Reset, System Clock, JTAG & Misc.) row. • In Table 8, “Device AVDD Power Dissipation,” removed V_{DD_LP} from table. • Added Table 10, “VDD_LP Power Dissipation.” • In Table 53, “MPIC Input AC Timing Specifications,” added Trust inputs AC timing and footnote 2. • In Table 93, “Processor Clocking Specifications,” updated footnote 8 with Rev 1.1 silicon. • In Table 107, “Part Numbering Nomenclature,” added “C” in the Die Revision collumn. • In Section 6.2, “Orderable Part Numbers Addressed by this Document,” added the device part numbers for Rev 2.0 silicon.