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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	-
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2040nsn1hlb

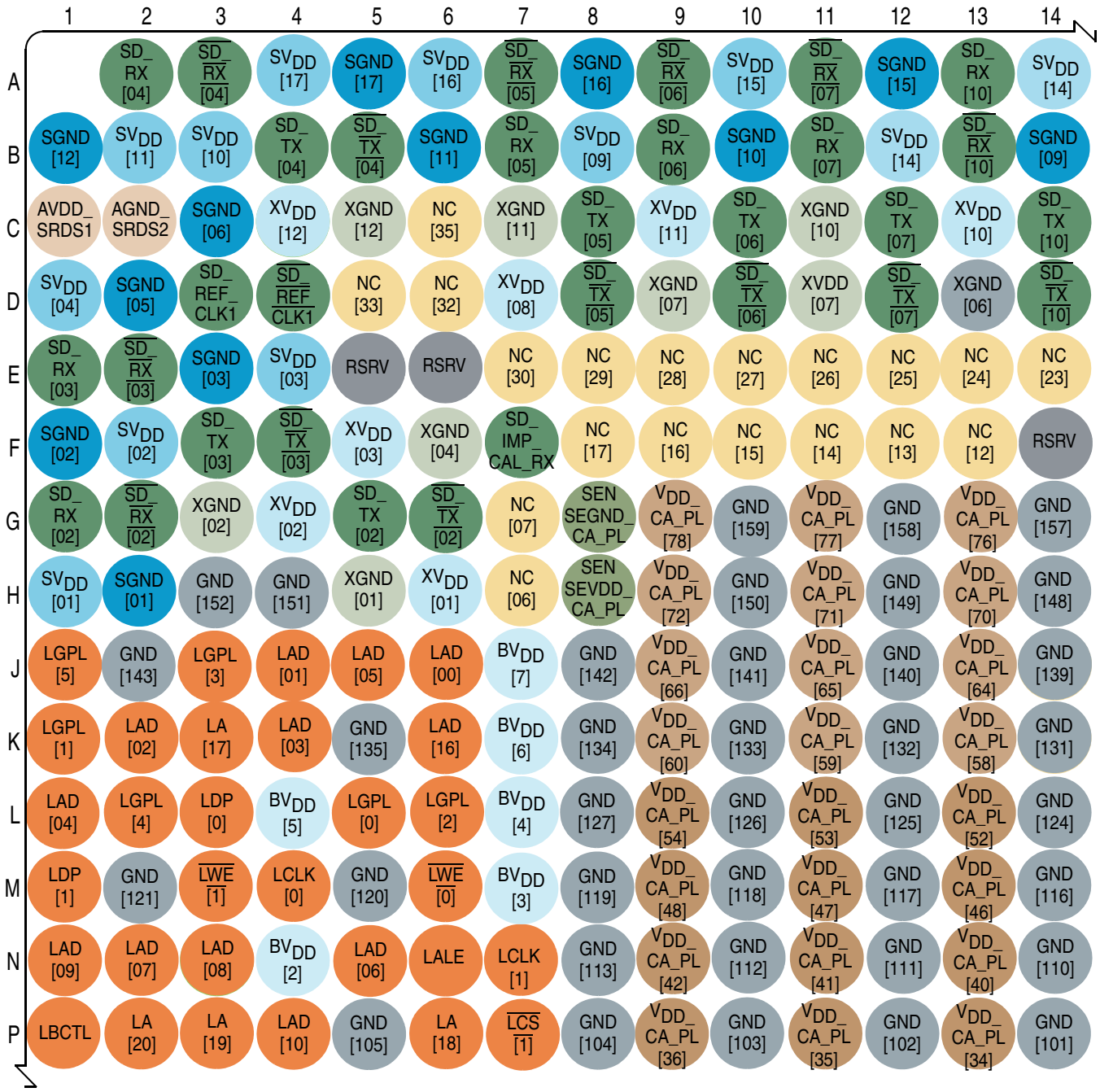

Figure 3. 780 BGA Ball Map Diagram (Detail View A)

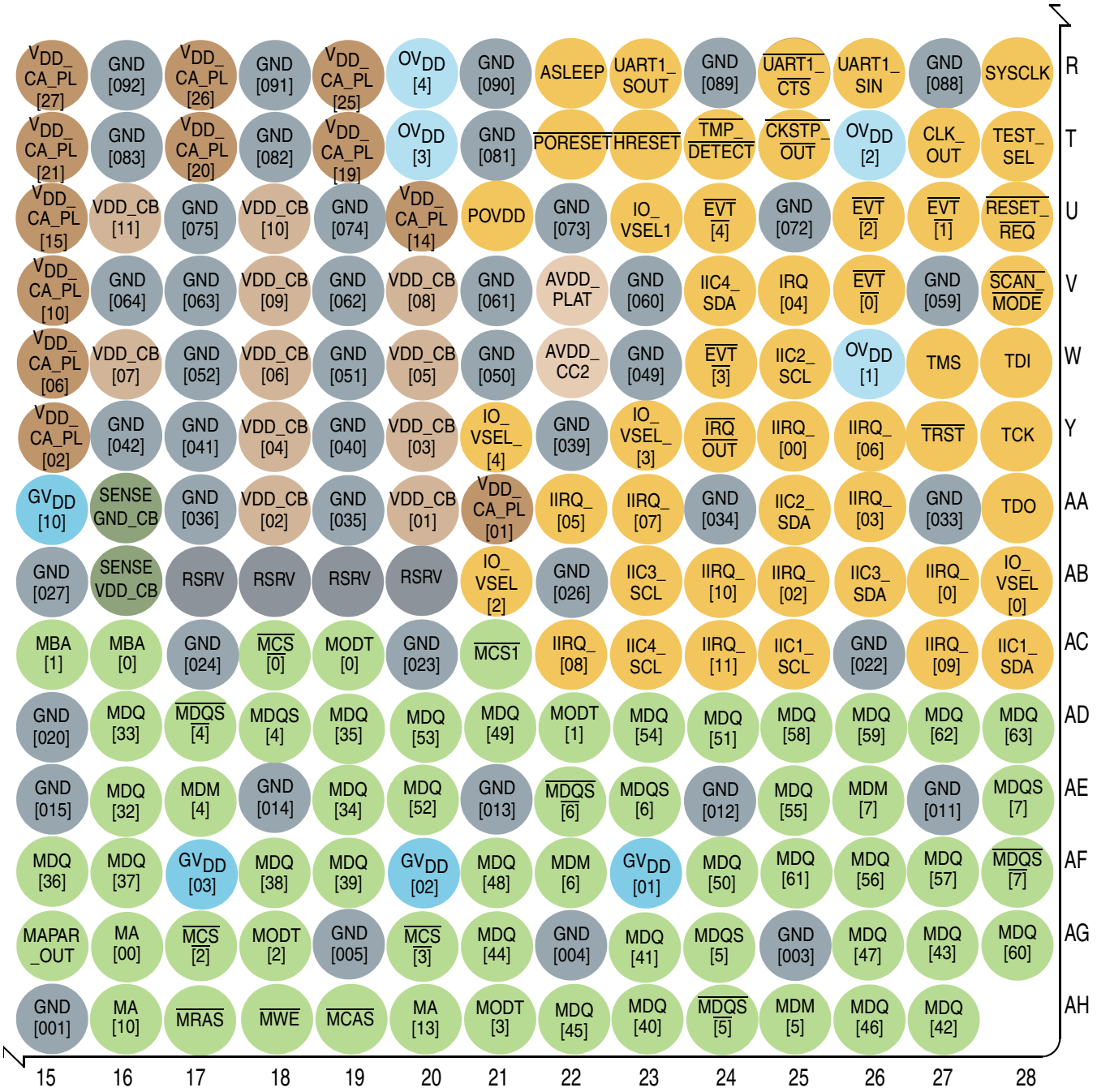

Figure 6. 780 BGA Ball Map Diagram (Detail View D)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IEEE 1588					
TSEC_1588_CLK_IN/EC1_RXD2	Clock In	B27	I	LV_{DD}	—
TSEC_1588_TRIG_IN1/EC1_RXD0	Trigger In 1	B28	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RXD1	Trigger In 2	A27	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1/EC1_TXD0	Alarm Out 1	B24	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/ EC1_TXD1/GPIO30	Alarm Out 2	C25	O	LV_{DD}	23
TSEC_1588_CLK_OUT/EC1_RXD3	Clock Out	B26	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1/EC1_TXD2	Pulse Out1	C28	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_TXD3/GPIO31	Pulse Out2	A26	O	LV_{DD}	23
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	F23	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	G24	I/O	LV_{DD}	—
Ethernet Reference Clock					
EC1_GTX_CLK125/EC_XTRNL_TX_STMP2	Reference Clock (RGMII)	A24	I	LV_{DD}	25
EC2_GTX_CLK125	Reference Clock (RGMII)	D24	I	LV_{DD}	25
Ethernet External Timestamping					
EC_XTRNL_TX_STMP1/EC1_TX_EN	External Timestamp Transmit 1	C27	I	LV_{DD}	—
EC_XTRNL_RX_STMP1/EC1_RX_DV	External Timestamp Receive 1	A25	I	LV_{DD}	—
EC_XTRNL_TX_STMP2/EC1_GTX_CLK125	External Timestamp Transmit 2	A24	I	LV_{DD}	—
EC_XTRNL_RX_STMP2/EC1_RX_CLK	External Timestamp Receive 2	C24	I	LV_{DD}	—
Three-Speed Ethernet Controller 1					
EC1_TXD3/TSEC_1588_PULSE_OUT2/GPIO31	Transmit Data	A26	O	LV_{DD}	—
EC1_TXD2/TSEC_1588_PULSE_OUT1	Transmit Data	C28	O	LV_{DD}	—
EC1_TXD1/TSEC_1588_ALARM_OUT2/GPIO30	Transmit Data	C25	O	LV_{DD}	—
EC1_TXD0/TSEC_1588_ALARM_OUT1	Transmit Data	B24	O	LV_{DD}	—
EC1_TX_EN/EC_XTRNL_TX_STMP1	Transmit Enable	C27	O	LV_{DD}	15
EC1_GTX_CLK	Transmit Clock Out (RGMII)	D26	O	LV_{DD}	24
EC1_RXD3/TSEC_1588_CLK_OUT	Receive Data	B26	I	LV_{DD}	25
EC1_RXD2/TSEC_1588_CLK_IN	Receive Data	B27	I	LV_{DD}	25

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
XGND08	SerDes Transceiver GND	C21	—	—	—
XGND07	SerDes Transceiver GND	D9	—	—	—
XGND06	SerDes Transceiver GND	D13	—	—	—
XGND05	SerDes Transceiver GND	D19	—	—	—
XGND04	SerDes Transceiver GND	F6	—	—	—
XGND03	SerDes Transceiver GND	F21	—	—	—
XGND02	SerDes Transceiver GND	G3	—	—	—
XGND01	SerDes Transceiver GND	H5	—	—	—
SGND17	SerDes Core Logic GND	A5	—	—	—
SGND16	SerDes Core Logic GND	A8	—	—	—
SGND15	SerDes Core Logic GND	A12	—	—	—
SGND14	SerDes Core Logic GND	A16	—	—	—
SGND13	SerDes Core Logic GND	A20	—	—	—
SGND12	SerDes Core Logic GND	B1	—	—	—
SGND11	SerDes Core Logic GND	B6	—	—	—
SGND10	SerDes Core Logic GND	B10	—	—	—
SGND09	SerDes Core Logic GND	B14	—	—	—
SGND08	SerDes Core Logic GND	B18	—	—	—
SGND07	SerDes Core Logic GND	B22	—	—	—
SGND06	SerDes Core Logic GND	C3	—	—	—
SGND05	SerDes Core Logic GND	D2	—	—	—
SGND04	SerDes Core Logic GND	D17	—	—	—
SGND03	SerDes Core Logic GND	E3	—	—	—
SGND02	SerDes Core Logic GND	F1	—	—	—
SGND01	SerDes Core Logic GND	H2	—	—	—
AGND_SRDS1	SerDes PLL1 GND	C2	—	—	—
AGND_SRDS2	SerDes PLL2 GND	B17	—	—	—
SENSEGND_CA_PL	Core Group A and Platform GND Sense	G8	—	—	8
SENSEGND_CB	Core Group B GND Sense	AA16	—	—	8
USB1_AGND06	USB1 PHY Transceiver GND	J28	—	—	—
USB1_AGND05	USB1 PHY Transceiver GND	K27	—	—	—
USB1_AGND04	USB1 PHY Transceiver GND	L27	—	—	—
USB1_AGND03	USB1 PHY Transceiver GND	M22	—	—	—
USB1_AGND02	USB1 PHY Transceiver GND	M24	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
Reserve	—	AB20	—	GND	19

Note:

1. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD} in order to ensure no random chip select assertion due to possible noise, etc.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the corresponding power and ground nets internally. They may be connected as a differential pair to be used by the voltage regulators with remote sense function. For Rev1.1 silicon, the better solution is to use the far sense pins relative to the power supply location, the other pair can be left as no connected. The DC power simulation should be done during the board layout process to approve the selected solution.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
10. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
11. Do not connect.
12. These are test signals for factory use only and must be pulled low (1 KΩ–2 kΩ) to ground (GND) for normal machine operation.
13. Independent supplies derived from board $V_{DD\_CA\_CB\_PL}$ (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD} if I^2C interface is used.
15. This pin requires an external 1 KΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
17. These pins must be pulled up to 1.2 V through a 180 $\Omega \pm 1\%$ resistor for EM2_MDC and a 330 $\Omega \pm 1\%$ resistor for EM2_MDIO.
18. Pin has a weak internal pull-up.
19. These pins must be pulled to ground (GND).
20. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
21. This pin requires a 200-Ω pull-up to XV_{DD}.
22. This pin requires a 200-Ω pull-up to SV_{DD}.
23. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
24. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
25. See Section 3.6, "Connection Recommendations," for additional details on this signal.

Table 6. Device Power Dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	667	534	1067	467	1.0	65	8.7	—	8.2	—	—	2, 3
Thermal						105	12.0	—	11.8	—	—	5, 7
Maximum							12.3	11.1	11.9	10.6	1.4	4, 6, 7

Note:

1. Combined power of $V_{DD\_CA\_CB\_PL}$, SVDD with the DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P2040 I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.705	1.764	W	1,2,5,6
	800 MT/s data rate		0.714	1.785		
	1066 MT/s data rate		0.731	1.827		
	1200 MT/s data rate		0.739	1.848		
	1333 MT/s data rate		0.747	1.869		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1, 7
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC Per Controller	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.35 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed the $MV_{REF}n$ DC level by more than ±1% of the DC value (that is, ±13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF}n with a min value of MV_{REF}n – 0.04 and a max value of MV_{REF}n + 0.04. V_{TT} should track variations in the DC level of MVREFn.
4. The voltage regulator for $MV_{REF}n$ must meet the specifications stated in Table 23.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. I_{OH} and I_{OL} are measured at GV_{DD} = 1.283 V

This table provides the DDR controller interface capacitance for DDR3 and DDR3L.

Table 22. DDR3 and DDR3L SDRAM Capacitance

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.150 V.
2. This parameter is sampled. GV_{DD} = 1.35 V – 0.067 V ÷ + 0.100 V (for DDR3L), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.167 V.

This table provides the current draw characteristics for MVREF*n*.

Table 23. Current Draw Characteristics for MVREF*n*

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Current draw for DDR3 SDRAM for MVREF*n*	MVREF*n*	—	500	μA	—
Current draw for DDR3L SDRAM for MVREF*n*	MVREF*n*	—	500	μA	—

2.9.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

This figure represents the AC timing from Table 33 in master mode (internal clock). Note that although timing specifications generally refer to the rising edge of the clock, this figure also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

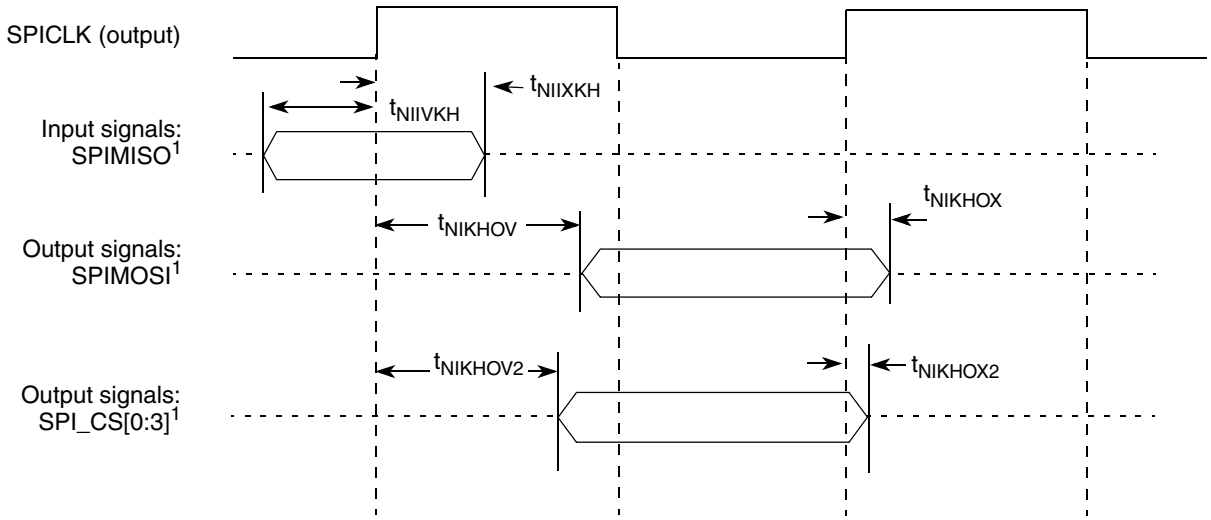

Figure 15. eSPI AC Timing in Master Mode (Internal Clock) Diagram

2.11 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.11.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 34. DUART DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

Table 38. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

The Ethernet management interface is defined to operate at a supply voltage of 2.5 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 39. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

2.12.3.2 Ethernet Management Interface AC Timing Specifications

This table provides the Ethernet management interface AC timing specifications.

Table 40. Ethernet Management Interface AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 6$	—	$(16 \times t_{plb\_clk}) + 6$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

This figure provides the JTAG clock input timing diagram.

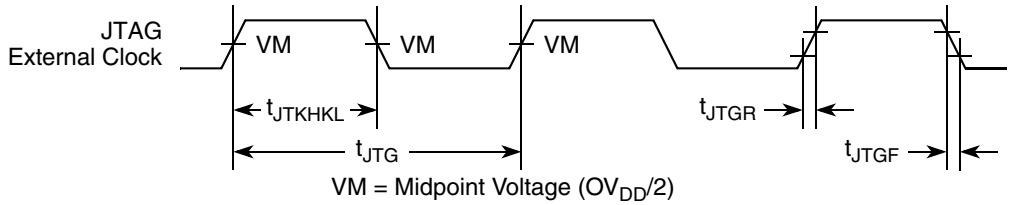

Figure 26. JTAG Clock Input Timing Diagram

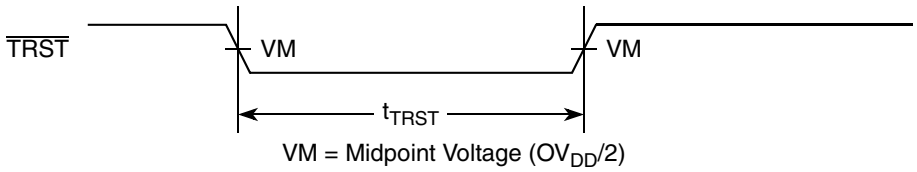

Figure 27. $\overline{\text{TRST}}$ Timing Diagram

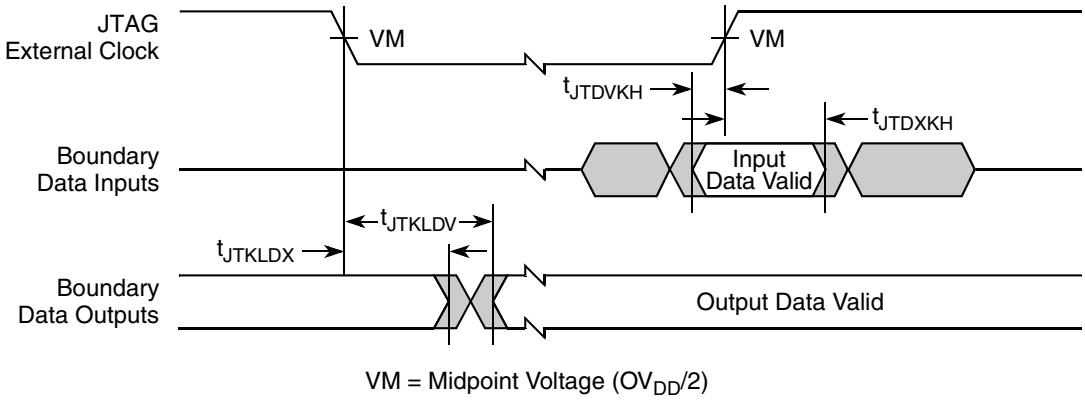

Figure 28. Boundary-Scan Timing Diagram

2.18 I²C

This section describes the DC and AC electrical characteristics for the I^2C interface.

2.18.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 56. I^2C DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2

2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V.

Table 58. GPIO DC Electrical Characteristics (CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max L/OV_{IN} respective values found in Table 3.
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} or LV_{DD} = 2.5 V.

Table 59. GPIO DC Electrical Characteristics (CV_{DD} or LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

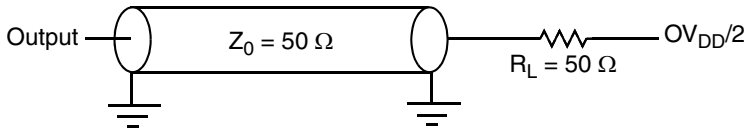

Figure 31. GPIO AC Test Load

2.20 High-Speed Serial Interfaces (HSSI)

The device features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, Aurora, and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or a receiver input (SD_RX*n* and $\overline{\text{SD\_RX}n}$). Each signal swings between A volts and B volts where A > B.

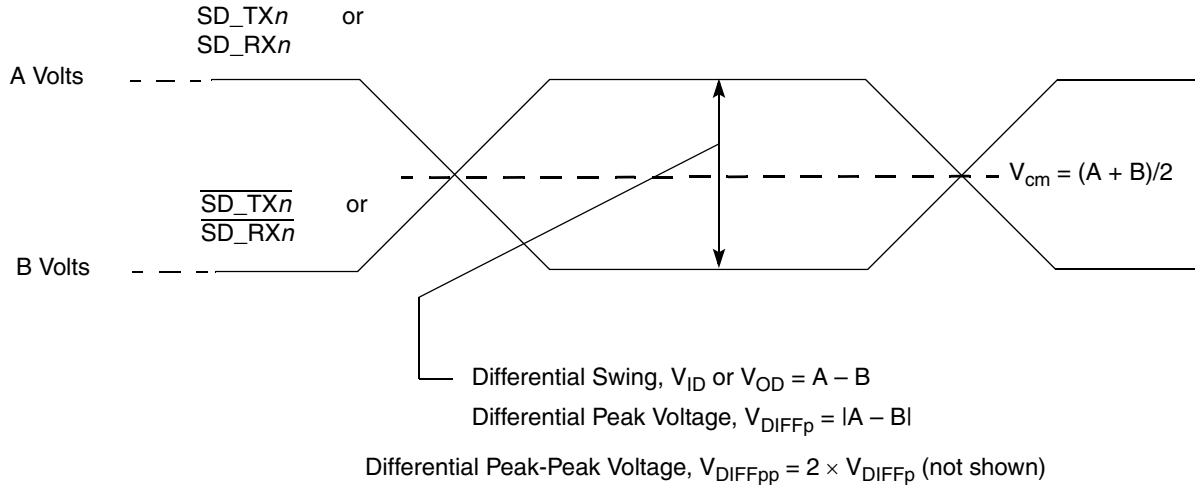

Figure 32. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX*n*, $\overline{\text{SD\_TX}n}$, SD_RX*n* and $\overline{\text{SD\_RX}n}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**):

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn} - V_{\overline{SD\_TXn}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**):

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn} - V_{\overline{SD\_RXn}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}n}$, for example) from the non-inverting signal ($\overline{\text{SD\_TX}n}$, for example) within a differential pair. There is

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in Section 2.1.2, "Recommended Operating Conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ are internally AC-coupled differential inputs as shown in Figure 33. Each differential clock input (SD_REF_CLK*n* or $\overline{\text{SD\_REF\_CLK}n}$) has on-chip 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. This figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

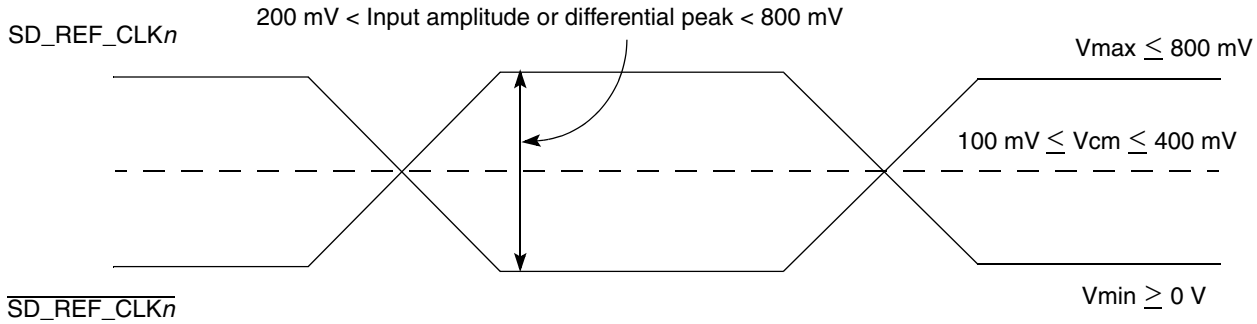

Figure 34. Differential Reference Clock Input DC Requirements (External DC-Coupled)

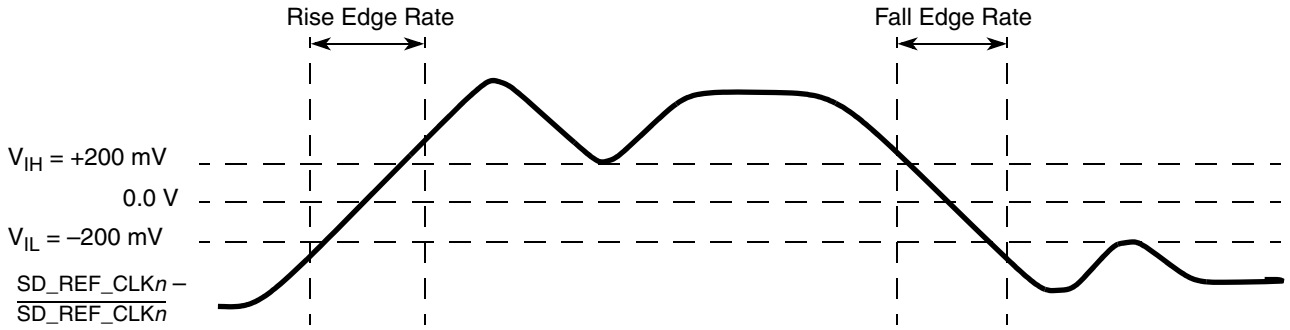

Figure 37. Differential Measurement Points for Rise and Fall Time

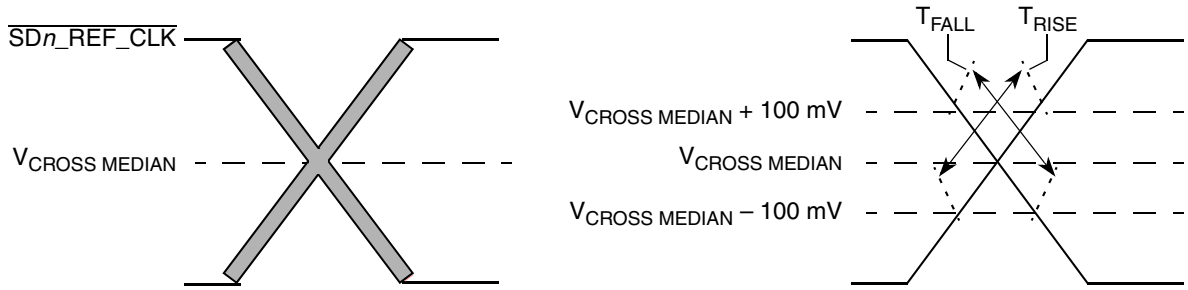

Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 Spread Spectrum Clock

SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

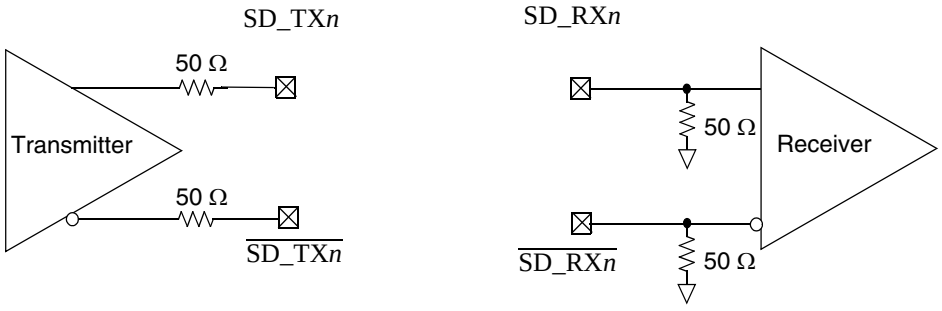

Figure 39. SerDes Transmitter and Receiver Reference Circuits

Table 62. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 63. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	—	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.4.4 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.20.5.1 Signal Definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. This figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$—each have a peak-to-peak swing of A – B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

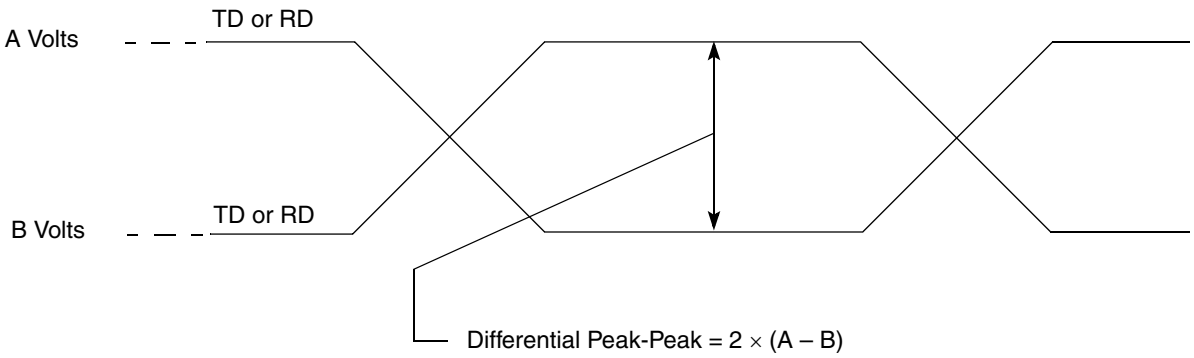

Figure 41. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.20.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.

See Section 19.4 “LP-Serial Signal Descriptions,” in the chip reference manual for Serial RapidIO interface width and frequency details.

3.1.7 SerDes PLL Ratio

The clock ratio between each of the three SerDes PLLs and their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs is determined by the binary value of the RCW Configuration field SRDS_RATIO_B*n* as shown in this table. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW field SRDS_DIV_B*n* as shown in Table 103.

This table lists the supported SerDes PLL Bank *n* to SD_REF_CLK*n* ratios.

Table 101. SerDes PLL Bank *n* to SD_REF_CLK*n* Ratios

Binary Value of SRDS_RATIO_B1	SRDS_PLL_*n*:SD_REF_CLK*n* Ratio	
	***n* = 1 (Bank)**	***n* = 2 (Bank 2)**
000	Reserved	Reserved
001	Reserved	20:1
010	25:1	25:1
011	40:1	40:1
100	50:1	50:1
101	Reserved	24:1
110	Reserved	30:1
All Others	Reserved	Reserved

These tables list the supported SerDes PLL dividers.

This table shows the PLL divider support for each pair of lanes on SerDes Bank 1.

Table 102. SerDes Bank 1 PLL Dividers

Binary Value of SRDS_DIV_B1[0:4]	SerDes Bank 1 PLL Divider
0b0	Divide by 1 off Bank 1 PLL
0b1	Divide by 2 off Bank 1 PLL

Note: 1 bit (of 5 total SRDS_DIV_B1 bits) controls each pair of lanes.

This table shows the PLL dividers supported for each 4-lane for SerDes Banks 2.

Table 103. SerDes Banks 2 PLL Dividers

Binary Value of SRDS_DIV_B2	SerDes Bank *2* PLL Divider
0b0	Divide by 1 off Bank *2* PLL
0b1	Divide by 2 off Bank *2* PLL

Note: 1 bit controls all four lanes of bank 2.

3.1.8 Frame Manager (FMan) Clock Select

The Frame Managers (FM) can each be synchronous to the platform.

3.3 Power Supply Design

This section discusses the power supply design.

3.3.1 PLL Power Supply Filtering

Each of the PLLs described in Section 3.1, "System Clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, AV_{DD_CCn} and AV_{DD_DDR} voltages must be derived directly from the $V_{DD\_CA\_CB\_PL}$ source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 50, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 50 shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%

C1 = 10µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH

C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD}.

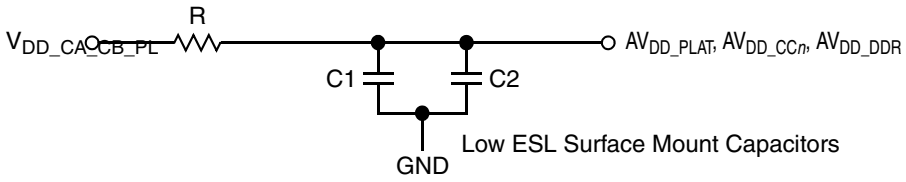

Figure 50. PLL Power Supply Filter Circuit

The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 51. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn}

to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide, and direct.

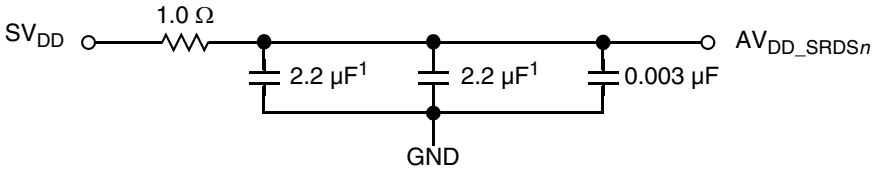

Figure 51. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD_SRDSn} must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn}.
- A 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} Power Supply Filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered GV_{DD}. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where XV_{DD} is sourced from GV_{DD}, is illustrated in Figure 52. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

C2 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

F1 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

F2 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

Bulk and decoupling capacitors are added, as needed, per power supply design.

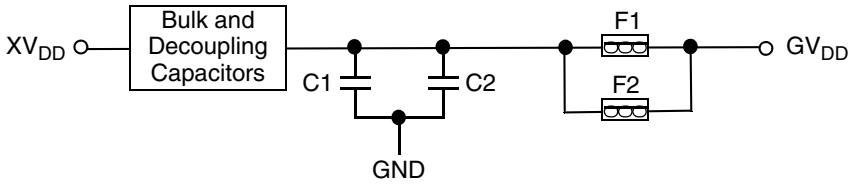

Figure 52. XV_{DD} Power Supply Filter Circuit

3.3.3 $USB\_V_{DD}\_1P0$ Power Supply Filtering

$USB\_V_{DD}\_1P0$ must be sourced by a filtered $V_{DD\_CA\_CB\_PL}$ using a star connection. An example solution for $USB\_V_{DD}\_1P0$ filtering, where $USB\_V_{DD}\_1P0$ is sourced from $V_{DD\_CA\_CB\_PL}$, is illustrated in Figure 53. The component values in this example filter is system dependent and are still under characterization; component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 µF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)

F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)

Bulk and decoupling capacitors are added, as needed, per power supply design.