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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	-
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2040nsn1mmb

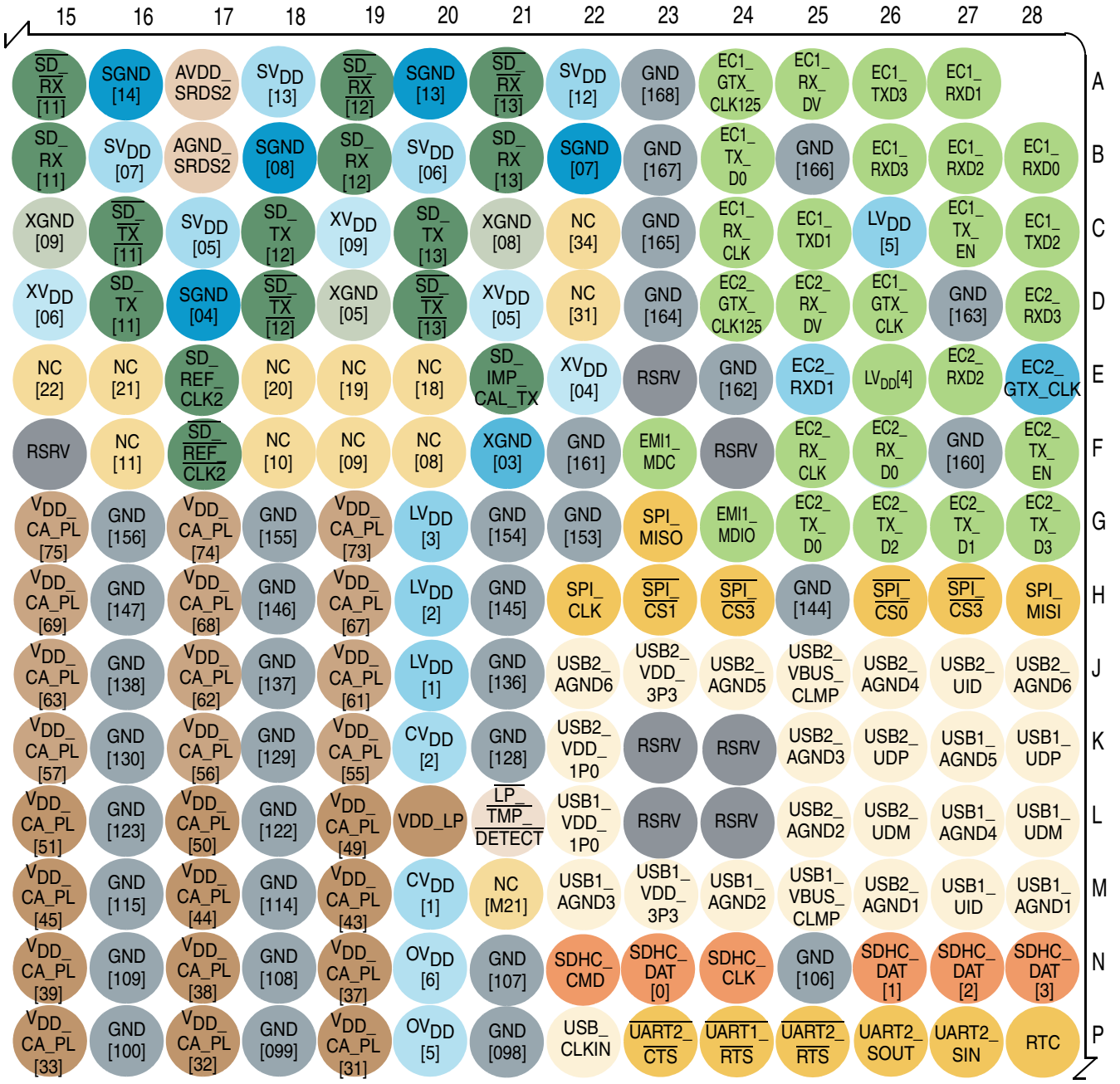


Figure 4. 780 BGA Ball Map Diagram (Detail View B)

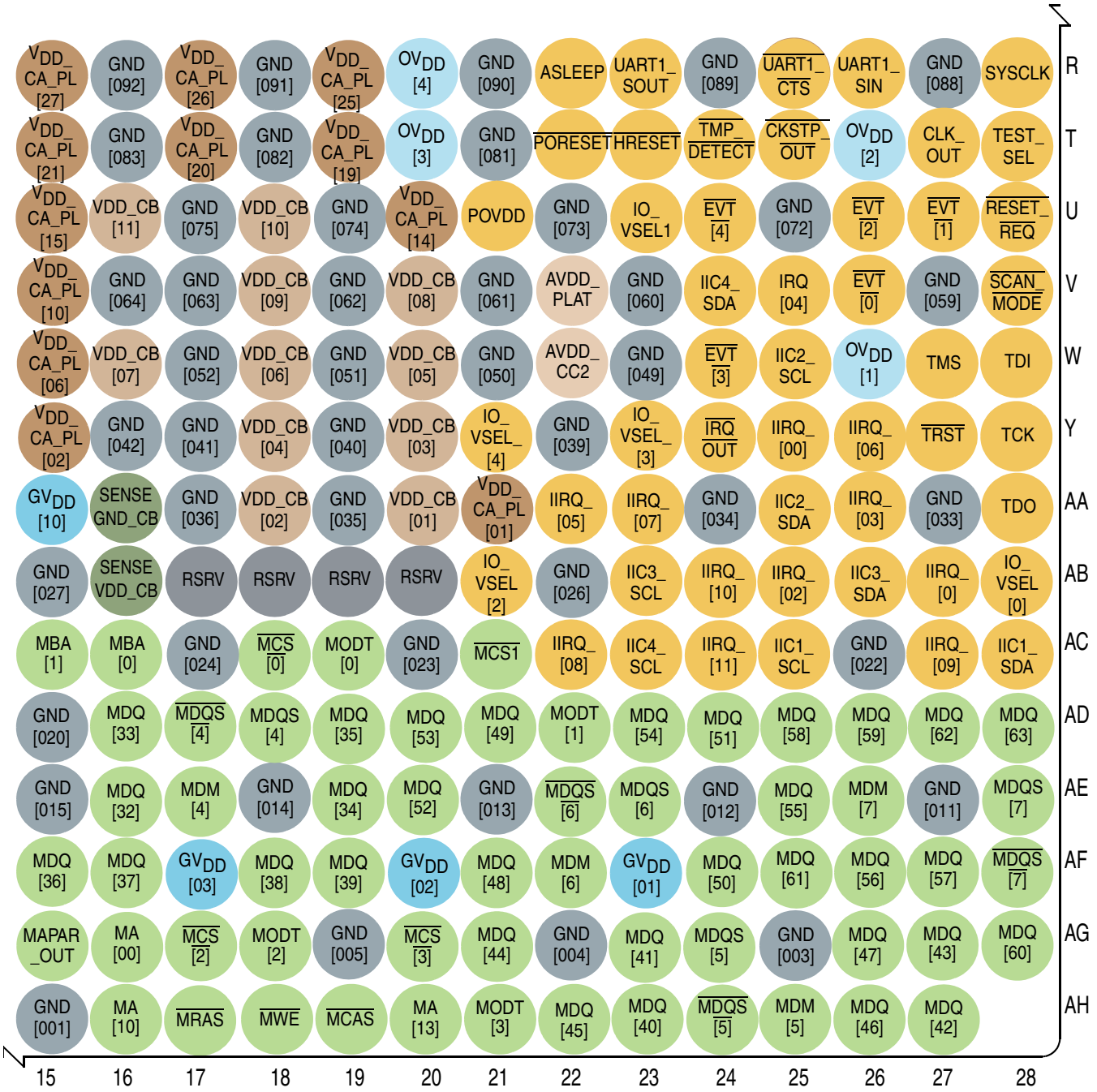


Figure 6. 780 BGA Ball Map Diagram (Detail View D)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ29	Data	AC4	I/O	GV_{DD}	—
MDQ30	Data	AE1	I/O	GV_{DD}	—
MDQ31	Data	AE3	I/O	GV_{DD}	—
MDQ32	Data	AE16	I/O	GV_{DD}	—
MDQ33	Data	AD16	I/O	GV_{DD}	—
MDQ34	Data	AE19	I/O	GV_{DD}	—
MDQ35	Data	AD19	I/O	GV_{DD}	—
MDQ36	Data	AF15	I/O	GV_{DD}	—
MDQ37	Data	AF16	I/O	GV_{DD}	—
MDQ38	Data	AF18	I/O	GV_{DD}	—
MDQ39	Data	AF19	I/O	GV_{DD}	—
MDQ40	Data	AH23	I/O	GV_{DD}	—
MDQ41	Data	AG23	I/O	GV_{DD}	—
MDQ42	Data	AH27	I/O	GV_{DD}	—
MDQ43	Data	AG27	I/O	GV_{DD}	—
MDQ44	Data	AG21	I/O	GV_{DD}	—
MDQ45	Data	AH22	I/O	GV_{DD}	—
MDQ46	Data	AH26	I/O	GV_{DD}	—
MDQ47	Data	AG26	I/O	GV_{DD}	—
MDQ48	Data	AF21	I/O	GV_{DD}	—
MDQ49	Data	AD21	I/O	GV_{DD}	—
MDQ50	Data	AF24	I/O	GV_{DD}	—
MDQ51	Data	AD24	I/O	GV_{DD}	—
MDQ52	Data	AE20	I/O	GV_{DD}	—
MDQ53	Data	AD20	I/O	GV_{DD}	—
MDQ54	Data	AD23	I/O	GV_{DD}	—
MDQ55	Data	AE25	I/O	GV_{DD}	—
MDQ56	Data	AF26	I/O	GV_{DD}	—
MDQ57	Data	AF27	I/O	GV_{DD}	—
MDQ58	Data	AD25	I/O	GV_{DD}	—
MDQ59	Data	AD26	I/O	GV_{DD}	—
MDQ60	Data	AG28	I/O	GV_{DD}	—
MDQ61	Data	AF25	I/O	GV_{DD}	—
MDQ62	Data	AD27	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note

26. For reduced core (core 2 and 3 disabled) mode, this signal must be pulled high (100 Ω–1 kΩ) to OVDD.
27. Warning, incorrect voltage select settings can lead to irreversible device damage. This pin has an internal 2 kΩ pull-down resistor, to pull it high, a pull-up resistor of less than 1 kΩ to OVDD should be used. See Section 3.2, "Supply Power Default Setting."
28. SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
29. The *cfg_xvdd_sel* (LA[26]) reset configuration pin must select the correct voltage that is being supplied on the XVDD pin. Incorrect voltage select settings can lead to irreversible device damage.
30. See Section 2.2, "Power Up Sequencing," and Section 5, "Security Fuse Processor," for additional details on this signal.
31. Pin must NOT be pulled down during power-on reset.
32. This pin must be connected to GND through a 10 kΩ ± 0.1% resistor for bias generation.
33. A 1μF to 1.5 μF capacitor connected to GND is required on this signal. Section 3.6.4.2, "USBn_V_{DD}_1P8_DECAP Capacitor Options," provides a list of recommended capacitors.
34. A divider network is required on this signal. See Section 3.6.4.1, "USB Divider Network."
35. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal machine operation.
36. For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull-up on LGPL4 is required.
37. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but they are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section describes the ratings, conditions, and other electrical characteristics.

2.1.1 Absolute Maximum Ratings

Table 2. Absolute Operating Conditions[1]

Parameter	Symbol	Max Value	Unit	Note
Core Group A (cores 0–1) and platform supply voltage (Silicon Rev 1.0)	$V_{DD\_CA\_PL}$	–0.3 to 1.1	V	9, 10
Core Group B (cores 2–3) supply voltage (Silicon Rev 1.0)	V_{DD_CB}	–0.3 to 1.1	V	9, 10
Core Group A (cores 0–1), Core Group B (cores 2–3) and platform supply voltage (Silicon Rev 1.1)	$V_{DD\_CA\_CB\_PL}$	–0.3 to 1.1	V	9, 10
PLL supply voltage (core, platform, DDR)	AV_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (SerDes, filtered from SV_{DD})	AV_{DD_SRDS}	–0.3 to 1.1	V	—
Fuse programming override supply	POV_{DD}	–0.3 to 1.65	V	1
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—

Table 7. P2040 I/O Power Supply Estimated Values (continued)

IEEE 1588	—	LVdd (2.5V)	0.004	0.005	W	1,3,6
eLBC	32-bit, 100Mhz	BVdd (1.8V)	0.048	0.120	W	1,3,6
		BVdd (2.5V)	0.072	0.193		
		BVdd (3.3V)	0.120	0.277		
	16-bit, 100Mhz	BVdd (1.8V)	0.021	0.030	W	1,3,6
		BVdd (2.5V)	0.036	0.046		
		BVdd (3.3V)	0.057	0.076		
eSDHC	—	Ovdd (3.3V)	0.014	0.150	W	1,3,6
eSPI	—	CVdd (1.8V)	0.004	0.005	W	1,3,6
		CVdd (2.5V)	0.006	0.008		
		CVdd (3.3V)	0.010	0.013		
USB	—	USB_Vdd_3P3	0.012	0.015	W	1,3,6
I2C	—	OVdd (3.3V)	0.002	0.003	W	1,3,6
DUART	—	OVdd (3.3V)	0.006	0.008	W	1,3,6
GPIO	x8	OVdd (1.8V)	0.005	0.006	W	1,3,4,6
		OVdd (2.5V)	0.007	0.009		
		OVdd (3.3V)	0.009	0.011		
Others (Reset, System Clock, JTAG & Misc)	—	OVdd (3.3V)	0.003	0.015	W	1,3,4,6

Note:

1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load.
4. GPIO's are supported on 1.8 V, 2.5 V and 3.3 V rails as specified in the hardware specification.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guranteed current.
7. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configuration combination possible for the device. To get the XVDD power numbers, the user should add the combined lanes to match to the total SerDes lanes used, not simply multiply the power numbers by the number of lanes.

2.6.3 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the e500mc; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 16× the period of the platform clock. That is, minimum clock high time is 8× (platform clock), and minimum clock low time is 8× (platform clock). There is no minimum RTC frequency; RTC may be grounded if not needed.

2.6.4 dTSEC Gigabit Ethernet Reference Clock Timing

This table provides the dTSEC gigabit reference clocks DC electrical characteristics.

Table 15. EC_GTX_CLK125 DC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.

This table provides the dTSEC gigabit reference clocks AC timing specifications.

Table 16. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Note:
1. Rise and fall times for EC_GTX_CLK125 are measured from 20% to 80% (rise time) and 80% to 20% (fall time) of LV_{DD}.
2. EC_GTX_CLK125 is used to generate the GTX clock for the dTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the dTSEC GTX_CLK. See Section 2.12.2.2, "RGMII AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.6.5 Other Input Clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information on the input clock requirements of functional blocks sourced external of the device, such as SerDes, Ethernet Management, eSDHC, Local Bus, see the specific interface section.

This figure provides the AC test load for the DDR3 and DDR3L controller bus.

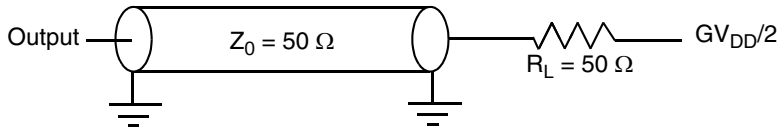


Figure 12. DDR3 and DDR3L Controller Bus AC Test Load

2.9.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 and DDR3L SDRAM controller interface. This figure shows the differential timing specification.

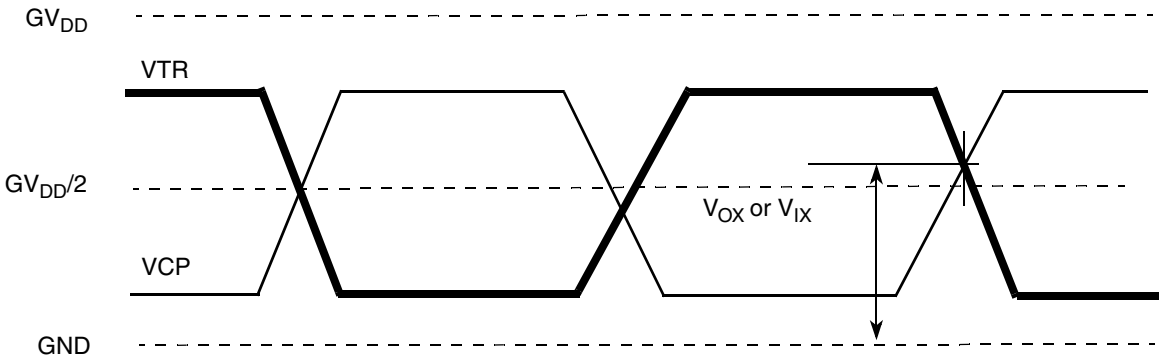


Figure 13. DDR3 and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

This table provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 28. DDR3 SDRAM Differential Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.150$	$0.5 \times GV_{DD} + 0.150$	V	—
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.115$	$0.5 \times GV_{DD} + 0.115$	V	—

Note:
1. I/O drivers are calibrated before making measurements.

This table provides the DDR3L differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 29. DDR3L SDRAM Differential Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit	Note
Input AC differential cross-point voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.135$	$0.5 \times GV_{DD} + 0.135$	V	—
Output AC differential cross-point voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.105$	$0.5 \times GV_{DD} + 0.105$	V	—

Note:
1. I/O drivers are calibrated before making measurements.

2.14 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 46. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 47. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This figure shows the AC timing diagram of the local bus interface.

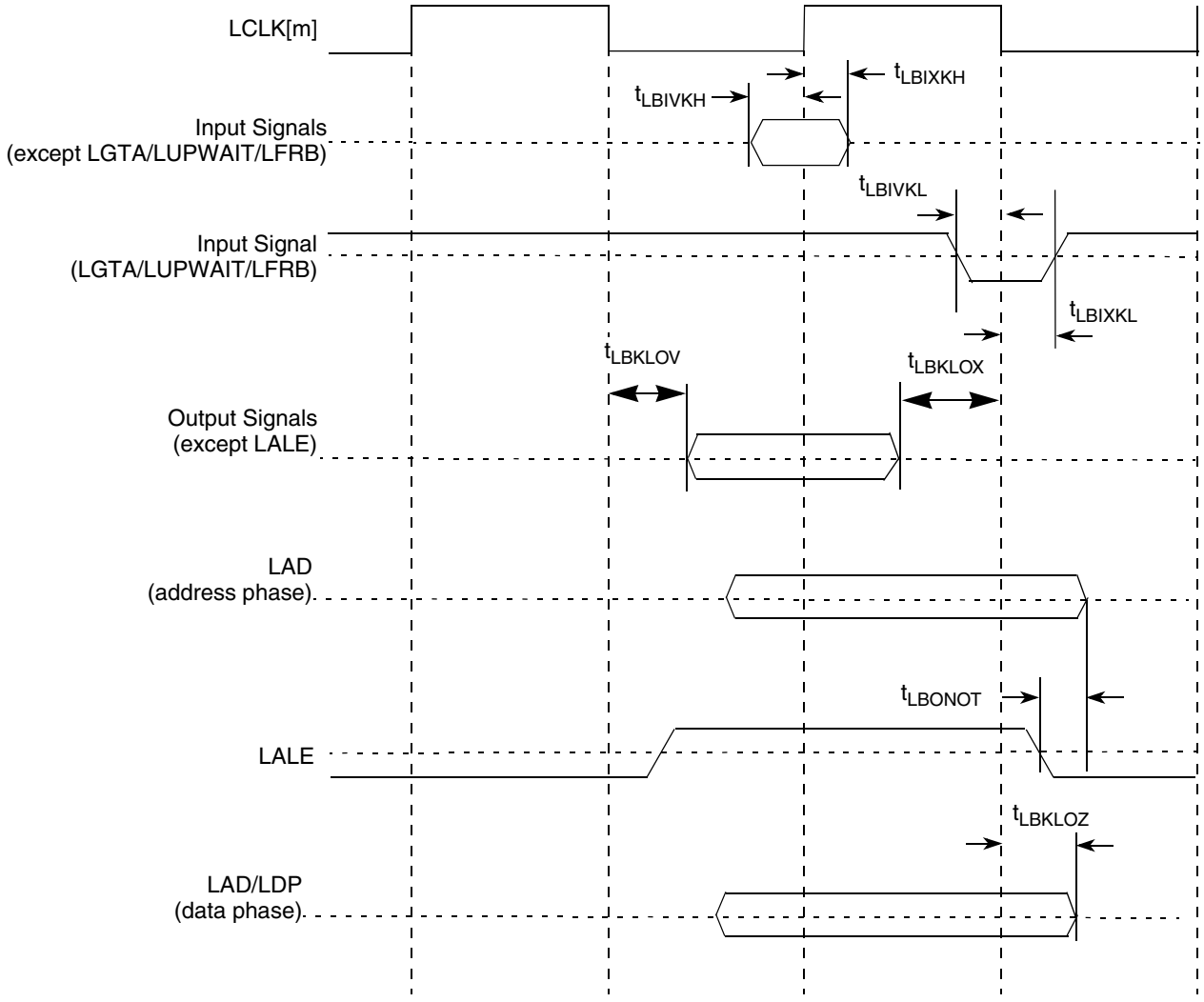


Figure 21. Enhanced Local Bus Signals

Figure 22 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

Table 56. I^2C DC Electrical Characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–40	40	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.18.2 I^2C AC Electrical Specifications

This table provides the I^2C AC timing specifications.

Table 57. I^2C AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V.

Table 58. GPIO DC Electrical Characteristics (CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max L/OV_{IN} respective values found in Table 3.
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} or LV_{DD} = 2.5 V.

Table 59. GPIO DC Electrical Characteristics (CV_{DD} or LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or a receiver input (SD_RX*n* and $\overline{\text{SD\_RX}n}$). Each signal swings between A volts and B volts where A > B.

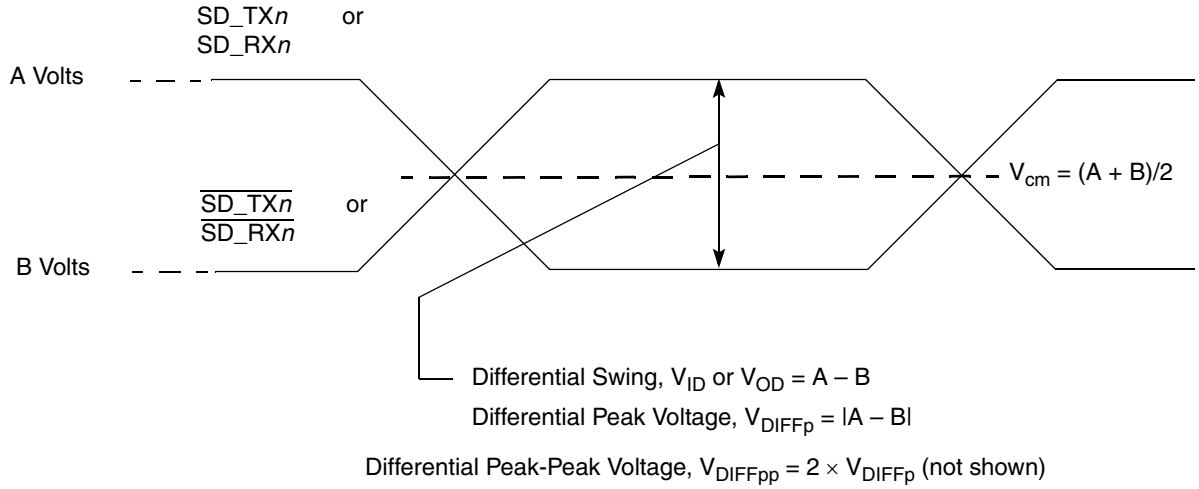


Figure 32. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX*n*, $\overline{\text{SD\_TX}n}$, SD_RX*n* and $\overline{\text{SD\_RX}n}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**):

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn} - V_{\overline{SD\_TXn}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**):

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn} - V_{\overline{SD\_RXn}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}n}$, for example) from the non-inverting signal ($\overline{\text{SD\_TX}n}$, for example) within a differential pair. There is

only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 37 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{\overline{SD\_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{TD}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and $\overline{SD\_REF\_CLK1}$ for SerDes bank1 and SD_REF_CLK2 and $\overline{SD\_REF\_CLK2}$ for SerDes bank2.

SerDes banks 1–2 may be used for various combinations of the following IP blocks based on the RCW configuration field SRDS_PRTCL:

- SerDes bank 1: PCI Express 1/2/3, sRIO1/2, SGMII (1.25 Gbps only).
- SerDes bank 2: PCI Express3, SGMII (1.25 or 3.125 GBaud), SATA or Aurora.

The following sections describe the SerDes reference clock requirements and provide application information.

2.20.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

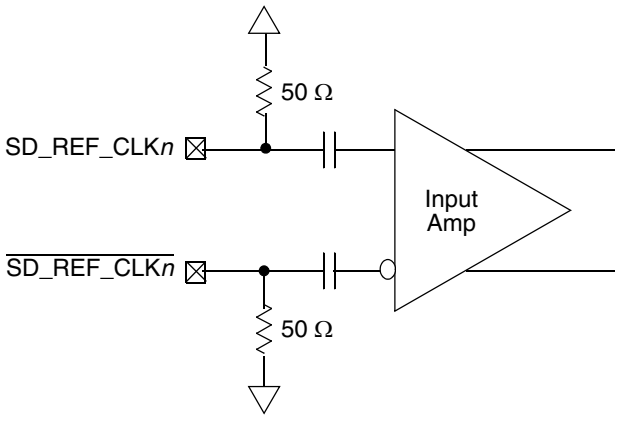


Figure 33. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in Section 2.1.2, "Recommended Operating Conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ are internally AC-coupled differential inputs as shown in Figure 33. Each differential clock input (SD_REF_CLK*n* or $\overline{\text{SD\_REF\_CLK}n}$) has on-chip 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. This figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

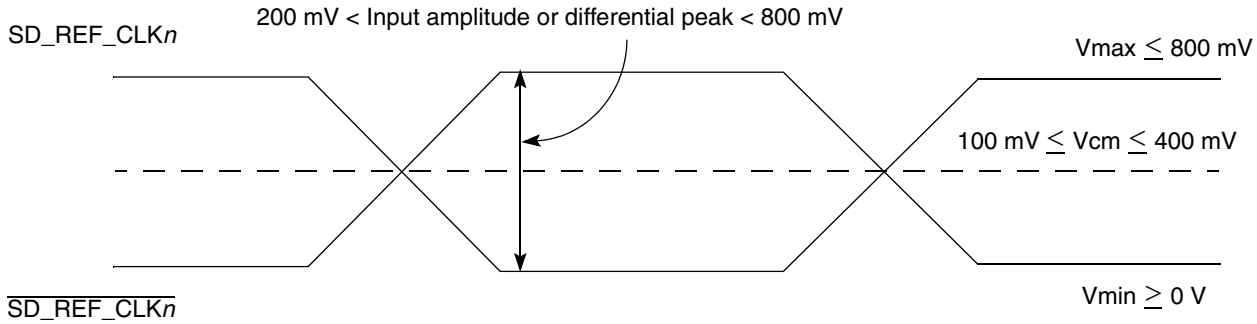


Figure 34. Differential Reference Clock Input DC Requirements (External DC-Coupled)

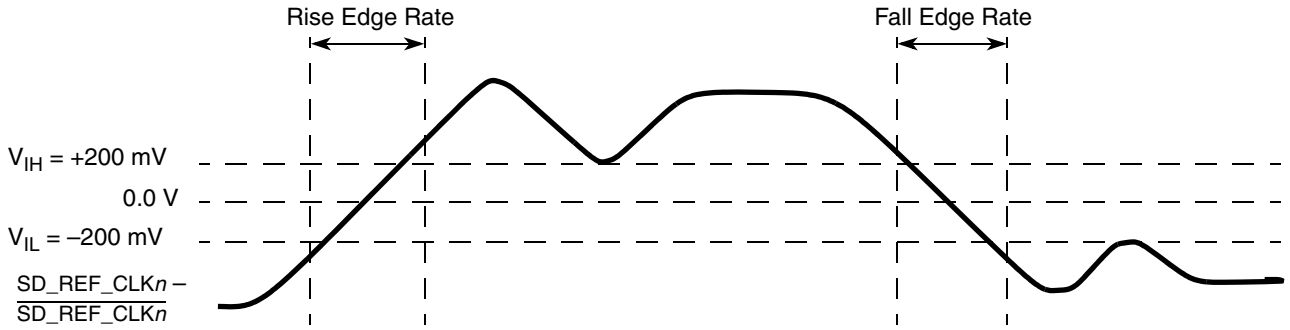


Figure 37. Differential Measurement Points for Rise and Fall Time

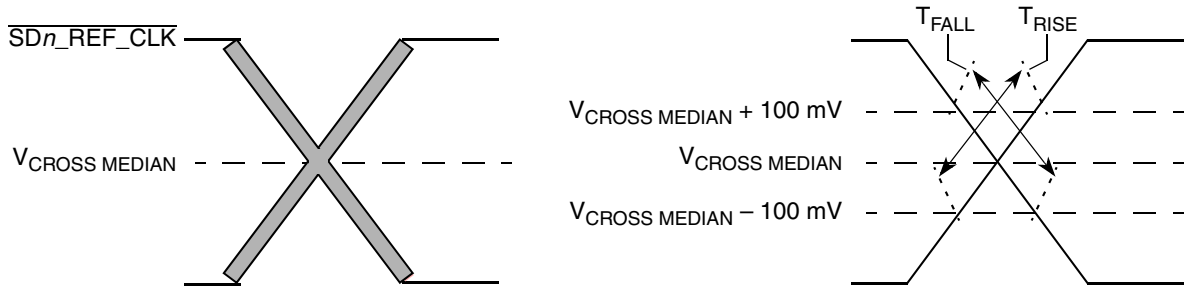


Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 Spread Spectrum Clock

SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

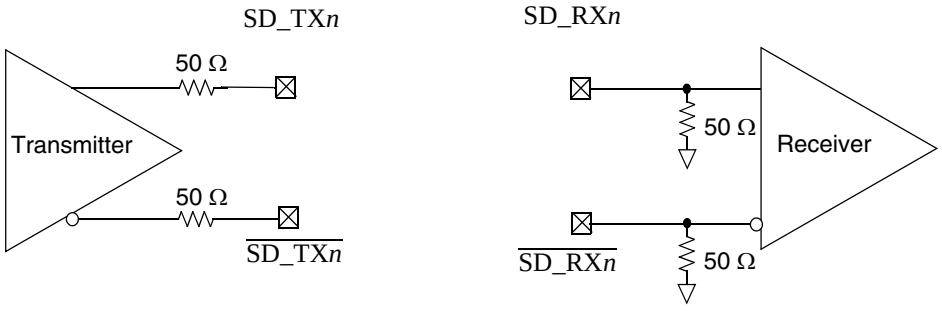


Figure 39. SerDes Transmitter and Receiver Reference Circuits

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 2i/3G Receiver (Rx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:
1. Measured at receiver.

2.20.8 SGMII Interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the device, as shown in Figure 44, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 39.

2.20.8.0.1 SGMII Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK[1:2] and $\overline{\text{SD\_REF\_CLK}[1:2]}$ pins. SerDes banks 1–2 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, “SerDes Reference Clocks.”

2.20.8.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.1.1 SGMII Transmit DC Timing Specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) as shown in Figure 45.

Table 87. SGMII DC Transmitter Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1

"e500mc Core Cluster to SYSCLK PLL Ratio." The frequency for each core complex 0–3 is selected using the configuration bits as described in Table 96.

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Platform to SYSCLK PLL Ratio."
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in Section 3.1.5, "DDR Controller PLL Ratios."
- Each of the three SerDes blocks has a PLL which generate a core clock from their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.6, "Frequency Options."

3.1.1 Clock Ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 93. Processor Clocking Specifications

Parameter	Maximum Processor Core Frequency								Unit	Note
	667 MHz		800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500mc core PLL frequency	667	667	667	800	667	1000	667	1200	MHz	1,4
e500mc core frequency	333	667	333	800	333	1000	333	1200	MHz	4, 8
Platform clock frequency	400	533	400	533	400	533	400	600	MHz	1
Memory bus clock frequency	400	533	400	533	400	533	400	600	MHz	1,2,5,6
Local bus clock frequency	—	67	—	67	—	67	—	75	MHz	3
PME	—	267	—	267	—	267	—	300	MHz	7
FMan	—	467	—	467	—	467	—	500	MHz	—

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500-mc core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e500mc (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3 memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the chip reference manual for more information.
4. The e500mc core can run at e500mc core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 667 MHz, this results in a minimum allowable e500mc core frequency of 333 MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. The PME runs synchronously to the platform clock, running at a frequency of platform clock/2.
8. Core frequency must be at least as fast as the platform frequency (Rev 1.1 silicon).

3.3 Power Supply Design

This section discusses the power supply design.

3.3.1 PLL Power Supply Filtering

Each of the PLLs described in Section 3.1, "System Clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, AV_{DD_CCn} and AV_{DD_DDR} voltages must be derived directly from the $V_{DD\_CA\_CB\_PL}$ source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 50, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 50 shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%

C1 = 10µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH

C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD}.

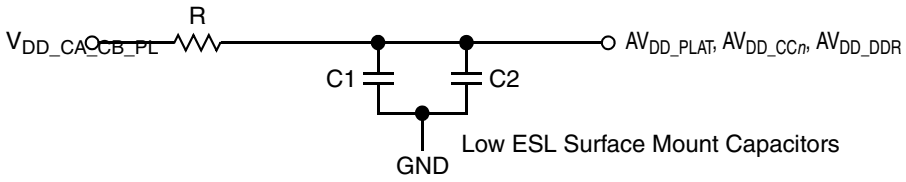
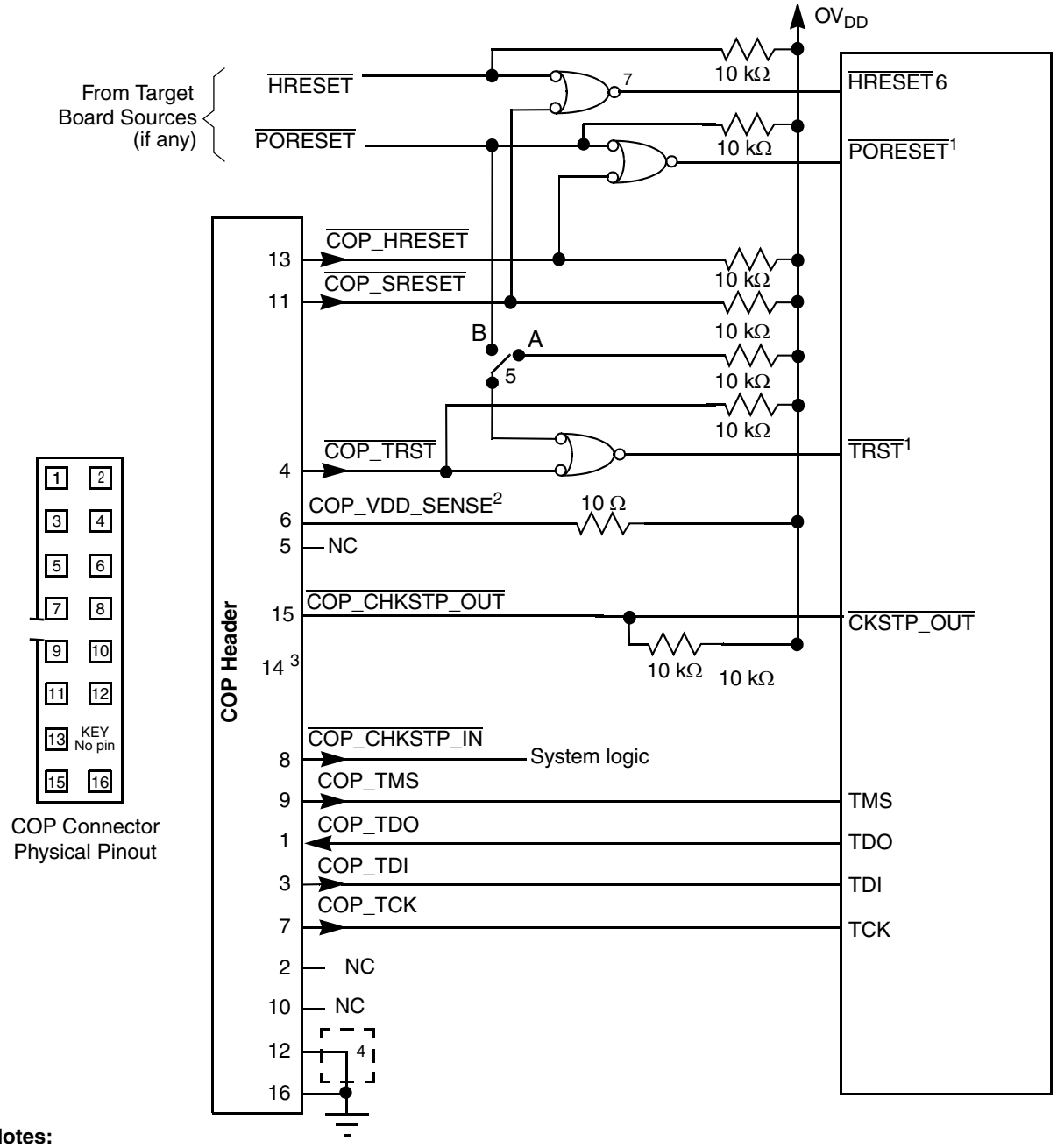


Figure 50. PLL Power Supply Filter Circuit

The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 51. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn}



Notes:

1. The COP port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
6. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.
7. This is an open-drain gate.

Figure 55. Legacy JTAG Interface Connection

3.6.3 Guidelines for High-Speed Interface Termination

This section provides the guidelines for when the SerDes interface is either entirely unused or partly unused.

3.6.3.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[7:2], SD_TX[13:10]
- $\overline{\text{SD\_TX}}$[7:2], $\overline{\text{SD\_TX}}$[13:10]
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[7:2], SD_RX[13:10]
- $\overline{\text{SD\_RX}}$[13:10], $\overline{\text{SD\_RX}}$[13:10]
- SD_REF_CLK1, SD_REF_CLK2
- $\overline{\text{SD\_REF\_CLK1}}$, $\overline{\text{SD\_REF\_CLK2}}$

In the RCW configuration fields SRDS_LPD_B1 and SRDS_LPD_B2, all bits must be set to power down all the lanes in each bank.

RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN] = 0 power-downs the PLLs of both banks.

Additionally, software may configure SRDSB*n*RSTCTL[SDRD] = 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both SV_{DD} and XV_{DD} must remain powered.

3.6.3.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following unused pins must be left unconnected:

- SD_TX[*n*]
- $\overline{\text{SD\_TX}}$[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*]
- $\overline{\text{SD\_RX}}$[*n*]
- SD_REF_CLK1, $\overline{\text{SD\_REF\_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD\_REF\_CLK2}}$ (If entire SerDes bank 2 unused)

In the RCW configuration field for each bank SRDS_LPD_B*n* with unused lanes, the respective bit for each unused lane must be set to power down the lane.

3.6.4 USB Controller Connections

This section details the hardware connections required for the USB controllers.