**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500mc |
| Number of Cores/Bus Width | 4 Core, 32-Bit |
| Speed | 800MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR3, DDR3L |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (5) |
| SATA | SATA 3Gbps (2) |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | - |
| Supplier Device Package | 780-FCPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p2040nsn7hlc |

## 1.1 780 FC-PBGA Ball Layout Diagrams

These figures show the FC-PBGA ball map diagrams.

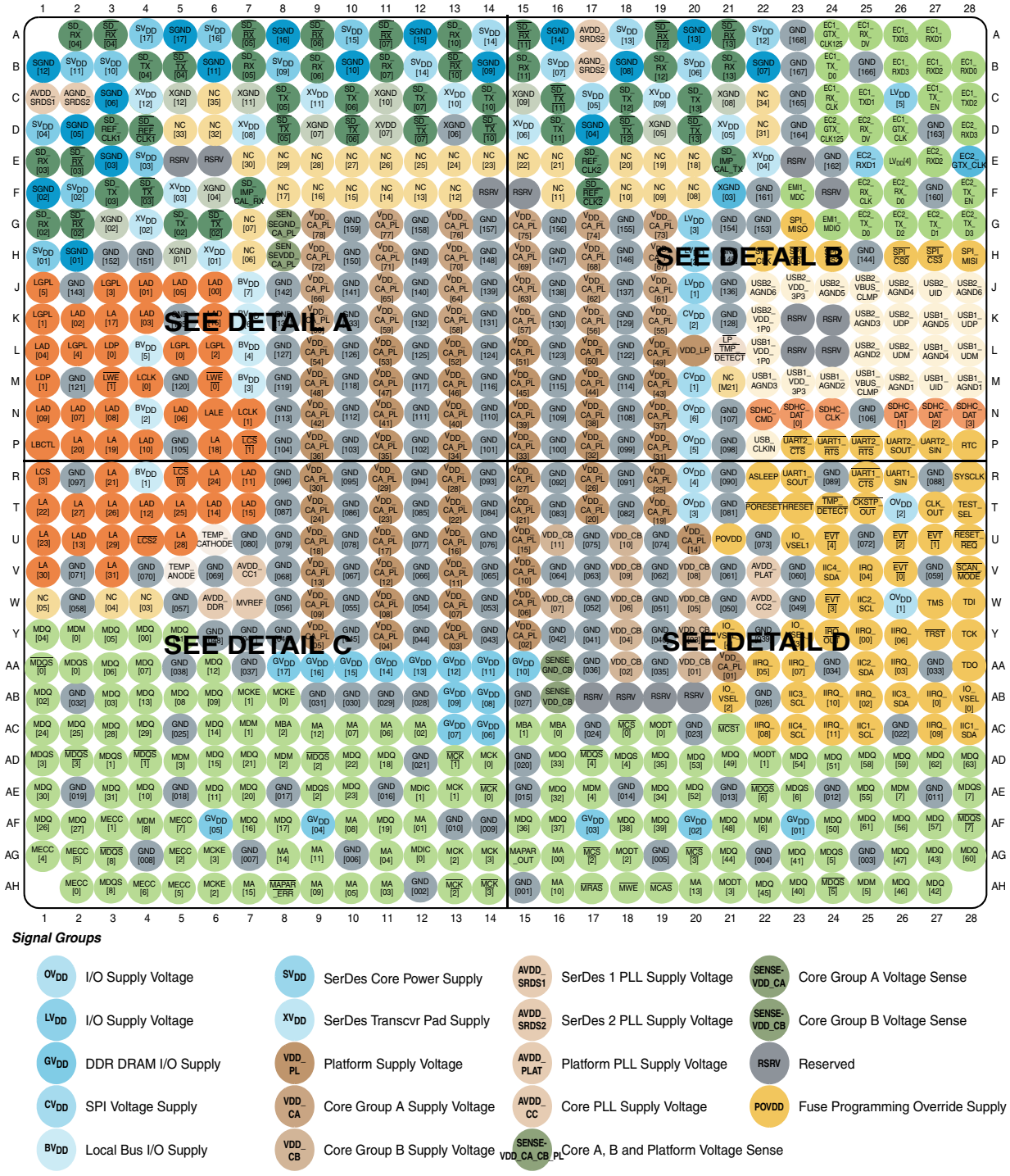



**Figure 2. 780 BGA Ball Map Diagram (Top View)**

## 1.2 Pinout List

This table provides the pinout listing for the 780 FC-PBGA package by bus. Pins for multiplexed signals appear in the bus group for their default status and have a corresponding note stating that they have multiple functionality depending on the mode in which they are configured.

**Table 1. Pin List by Bus**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| **DDR SDRAM Memory Interface** | | | | | |
| MDQ00 | Data | Y4 | I/O | $GV_{DD}$ | — |
| MDQ01 | Data | Y5 | I/O | $GV_{DD}$ | — |
| MDQ02 | Data | AB1 | I/O | $GV_{DD}$ | — |
| MDQ03 | Data | AB3 | I/O | $GV_{DD}$ | — |
| MDQ04 | Data | Y1 | I/O | $GV_{DD}$ | — |
| MDQ05 | Data | Y3 | I/O | $GV_{DD}$ | — |
| MDQ06 | Data | AA3 | I/O | $GV_{DD}$ | — |
| MDQ07 | Data | AA4 | I/O | $GV_{DD}$ | — |
| MDQ08 | Data | AB5 | I/O | $GV_{DD}$ | — |
| MDQ09 | Data | AB6 | I/O | $GV_{DD}$ | — |
| MDQ10 | Data | AE4 | I/O | $GV_{DD}$ | — |
| MDQ11 | Data | AE6 | I/O | $GV_{DD}$ | — |
| MDQ12 | Data | AA6 | I/O | $GV_{DD}$ | — |
| MDQ13 | Data | AB4 | I/O | $GV_{DD}$ | — |
| MDQ14 | Data | AC6 | I/O | $GV_{DD}$ | — |
| MDQ15 | Data | AD6 | I/O | $GV_{DD}$ | — |
| MDQ16 | Data | AF7 | I/O | $GV_{DD}$ | — |
| MDQ17 | Data | AF8 | I/O | $GV_{DD}$ | — |
| MDQ18 | Data | AD11 | I/O | $GV_{DD}$ | — |
| MDQ19 | Data | AF11 | I/O | $GV_{DD}$ | — |
| MDQ20 | Data | AE7 | I/O | $GV_{DD}$ | — |
| MDQ21 | Data | AD7 | I/O | $GV_{DD}$ | — |
| MDQ22 | Data | AD10 | I/O | $GV_{DD}$ | — |
| MDQ23 | Data | AE10 | I/O | $GV_{DD}$ | — |
| MDQ24 | Data | AC1 | I/O | $GV_{DD}$ | — |
| MDQ25 | Data | AC2 | I/O | $GV_{DD}$ | — |
| MDQ26 | Data | AF1 | I/O | $GV_{DD}$ | — |
| MDQ27 | Data | AF2 | I/O | $GV_{DD}$ | — |
| MDQ28 | Data | AC3 | I/O | $GV_{DD}$ | — |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| IRQ05/GPIO23/DMA2_DDONE0 | External Interrupts | AA22 | I | $OV_{DD}$ | 24 |
| IRQ06/GPIO24/USB1_DRVVBUS | External Interrupts | Y26 | I | $OV_{DD}$ | 24 |
| IRQ07/GPIO25/USB1_PWRFAULT | External Interrupts | AA23 | I | $OV_{DD}$ | 24 |
| IRQ08/GPIO26/USB2_DRVVBUS | External Interrupts | AC22 | I | $OV_{DD}$ | 24 |
| IRQ09/GPIO27/USB2_PWRFAULT | External Interrupts | AC27 | I | $OV_{DD}$ | 24 |
| IRQ10/GPIO28/EVT7 | External Interrupts | AB24 | I | $OV_{DD}$ | 24 |
| IRQ11/GPIO29/EVT8 | External Interrupts | AC24 | I | $OV_{DD}$ | 24 |
| IRQ_OUT/EVT9 | Interrupt Output | Y24 | O | $OV_{DD}$ | 1, 2, 24 |
| **Trust** | | | | | |
| TMP_DETECT | Tamper Detect | T24 | I | $OV_{DD}$ | 25 |
| LP_TMP_DETECT | Low Power Tamper Detect | L21 | I | $V_{DD\_LP}$ | 25 |
| **eSDHC** | | | | | |
| SDHC_CMD | Command/Response | N22 | I/O | $CV_{DD}$ | — |
| SDHC_DAT0 | Data | N23 | I/O | $CV_{DD}$ | — |
| SDHC_DAT1 | Data | N26 | I/O | $CV_{DD}$ | — |
| SDHC_DAT2 | Data | N27 | I/O | $CV_{DD}$ | — |
| SDHC_DAT3 | Data | N28 | I/O | $CV_{DD}$ | — |
| SDHC_DAT4/SPI_CS0/GPIO00 | Data | H26 | I/O | $CV_{DD}$ | 24, 28 |
| SDHC_DAT5/SPI_CS1/GPIO01 | Data | H23 | I/O | $CV_{DD}$ | 24, 28 |
| SDHC_DAT6/SPI_CS2/GPIO02 | Data | H27 | I/O | $CV_{DD}$ | 24, 28 |
| SDHC_DAT7/SPI_CS3/GPIO03 | Data | H24 | I/O | $CV_{DD}$ | 24, 28 |
| SDHC_CLK | Host to Card Clock | N24 | O | $OV_{DD}$ | — |
| SDHC_CD/IIC3_SCL/GPIO16/ M1DVAL/LB_DVAL/DMA1_DACK0 | Card Detection | AB23 | I/O | $OV_{DD}$ | 24, 28 |
| SDHC_WP/IIC3_SDA/GPIO17/ M1SRCID0/LB_SRCID0/DMA1_DDONE0 | Card Write Protection | AB26 | I | $OV_{DD}$ | 24, 28 |
| **eSPI** | | | | | |
| SPI_MOSI | Master Out Slave In | H28 | I/O | $CV_{DD}$ | — |
| SPI_MISO | Master In Slave Out | G23 | I | $CV_{DD}$ | — |
| SPI_CLK | eSPI Clock | H22 | O | $CV_{DD}$ | — |
| SPI_CS0/SDHC_DAT4/GPIO00 | eSPI Chip Select | H26 | O | $CV_{DD}$ | 24 |
| SPI_CS1/SDHC_DAT5/GPIO01 | eSPI Chip Select | H23 | O | $CV_{DD}$ | 24 |
| SPI_CS2/SDHC_DAT6/GPIO02 | eSPI Chip Select | H27 | O | $CV_{DD}$ | 24 |
| SPI_CS3/SDHC_DAT7/GPIO03 | eSPI Chip Select | H24 | O | $CV_{DD}$ | 24 |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| SD_RX04 | Receive Data (positive) | A2 | I | $XV_{DD}$ | — |
| SD_RX03 | Receive Data (positive) | E1 | I | $XV_{DD}$ | — |
| SD_RX02 | Receive Data (positive) | G1 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX13}}$ | Receive Data (negative) | A21 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX12}}$ | Receive Data (negative) | A19 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX11}}$ | Receive Data (negative) | A15 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX10}}$ | Receive Data (negative) | B13 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX07}}$ | Receive Data (negative) | A11 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX06}}$ | Receive Data (negative) | A9 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX05}}$ | Receive Data (negative) | A7 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX04}}$ | Receive Data (negative) | A3 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX03}}$ | Receive Data (negative) | E2 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX02}}$ | Receive Data (negative) | G2 | I | $XV_{DD}$ | — |
| SD_REF_CLK1 | SerDes Bank 1 PLL Reference Clock | D3 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK1}}$ | SerDes Bank 1 PLL Reference Clock Complement | D4 | I | $XV_{DD}$ | — |
| SD_REF_CLK2 | SerDes Bank 2 PLL Reference Clock | E17 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK2}}$ | SerDes Bank 2 PLL Reference Clock Complement | F17 | I | $XV_{DD}$ | — |
| **General-Purpose Input/Output** | | | | | |
| GPIO00/$\overline{\text{SPI\_CS0}}$/SDHC_DATA4 | General Purpose Input/Output | H26 | I/O | $CV_{DD}$ | — |
| GPIO01/$\overline{\text{SPI\_CS1}}$/SDHC_DATA5 | General Purpose Input/Output | H23 | I/O | $CV_{DD}$ | — |
| GPIO02/$\overline{\text{SPI\_CS2}}$/SDHC_DATA6 | General Purpose Input/Output | H27 | I/O | $CV_{DD}$ | — |
| GPIO03$\overline{\text{SPI_CS3}}$/SDHC_DATA7 | General Purpose Input/Output | H24 | I/O | $CV_{DD}$ | — |
| GPIO08/UART1_SOUT | General Purpose Input/Output | R23 | I/O | $OV_{DD}$ | — |
| GPIO09/UART2_SOUT | General Purpose Input/Output | P26 | I/O | $OV_{DD}$ | — |
| GPIO10/UART1_SIN | General Purpose Input/Output | R26 | I/O | $OV_{DD}$ | — |
| GPIO11/UART2_SIN | General Purpose Input/Output | P27 | I/O | $OV_{DD}$ | — |
| GPIO12/$\overline{\text{UART1\_RTS}}$/UART3_SOUT | General Purpose Input/Output | P24 | I/O | $OV_{DD}$ | — |
| GPIO13/$\overline{\text{UART2\_RTS}}$/UART4_SOUT | General Purpose Input/Output | P25 | I/O | $OV_{DD}$ | — |
| GPIO14/$\overline{\text{UART1\_CTS}}$/UART3_SIN | General Purpose Input/Output | R25 | I/O | $OV_{DD}$ | — |
| GPIO15/$\overline{\text{UART2\_CTS}}$/UART4_SIN | General Purpose Input/Output | P23 | I/O | $OV_{DD}$ | — |
| GPIO16/IIC3_SCL/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/$\overline{\text{SDHC\_CD}}$ | General Purpose Input/Output | AB23 | I/O | $OV_{DD}$ | — |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| GND098 | Ground | P21 | — | — | — |
| GND097 | Ground | R2 | — | — | — |
| GND096 | Ground | R8 | — | — | — |
| GND095 | Ground | R10 | — | — | — |
| GND094 | Ground | R12 | — | — | — |
| GND093 | Ground | R14 | — | — | — |
| GND092 | Ground | R16 | — | — | — |
| GND091 | Ground | R18 | — | — | — |
| GND090 | Ground | R21 | — | — | — |
| GND089 | Ground | R24 | — | — | — |
| GND088 | Ground | R27 | — | — | — |
| GND087 | Ground | T8 | — | — | — |
| GND086 | Ground | T10 | — | — | — |
| GND085 | Ground | T12 | — | — | — |
| GND084 | Ground | T14 | — | — | — |
| GND083 | Ground | T16 | — | — | — |
| GND082 | Ground | T18 | — | — | — |
| GND081 | Ground | T21 | — | — | — |
| GND080 | Ground | U7 | — | — | — |
| GND079 | Ground | U8 | — | — | — |
| GND078 | Ground | U10 | — | — | — |
| GND077 | Ground | U12 | — | — | — |
| GND076 | Ground | U14 | — | — | — |
| GND075 | Ground | U17 | — | — | — |
| GND074 | Ground | U19 | — | — | — |
| GND073 | Ground | U22 | — | — | — |
| GND072 | Ground | U25 | — | — | — |
| GND071 | Ground | V2 | — | — | — |
| GND070 | Ground | V4 | — | — | — |
| GND069 | Ground | V6 | — | — | — |
| GND068 | Ground | V8 | — | — | — |
| GND067 | Ground | V10 | — | — | — |
| GND066 | Ground | V12 | — | — | — |
| GND065 | Ground | V14 | — | — | — |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| XGND08 | SerDes Transceiver GND | C21 | — | — | — |
| XGND07 | SerDes Transceiver GND | D9 | — | — | — |
| XGND06 | SerDes Transceiver GND | D13 | — | — | — |
| XGND05 | SerDes Transceiver GND | D19 | — | — | — |
| XGND04 | SerDes Transceiver GND | F6 | — | — | — |
| XGND03 | SerDes Transceiver GND | F21 | — | — | — |
| XGND02 | SerDes Transceiver GND | G3 | — | — | — |
| XGND01 | SerDes Transceiver GND | H5 | — | — | — |
| SGND17 | SerDes Core Logic GND | A5 | — | — | — |
| SGND16 | SerDes Core Logic GND | A8 | — | — | — |
| SGND15 | SerDes Core Logic GND | A12 | — | — | — |
| SGND14 | SerDes Core Logic GND | A16 | — | — | — |
| SGND13 | SerDes Core Logic GND | A20 | — | — | — |
| SGND12 | SerDes Core Logic GND | B1 | — | — | — |
| SGND11 | SerDes Core Logic GND | B6 | — | — | — |
| SGND10 | SerDes Core Logic GND | B10 | — | — | — |
| SGND09 | SerDes Core Logic GND | B14 | — | — | — |
| SGND08 | SerDes Core Logic GND | B18 | — | — | — |
| SGND07 | SerDes Core Logic GND | B22 | — | — | — |
| SGND06 | SerDes Core Logic GND | C3 | — | — | — |
| SGND05 | SerDes Core Logic GND | D2 | — | — | — |
| SGND04 | SerDes Core Logic GND | D17 | — | — | — |
| SGND03 | SerDes Core Logic GND | E3 | — | — | — |
| SGND02 | SerDes Core Logic GND | F1 | — | — | — |
| SGND01 | SerDes Core Logic GND | H2 | — | — | — |
| AGND_SRDS1 | SerDes PLL1 GND | C2 | — | — | — |
| AGND_SRDS2 | SerDes PLL2 GND | B17 | — | — | — |
| SENSEGND_CA_PL | Core Group A and Platform GND Sense | G8 | — | — | 8 |
| SENSEGND_CB | Core Group B GND Sense | AA16 | — | — | 8 |
| USB1_AGND06 | USB1 PHY Transceiver GND | J28 | — | — | — |
| USB1_AGND05 | USB1 PHY Transceiver GND | K27 | — | — | — |
| USB1_AGND04 | USB1 PHY Transceiver GND | L27 | — | — | — |
| USB1_AGND03 | USB1 PHY Transceiver GND | M22 | — | — | — |
| USB1_AGND02 | USB1 PHY Transceiver GND | M24 | — | — | — |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| VDD_CA_PL16 | Core Group A and Platform Supply | U13 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL15 | Core Group A and Platform Supply | U15 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL14 | Core Group A and Platform Supply | U20 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL13 | Core Group A and Platform Supply | V9 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL12 | Core Group A and Platform Supply | V11 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL11 | Core Group A and Platform Supply | V13 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL10 | Core Group A and Platform Supply | V15 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL09 | Core Group A and Platform Supply | W9 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL08 | Core Group A and Platform Supply | W11 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL07 | Core Group A and Platform Supply | W13 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL06 | Core Group A and Platform Supply | W15 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL05 | Core Group A and Platform Supply | Y9 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL04 | Core Group A and Platform Supply | Y11 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL03 | Core Group A and Platform Supply | Y13 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL02 | Core Group A and Platform Supply | Y15 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CA_PL01 | Core Group A and Platform Supply | AA21 | — | $V_{DD\_CA\_PL}$ | 37 |
| VDD_CB11 | Core Group B Supply | U16 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB10 | Core Group B Supply | U18 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB09 | Core Group B Supply | V18 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB08 | Core Group B Supply | V20 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB07 | Core Group B Supply | W16 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB06 | Core Group B Supply | W18 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB05 | Core Group B Supply | W20 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB04 | Core Group B Supply | Y18 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB03 | Core Group B Supply | Y20 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB02 | Core Group B Supply | AA18 | — | $V_{DD\_CB}$ | 37 |
| VDD_CB01 | Core Group B Supply | AA20 | — | $V_{DD\_CB}$ | 37 |
| VDD_LP | Low Power Security Monitor Supply | L20 | — | $V_{DD\_LP}$ | 25 |
| AVDD_CC1 | Core Cluster PLL1 Supply | V7 | — | — | 13 |
| AVDD_CC2 | Core Cluster PLL2 Supply | W22 | — | — | 13 |
| AVDD_PLAT | Platform PLL Supply | V22 | — | — | 13 |
| AVDD_DDR | DDR PLL Supply | W6 | — | — | 13 |
| AVDD_SRDS1 | SerDes PLL1 Supply | C1 | — | — | 13 |
| AVDD_SRDS2 | SerDes PLL2 Supply | A17 | — | — | 13 |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| SENSEVDD_CA_PL | Core Group A and Platform Vdd Sense | H8 | — | — | 8 |
| SENSEVDD_CB | Core Group B Vdd Sense | AB16 | — | — | 8 |
| USB1_VDD_3P3 | USB1 PHY Transceiver 3.3 V Supply | M23 | — | — | — |
| USB2_VDD_3P3 | USB2 PHY Transceiver 3.3 V Supply | J23 | — | — | — |
| USB1_VDD_1P0 | USB1 PHY PLL 1.0 V Supply | L22 | — | — | — |
| USB2_VDD_1P0 | USB2 PHY PLL 1.0 V Supply | K22 | — | — | — |
| **Analog Signals** | | | | | |
| MVREF | SSTL_1.5/1.35 Reference Voltage | W7 | I | $GV_{DD}/2$ | — |
| SD_IMP_CAL_TX | SerDes Tx Impedance Calibration | E21 | I | 200Ω (±1%) to $XV_{DD}$ | 21 |
| SD_IMP_CAL_RX | SerDes Rx Impedance Calibration | F7 | I | 200Ω (±1%) to $SV_{DD}$ | 22 |
| TEMP_ANODE | Temperature Diode Anode | V5 | — | internal diode | 9 |
| TEMP_CATHODE | Temperature Diode Cathode | U6 | — | internal diode | 9 |
| USB2_IBIAS_REXT | USB PHY2 Reference Bias Current Generation | K23 | — | GND | 32 |
| USB1_IBIAS_REXT | USB PHY1 Reference Bias Current Generation | L23 | — | GND | 32 |
| USB2_VDD_1P8_DECAP | USB2 PHY 1.8 V Output to External Decap | K24 | — | GND | 33 |
| USB1_VDD_1P8_DECAP | USB1 PHY 1.8 V Output to External Decap | L24 | — | GND | 33 |
| **No Connection Pins** | | | | | |
| NC03 | No Connection | W4 | — | — | 11 |
| NC04 | No Connection | W3 | — | — | 11 |
| NC05 | No Connection | W1 | — | — | 11 |
| NC06 | No Connection | H7 | — | — | 11 |
| NC07 | No Connection | G7 | — | — | 11 |
| NC08 | No Connection | F20 | — | — | 11 |
| NC09 | No Connection | F19 | — | — | 11 |
| NC10 | No Connection | F18 | — | — | 11 |
| NC11 | No Connection | F16 | — | — | 11 |
| NC12 | No Connection | F13 | — | — | 11 |

### 2.1.3 Output Driver Characteristics

This table provides information about the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 4. Output Drive Capability**

| Driver Type | Output Impedance (Ω) | (Nominal) Supply Voltage | Note |
|---|---|---|---|
| Local Bus interface utilities signals | 45<br>45<br>45 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V<br>$BV_{DD}$ = 1.8 V | — |
| DDR3 signal | 20 (full-strength mode)<br>40 (half-strength mode) | $GV_{DD}$ = 1.5 V | 1 |
| DDR3L signal | 20 (full-strength mode)<br>40 (half-strength mode) | $GV_{DD}$ = 1.35 V | 1 |
| eTSEC/10/100 signals | 45<br>45 | $LV_{DD}$ = 3.3 V<br>$LV_{DD}$ = 2.5 V | — |
| DUART, system control, JTAG | 45 | $OV_{DD}$ = 3.3 V | — |
| $I^2C$ | 45 | $OV_{DD}$ = 3.3 V | — |
| eSPI, eSDHC | 45<br>45<br>45 | $CV_{DD}$ = 3.3 V<br>$CV_{DD}$ = 2.5 V<br>$CV_{DD}$ =1.8 V | — |

**Note:**

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at $T_j$ = 105 °C and at $GV_{DD}$ (min).

## 2.2 Power Up Sequencing

The device requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. Bring up $OV_{DD}$, $LV_{DD}$, $BV_{DD}$, $CV_{DD}$, and USB_$V_{DD}$_3P3. Drive $POV_{DD}$ = GND.
   - — $\overline{\text{PORESET}}$ input must be driven asserted and held during this step.
   - — IO_VSEL inputs must be driven during this step and held stable during normal operation.
   - — USB_$V_{DD}$_3P3 rise time (10% to 90%) has a minimum of 350 µs.
2. Bring up $V_{DD\_CA\_CB\_PL}$, $SV_{DD}$, $AV_{DD}$ (cores, platform, SerDes) and USB_$V_{DD}$_1P0. $V_{DD\_CA\_CB\_PL}$ and USB_$V_{DD}$_1P0 must be ramped up simultaneously.
3. Bring up $GV_{DD}$ (DDR) and $XV_{DD}$.
4. Negate $\overline{\text{PORESET}}$ input as long as the required assertion/hold time has been met per Table 17.
5. For secure boot fuse programming: After negation of $\overline{\text{PORESET}}$, drive $POV_{DD}$ = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return $POV_{DD}$ = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5. See Section 5, "Security Fuse Processor," for additional details.

**WARNING**

Only two secure boot fuse programming events are permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while $POV_{DD}$ driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while $POV_{DD}$ = GND.

While VDD is ramping, current may be supplied from VDD through the chip to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

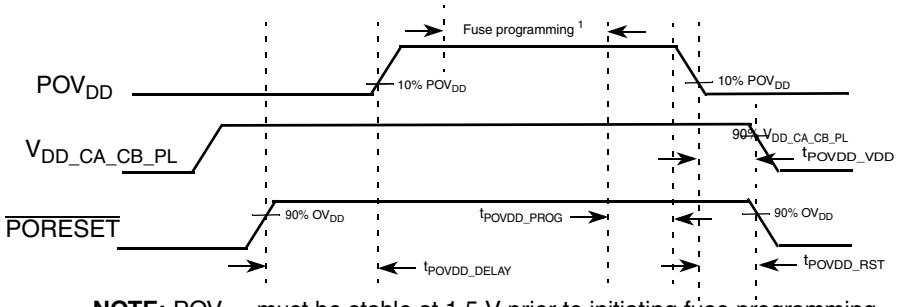
**WARNING**

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the $POV_{DD}$ timing diagram.




**NOTE:** $POV_{DD}$ must be stable at 1.5 V prior to initiating fuse programming.

**Figure 8. $POV_{DD}$ Timing Diagram**

This table provides information on the power-down and power-up sequence parameters for $POV_{DD}$.

**Table 5. $POV_{DD}$ Timing [5]**

| Driver Type | Min | Max | Unit | Note |
|---|---|---|---|---|
| $t_{POVDD\_DELAY}$ | 100 | — | SYSCLKs | 1 |
| $t_{POVDD\_PROG}$ | 0 | — | µs | 2 |
| $t_{POVDD\_VDD}$ | 0 | — | µs | 3 |
| $t_{POVDD\_RST}$ | 0 | — | µs | 4 |

**Note:**

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving $POV_{DD}$ ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% $OV_{DD}$ to 10% $POV_{DD}$ ramp up.
2. Delay required from fuse programming finished to $POV_{DD}$ ramp down start. Fuse programming must complete while $POV_{DD}$ is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while $POV_{DD}$ driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while $POV_{DD}$ = GND. After fuse programming is completed, it is required to return $POV_{DD}$ = GND.
3. Delay required from $POV_{DD}$ ramp down complete to $V_{DD\_CA\_CB\_PL}$ ramp down start. $POV_{DD}$ must be grounded to minimum 10% $POV_{DD}$ before $V_{DD\_CA\_CB\_PL}$ is at 90% $V_{DD}$.
4. Delay required from $POV_{DD}$ ramp down complete to $\overline{\text{PORESET}}$ assertion. $POV_{DD}$ must be grounded to minimum 10% $POV_{DD}$ before $\overline{\text{PORESET}}$ assertion reaches 90% $OV_{DD}$.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for $GV_{DD}$ is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for $GV_{DD}$ is not required.

**WARNING**

Incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply Power Default Setting."

**NOTE**

From a system standpoint, if any of the I/O power supplies ramp prior to the $V_{DD\_CA\_CB\_PL}$ supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

## 2.3 Power Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power Up Sequencing," it is required that $POV_{DD}$ = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5.

$V_{DD\_CA\_CB\_PL}$ and USB_$V_{DD}$_1P0 must be ramped down simultaneously. USB_$V_{DD}$_1P8_DECAP should starts ramping down only after USB_$V_{DD}$_3P3 is below 1.65 V.

## 2.4 Power Characteristics

This table shows the power dissipations of the $V_{DD\_CA\_CB\_PL}$ supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

**Table 6. Device Power Dissipation**

| Power Mode | Core Freq (MHz) | Plat Freq (MHz) | DDR Data Rate (MT/s) | FM Freq (MHz) | $V_{DD\_CA\_CB\_PL}$ (V) | Junction Temp (°C) | Core & Platform Power[1] (W) | $V_{DD\_CA\_CB\_PL}$ Power (W) | Core & Platform Power[1] (W) | $V_{DD\_CA\_CB\_PL}$ Power (W) | $SV_{DD}$ Power (W) | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Quad Cores | | Dual Cores | | | |
| Typical | 1200 | 600 | 1200 | 500 | 1.0 | 65 | 10.3 | — | 9.8 | — | — | 2, 3 |
| Thermal | | | | | | 105 | 14.2 | — | 13.8 | — | — | 5, 7 |
| Maximum | | | | | | | 14.8 | 13.5 | 14.0 | 12.8 | 1.4 | 4, 6, 7 |
| Typical | 1000 | 533 | 1067 | 467 | 1.0 | 65 | 9.2 | — | 8.6 | — | — | 2, 3 |
| Thermal | | | | | | 105 | 12.5 | — | 12.1 | — | — | 5, 7 |
| Maximum | | | | | | | 13.0 | 11.7 | 12.3 | 11.0 | 1.4 | 4, 6, 7 |
| Typical | 800 | 534 | 1067 | 467 | 1.0 | 65 | 9.0 | — | 8.4 | — | — | 2, 3 |
| Thermal | | | | | | 105 | 12.2 | — | 12.0 | — | — | 5, 7 |
| Maximum | | | | | | | 12.6 | 11.4 | 12.1 | 10.9 | 1.4 | 4, 6, 7 |

### 2.12.2.2 RGMII AC Timing Specifications

This table shows the RGMII AC timing specifications.

**Table 37. RGMII AC Timing Specifications**

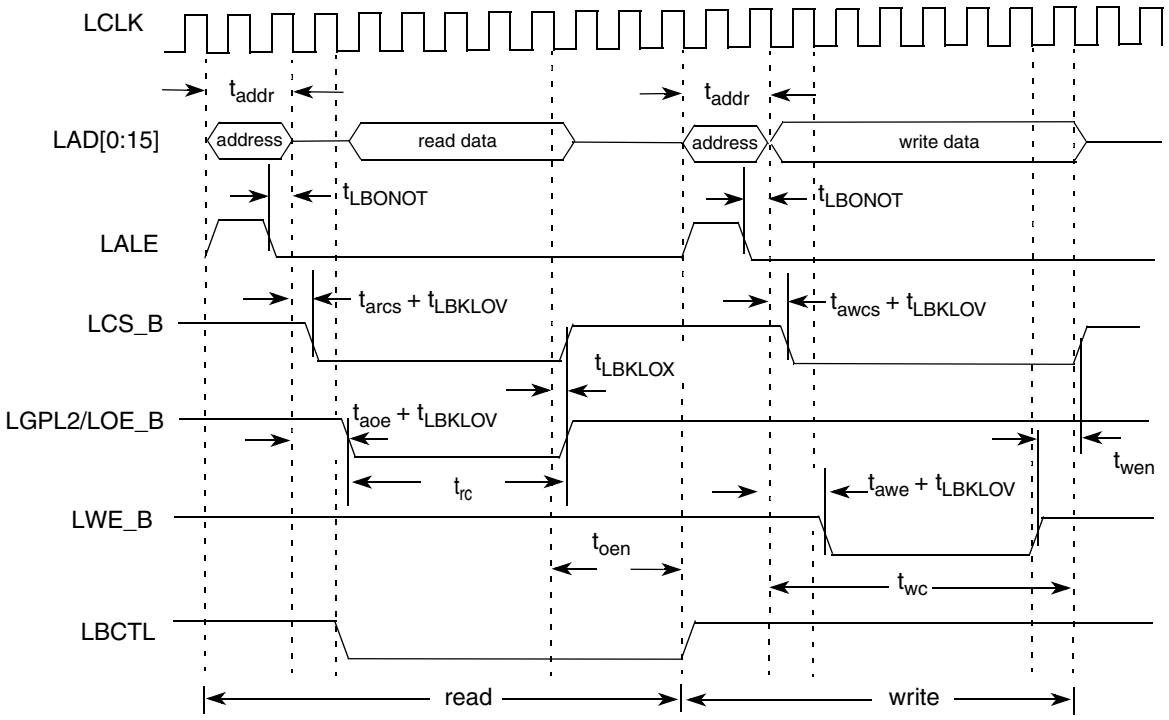
For recommended operating conditions, see Table 3.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT\_TX}$ | –500 | 0 | 500 | ps | 5 |
| Data to clock input skew (at receiver) | $t_{SKRGT\_RX}$ | 1.0 | — | 2.8 | ns | 2 |
| Clock period duration | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns | 3 |
| Duty cycle for 10BASE-T and 100BASE-TX | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % | 3, 4 |
| Duty cycle for Gigabit | $t_{RGTH}/t_{RGT}$ | 45 | 50 | 55 | % | — |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns | — |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns | — |

**Note:**

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300ppm.

This figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.




1 $t_{addr}$ is programmable and determined by LCRR[EADC] and ORx[EAD].

2 $t_{arcs}$, $t_{awcs}$, $t_{aoe}$, $t_{rc}$, $t_{oen}$, $t_{awe}$, $t_{wc}$, $t_{wen}$ are determined by ORx. See the chip reference manual.

**Figure 22. GPCM Output Timing Diagram**

## 2.15 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

### 2.15.1 eSDHC DC Electrical Characteristics

This table provides the eSDHC electrical characteristics.

**Table 50. eSDHC Interface DC Electrical Characteristics**

For recommended operating conditions, see Table 3.

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | $0.625 \times CV_{DD}$ | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | — | $0.25 \times CV_{DD}$ | V | 1 |
| Input/output leakage current | $I_{IN}/I_{OZ}$ | — | –50 | 50 | μA | — |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –100 μA at $CV_{DD}$ min | $0.75 \times CV_{DD}$ | — | V | — |

**Table 56. $I^2C$ DC Electrical Characteristics ($OV_{DD}$ = 3.3 V) (continued)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max) | $I_I$ | –40 | 40 | μA | 4 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Note:**

1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 2.18.2 $I^2C$ AC Electrical Specifications

This table provides the $I^2C$ AC timing specifications.

**Table 57. $I^2C$ AC Timing Specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz | 2 |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs | — |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs | — |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs | — |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs | — |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns | — |
| Data input hold time:<br>CBUS compatible masters<br>$I^2C$ bus devices | $t_{I2DXKL}$ | <br>—<br>0 | <br>—<br>— | μs | 3 |
| Data output delay time | $t_{I2OVKL}$ | — | 0.9 | μs | 4 |
| Setup time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | μs | — |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | μs | — |

## 2.19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

**Table 60. GPIO Input AC Timing Specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Unit | Note |
|---|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns | 1 |

**Note:**

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ to ensure proper operation.

This figure provides the AC test load for the GPIO.

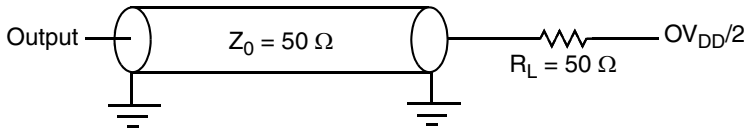



**Figure 31. GPIO AC Test Load**

## 2.20 High-Speed Serial Interfaces (HSSI)

The device features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, Aurora, and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

## 2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

#### 2.20.7.1.2 SATA DC Receiver (Rx) Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

**Table 80. Gen1i/1.5 G Receiver (Rx) Input DC Specifications ($XV_{DD}$ = 1.5 V or 1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential input voltage | $V_{SATA\_RXDIFF}$ | 240 | — | 600 | mV p-p | 1 |
| Differential Rx input impedance | $Z_{SATA\_RXSEIM}$ | 85 | 100 | 115 | Ω | — |
| OOB signal detection threshold | $V_{SATA\_OOB}$ | 50 | 120 | 240 | mV p-p | — |

**Note:**
1. Voltage relative to common of either signal comprising a differential pair

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

**Table 81. Gen2i/3 G Receiver (Rx) Input DC Specifications ($XV_{DD}$ = 1.5 V or 1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential input voltage | $V_{SATA\_RXDIFF}$ | 275 | — | 750 | mV p-p | 1 |
| Differential Rx input impedance | $Z_{SATA\_RXSEIM}$ | 85 | 100 | 115 | Ω | 2 |
| OOB signal detection threshold | $V_{SATA\_OOB}$ | 75 | 120 | 240 | mV p-p | 2 |

**Note:**
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

### 2.20.7.2 SATA AC Timing Specifications

This section discusses the SATA AC timing specifications.

#### 2.20.7.2.1 AC Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in this table to be guaranteed by the customer's application design.

**Table 82. SATA Reference Clock Input Requirements**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range | $t_{CLK\_REF}$ | — | 100/125 | — | MHz | 1 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance | $t_{CLK\_TOL}$ | –350 | — | +350 | ppm | — |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V) | $t_{CLK\_DUTY}$ | 40 | 50 | 60 | % | — |

### 3.1.4 e500mc Core Complex PLL Select

The clock frequency of each the e500mc core 0–3 complex is determined by the binary value of the RCW field CC*n*_PLL_SEL. These tables describe the supported ratios for each core complex 0–3, where each individual core complex can select a frequency from the table.

**Table 96. e500mc Core Complex [0,1] PLL Select**

| Binary Value of C*n*_PLL_SEL for n=[0,1] | e500mc:Core Cluster Ratio |
|---|---|
| 0000 | CC1 PLL /1 |
| 0001 | CC1 PLL /2 |
| 0100 | CC2 PLL /1 |
| All Others | Reserved |

**Table 97. e500mc Core Complex [2,3] PLL Select**

| Binary Value of C*n*_PLL_SEL for n=[0,1] | e500mc:Core Cluster Ratio |
|---|---|
| 0000 | CC1 PLL /1 |
| 0100 | CC2 PLL /1 |
| 0101 | CC2 PLL /2 |
| All Others | Reserved |

### 3.1.5 DDR Controller PLL Ratios

The single DDR memory controller complexes can be asynchronous to the platform, depending on configuration.

Table 98 describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in this table. This ratio is determined by the binary value of the RCW configuration field MEM_PLL_RAT[10:14].

The RCW configuration field MEM_PLL_CFG[8:9] must be set to MEM_PLL_CFG[8:9] = 0b01 if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in Table 98 for asynchronous DDR clock ratios; otherwise, set MEM_PLL_CFG[8:9] = 0b00.

**NOTE**

The RCW Configuration field DDR_SYNC (bit 184) must be set to 0b0 for asynchronous mode.

The RCW Configuration field DDR_RATE (bit 232) must be set to b’0 for asynchronous mode

The RCW Configuration field DDR_RSV0 (bit 234) must be set to b’0 for all ratios.

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

### 3.8.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 61).

The system board designer can choose among several types of commercially-available thermal interface materials.

### 3.8.3 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

- Operating range: 10 – 230µA
- Ideality factor over 13.5 – 220 µA: n = 1.00589 ± 0.008

# 4 Package Information

The following section describes the detailed content and mechanical description of the package.

## 4.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm × 23 mm, 780 flip chip plastic ball grid array (FC-PBGA).

| | |
|---|---|
| Package outline | 23 mm × 23mm |
| Interconnects | 780 |
| Ball Pitch | 0.8 mm |
| Ball Diameter (typical) | 0.40 mm |
| Solder Balls | 96.5% Sn, 3% Ag, 0.5% Cu |
| Module height (typical) | 2.21 mm to 2.51 mm (Maximum) |

# 5 Security Fuse Processor

The device implements the QorIQ platform's Trust Architecture supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

In order to program SFP fuses, the user is required to supply 1.5 V to the $POV_{DD}$ pin per Section 2.2, "Power Up Sequencing." $POV_{DD}$ should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times $POV_{DD}$ must be connected to GND. The sequencing requirements for raising and lowering $POV_{DD}$ are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect $POV_{DD}$ to GND.

# 6 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

## 6.1 Part Numbering Nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature. Not all possible combinations of part numbers implied by the part numbering scheme are supported. For a list of available part numbers, contact your Freescale Sales office. Each part number also contains a revision code which refers to the die mask revision number.

**Table 107. Part Numbering Nomenclature**

| *p* | *n* | *nn* | *n* | *x* | *t* | *e* | *n* | *c* | *d* | *r* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Generation** | **Platform** | **Number of Cores** | **Derivative** | **Qual Status** | **Temp. Range** | **Encryption** | **Package Type** | **CPU Freq** | **DDR Data Rate** | **Die Revision** |
| P = 45 nm | 1–5 | 01 = 1 core<br>02 = 2 cores<br>04 = 4 cores | 0–9 | P = Prototype<br>N = Industrial qualification | S = Std temp<br>X = Extended temp (–40 to 105C) | E = SEC present<br>N = SEC not present | 1 = FC-PBGA Pb-free spheres<br>7 = FC-PBGA C4 and sphere Pb-free | F = 667 MHz<br>H = 800 MHz<br>K = 1000 MHz<br>M = 1200 MHz | L = 1067 MT/s<br>M = 1200 MT/s | A = Rev 1.0<br>B = Rev 1.1<br>C = Rev 2.0 |

## 6.2 Orderable Part Numbers Addressed by this Document

This table provides the Freescale orderable part numbers addressed by this document for the chip.

| Part Number | *p* | *n* | *nn* | *n* | *x* | *t* | *e* | *n* | *c* | *d* | *r* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P2040NSE1FLB<br>P2040NSE7FLC | P | 2 | 04 = 4 core | 1 | N = Industrial qualification | S = Std temp | E = SEC present | 1= FC-PBGA Pb-free spheres<br>7 = FC-PBGA C4 and sphere Pb-free | F = 667 MHz | L = 1067 MT/s | B<br>C |
| P2040NSN1FLB<br>P2040NSN7FLC | | | | | | | N = SEC not present | | | | |
| P2040NSE1HLB<br>P2040NSE7HLC | | | | | | | E = SEC present | | H = 800 MHz | | |
| P2040NSN1HLB<br>P2040NSN7HLC | | | | | | | N = SEC not present | | | | |
| P2040NSE1KLB<br>P2040NSE7KLC | | | | | | | E = SEC Present | | K = 1000 MHz | | |
| P2040NSN1KLB<br>P2040NSN7KLC | | | | | | | N = SEC not present | | | | |
| P2040NSE1MMB<br>P2040NSE7MMC | | | | | | | E = SEC Present | | M = 1200 MHz | M = 1200 MT/s | |
| P2040NSN1MMB<br>P2040NSN7MMC | | | | | | | N = SEC not present | | | | |
| P2040NXE1FLB<br>P2040NXE7FLC | | | | | | X = Extended temp | E = SEC Present | | F = 667 MHz | L = 1067 MT/s | |
| P2040NXN1FLB<br>P2040NXN7FLC | | | | | | | N = SEC not present | | | | |
| P2040NXE1MMB<br>P2040NXE7MMC | | | | | | | E = SEC Present | | M = 1200 MHz | M = 1200 MT/s | |
| P2040NXN1MMB<br>P2040NXN7MMC | | | | | | | N = SEC not present | | | | |