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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2040nsn7klc

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
DMA					
DMA1_DREQ0/IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/GPIO18	DMA1 Channel 0 Request	AC23	I	OV_{DD}	24
DMA1_DACK0/IIC3_SCL/GPIO16/SDHC_CD/ M1DVAL/LB_DVAL	DMA1 Channel 0 Acknowledge	AB23	O	OV_{DD}	2, 14
DMA1_DDONE0/IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0/SDHC_WP	DMA1 Channel 0 Done	AB26	O	OV_{DD}	2, 14
DMA2_DREQ0/IRQ03/GPIO21	DMA2 Channel 0 Request	AA26	I	OV_{DD}	24
DMA2_DACK0/IRQ04/GPIO22	DMA2 Channel 0 Acknowledge	V25	O	OV_{DD}	24
DMA2_DDONE0/IRQ05/GPIO23	DMA2 Channel 0 Done	AA22	O	OV_{DD}	24
USB Host Port 1					
USB1_UDP	USB1 PHY Data Plus	K28	I/O	$USB\_V_{DD}\_3P3$	—
USB1_UDM	USB1 PHY Data Minus	L28	I/O	$USB\_V_{DD}\_3P3$	—
USB1_VBUS_CLMP	USB1 PHY VBUS Divided Signals	M25	I	$USB\_V_{DD}\_3P3$	34
USB1_UID	USB1 PHY ID Detect	M27	I	$USB\_V_{DD}\_3P3$	—
USB_CLKIN	USB PHY Clock Input	P22	I	OV_{DD}	—
USB1_DRVVBUS/GPIO24/IRQ6	USB1 5V Supply Enable	Y26	O	OV_{DD}	—
USB1_PWRFAULT/GPIO25/IRQ7	USB Power Fault	AA23	I	OV_{DD}	—
USB Host Port 2					
USB2_UDP	USB2 PHY Data Plus	K26	I/O	$USB\_V_{DD}\_3P3$	—
USB2_UDM	USB2 PHY Data Minus	L26	I/O	$USB\_V_{DD}\_3P3$	—
USB2_VBUS_CLMP	USB2 PHY VBUS Divided Signals	J25	I	$USB\_V_{DD}\_3P3$	34
USB2_UID	USB2 PHY ID Detect	J27	I	$USB\_V_{DD}\_3P3$	—
USB2_DRVVBUS/GPIO26/IRQ8	USB2 5V Supply Enable	AC22	I/O	OV_{DD}	—
USB2_PWRFAULT/GPIO27/IRQ9	USB2 Power Fault	AC27	I/O	OV_{DD}	—
Programmable Interrupt Controller					
IRQ00	External Interrupts	Y25	I	OV_{DD}	—
IRQ01	External Interrupts	AB27	I	OV_{DD}	—
IRQ02	External Interrupts	AB25	I	OV_{DD}	—
IRQ03/GPIO21/DMA2_DREQ0	External Interrupts	AA26	I	OV_{DD}	24
IRQ04/GPIO22/DMA2_DACK0	External Interrupts	V25	I	OV_{DD}	24

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IEEE 1588					
TSEC_1588_CLK_IN/EC1_RXD2	Clock In	B27	I	LV_{DD}	—
TSEC_1588_TRIG_IN1/EC1_RXD0	Trigger In 1	B28	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RXD1	Trigger In 2	A27	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1/EC1_TXD0	Alarm Out 1	B24	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/ EC1_TXD1/GPIO30	Alarm Out 2	C25	O	LV_{DD}	23
TSEC_1588_CLK_OUT/EC1_RXD3	Clock Out	B26	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1/EC1_TXD2	Pulse Out1	C28	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_TXD3/GPIO31	Pulse Out2	A26	O	LV_{DD}	23
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	F23	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	G24	I/O	LV_{DD}	—
Ethernet Reference Clock					
EC1_GTX_CLK125/EC_XTRNL_TX_STMP2	Reference Clock (RGMII)	A24	I	LV_{DD}	25
EC2_GTX_CLK125	Reference Clock (RGMII)	D24	I	LV_{DD}	25
Ethernet External Timestamping					
EC_XTRNL_TX_STMP1/EC1_TX_EN	External Timestamp Transmit 1	C27	I	LV_{DD}	—
EC_XTRNL_RX_STMP1/EC1_RX_DV	External Timestamp Receive 1	A25	I	LV_{DD}	—
EC_XTRNL_TX_STMP2/EC1_GTX_CLK125	External Timestamp Transmit 2	A24	I	LV_{DD}	—
EC_XTRNL_RX_STMP2/EC1_RX_CLK	External Timestamp Receive 2	C24	I	LV_{DD}	—
Three-Speed Ethernet Controller 1					
EC1_TXD3/TSEC_1588_PULSE_OUT2/GPIO31	Transmit Data	A26	O	LV_{DD}	—
EC1_TXD2/TSEC_1588_PULSE_OUT1	Transmit Data	C28	O	LV_{DD}	—
EC1_TXD1/TSEC_1588_ALARM_OUT2/GPIO30	Transmit Data	C25	O	LV_{DD}	—
EC1_TXD0/TSEC_1588_ALARM_OUT1	Transmit Data	B24	O	LV_{DD}	—
EC1_TX_EN/EC_XTRNL_TX_STMP1	Transmit Enable	C27	O	LV_{DD}	15
EC1_GTX_CLK	Transmit Clock Out (RGMII)	D26	O	LV_{DD}	24
EC1_RXD3/TSEC_1588_CLK_OUT	Receive Data	B26	I	LV_{DD}	25
EC1_RXD2/TSEC_1588_CLK_IN	Receive Data	B27	I	LV_{DD}	25

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD_CA_PL	Core Group A and Platform Vdd Sense	H8	—	—	8
SENSEVDD_CB	Core Group B Vdd Sense	AB16	—	—	8
USB1_VDD_3P3	USB1 PHY Transceiver 3.3 V Supply	M23	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3 V Supply	J23	—	—	—
USB1_VDD_1P0	USB1 PHY PLL 1.0 V Supply	L22	—	—	—
USB2_VDD_1P0	USB2 PHY PLL 1.0 V Supply	K22	—	—	—
Analog Signals					
MVREF	SSTL_1.5/1.35 Reference Voltage	W7	I	$GV_{DD}/2$	—
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	E21	I	200Ω (±1%) to XV_{DD}	21
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	F7	I	200Ω (±1%) to SV_{DD}	22
TEMP_ANODE	Temperature Diode Anode	V5	—	internal diode	9
TEMP_CATHODE	Temperature Diode Cathode	U6	—	internal diode	9
USB2_IBIAS_REXT	USB PHY2 Reference Bias Current Generation	K23	—	GND	32
USB1_IBIAS_REXT	USB PHY1 Reference Bias Current Generation	L23	—	GND	32
USB2_VDD_1P8_DECAP	USB2 PHY 1.8 V Output to External Decap	K24	—	GND	33
USB1_VDD_1P8_DECAP	USB1 PHY 1.8 V Output to External Decap	L24	—	GND	33
No Connection Pins					
NC03	No Connection	W4	—	—	11
NC04	No Connection	W3	—	—	11
NC05	No Connection	W1	—	—	11
NC06	No Connection	H7	—	—	11
NC07	No Connection	G7	—	—	11
NC08	No Connection	F20	—	—	11
NC09	No Connection	F19	—	—	11
NC10	No Connection	F18	—	—	11
NC11	No Connection	F16	—	—	11
NC12	No Connection	F13	—	—	11

2.1.3 Output Driver Characteristics

This table provides information about the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	(Nominal) Supply Voltage	Note
Local Bus interface utilities signals	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR3 signal	20 (full-strength mode) 40 (half-strength mode)	GV_{DD} = 1.5 V	1
DDR3L signal	20 (full-strength mode) 40 (half-strength mode)	GV_{DD} = 1.35 V	1
eTSEC/10/100 signals	45 45	LV_{DD} = 3.3 V LV_{DD} = 2.5 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—
eSPI, eSDHC	45 45 45	CV_{DD} = 3.3 V CV_{DD} = 2.5 V CV_{DD} =1.8 V	—

Note:

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at T_j = 105 °C and at GV_{DD} (min).

2.2 Power Up Sequencing

The device requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. Bring up OV_{DD}, LV_{DD}, BV_{DD}, CV_{DD}, and USB_V_{DD}_3P3. Drive POV_{DD} = GND.
   - — $\overline{\text{PORESET}}$ input must be driven asserted and held during this step.
   - — IO_VSEL inputs must be driven during this step and held stable during normal operation.
   - — USB_V_{DD}_3P3 rise time (10% to 90%) has a minimum of 350 µs.
2. Bring up $V_{DD\_CA\_CB\_PL}$, SV_{DD}, AV_{DD} (cores, platform, SerDes) and USB_V_{DD}_1P0. $V_{DD\_CA\_CB\_PL}$ and USB_V_{DD}_1P0 must be ramped up simultaneously.
3. Bring up GV_{DD} (DDR) and XV_{DD}.
4. Negate $\overline{\text{PORESET}}$ input as long as the required assertion/hold time has been met per Table 17.
5. For secure boot fuse programming: After negation of $\overline{\text{PORESET}}$, drive POV_{DD} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD} = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5. See Section 5, "Security Fuse Processor," for additional details.

WARNING

Only two secure boot fuse programming events are permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND.

2.6.3 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the e500mc; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 16× the period of the platform clock. That is, minimum clock high time is 8× (platform clock), and minimum clock low time is 8× (platform clock). There is no minimum RTC frequency; RTC may be grounded if not needed.

2.6.4 dTSEC Gigabit Ethernet Reference Clock Timing

This table provides the dTSEC gigabit reference clocks DC electrical characteristics.

Table 15. EC_GTX_CLK125 DC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.

This table provides the dTSEC gigabit reference clocks AC timing specifications.

Table 16. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Note:
1. Rise and fall times for EC_GTX_CLK125 are measured from 20% to 80% (rise time) and 80% to 20% (fall time) of LV_{DD}.
2. EC_GTX_CLK125 is used to generate the GTX clock for the dTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the dTSEC GTX_CLK. See Section 2.12.2.2, "RGMII AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.6.5 Other Input Clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information on the input clock requirements of functional blocks sourced external of the device, such as SerDes, Ethernet Management, eSDHC, Local Bus, see the specific interface section.

2.14 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 46. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 47. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

Table 49. Enhanced Local Bus Timing Specifications (continued)

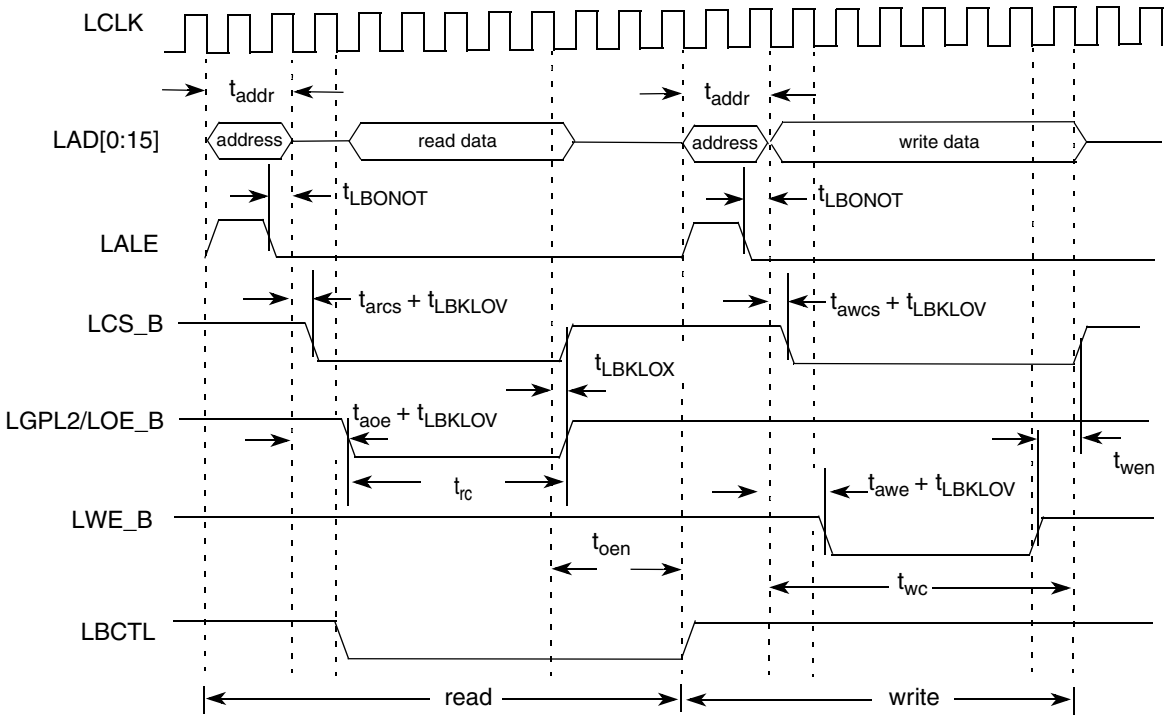
For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	2.0	ns	—
Output hold (Except LALE)	t_{LBKLOX}	-3.5	—	ns	5
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	2 platform clock cycles - 1ns (LBCR[AHD] = 1)	—	ns	4
		4 platform clock cycles - 2 ns (LBCR[AHD] = 0)	—		

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew is measured between different LCLKs at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. After power on reset, LBCR[AHD] defaults to 0.
5. Output hold is negative, meaning that the output transition happens earlier than the falling edge of LCLK.

This figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the chip reference manual.

Figure 22. GPCM Output Timing Diagram

2.15 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.15.1 eSDHC DC Electrical Characteristics

This table provides the eSDHC electrical characteristics.

Table 50. eSDHC Interface DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	$0.625 \times CV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	—	$0.25 \times CV_{DD}$	V	1
Input/output leakage current	I_{IN}/I_{OZ}	—	–50	50	μA	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at CV_{DD} min	$0.75 \times CV_{DD}$	—	V	—

Table 57. I²C AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 2 above is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

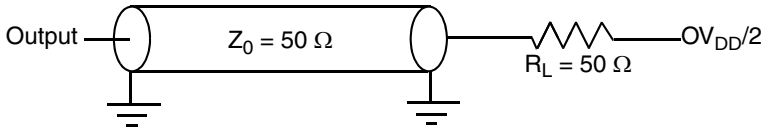


Figure 29. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

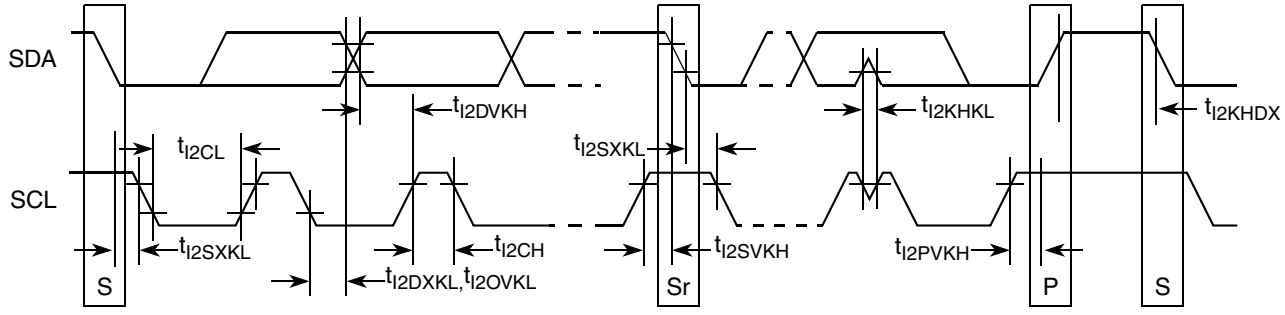


Figure 30. I²C Bus AC Timing Diagram

2.20.2.3 AC Requirements for SerDes Reference Clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO, SATA and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 61. SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ Input Clock Requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125/156.25	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-Fall Matching	—	—	20	%	5, 6

Note:

1. **Caution:** Only 100, 125 and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.

Table 62. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 63. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	—	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.4.4 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

2.20.6.1.3 Aurora Receiver DC Electrical Characteristics

This table provides the Aurora receiver DC electrical characteristics (XVDD = 1.5 V or 1.8 V).

Table 75. Aurora Receiver DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:
1. Measured at receiver

2.20.6.2 Aurora AC Timing Specifications

This section describes the AC timing specifications for Aurora.

2.20.6.2.1 Aurora AC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 2(SD_REF_CLK2 and $\overline{\text{SD\_REF\_CLK2}}$) may be used for SerDes Aurora configurations based on the RCW configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 1.

2.20.6.2.2 Aurora Transmitter AC Timing Specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 76. Aurora Transmitter AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

2.20.6.2.3 Aurora Receiver AC Timing Specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 77. Aurora Receiver AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—

Table 87. SGMII DC Transmitter Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output differential voltage[2, 3, 4] (XV_{DD-Typ} at 1.5 V and 1.8 V)	$\|V_{OD}\|$	320	500.0	725.0	mV	B(1-2)TECR(lane)0[AMP_RED] =0b000000
		293.8	459.0	665.6		B(1-2)TECR(lane)0[AMP_RED] =0b000010
		266.9	417.0	604.7		B(1-2)TECR(lane)0[AMP_RED] =0b000101
		240.6	376.0	545.2		B(1-2)TECR(lane)0[AMP_RED] =0b001000
		213.1	333.0	482.9		B(1-2)TECR(lane)0[AMP_RED] =0b001100
		186.9	292.0	423.4		B(1-2)TECR(lane)0[AMP_RED] =0b001111
		160.0	250.0	362.5		B(1-2)TECR(lane)0[AMP_RED] =0b010011
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Note:

1. This does not align to DC-coupled SGMII.
2. V_{OD}| = |V_{SD_TXn} – $V_{\overline{SD\_TXn}}$|. |V_{OD}| is also referred to as output differential peak voltage. $V_{TX-DIFFp-p}$ = 2*|V_{OD}|.
3. Example amplitude reduction setting for SGMII on SerDes bank 1 lane E: B1TECRE0[AMP_RED] = 0b000010 for an output differential voltage of 459 mV typical.
4. The |V_{OD}| value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.5 V or 1.8 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD_TX*n* and $\overline{\text{SD\_TX}n}$.

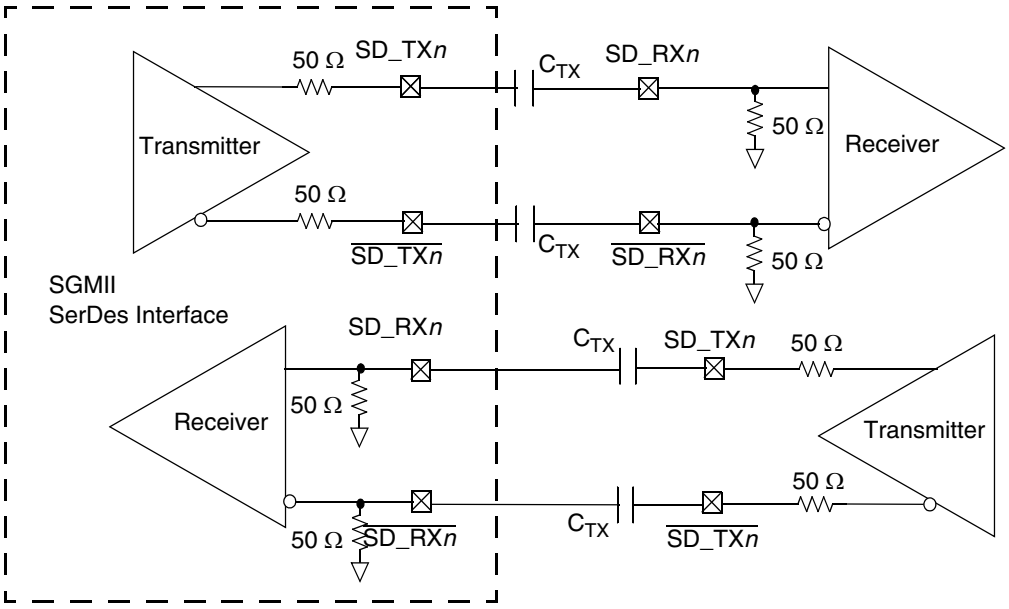


Figure 44. 4-Wire AC-Coupled SGMII Serial Link Connection Example

See Section 19.4 “LP-Serial Signal Descriptions,” in the chip reference manual for Serial RapidIO interface width and frequency details.

3.1.7 SerDes PLL Ratio

The clock ratio between each of the three SerDes PLLs and their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs is determined by the binary value of the RCW Configuration field SRDS_RATIO_B*n* as shown in this table. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW field SRDS_DIV_B*n* as shown in Table 103.

This table lists the supported SerDes PLL Bank *n* to SD_REF_CLK*n* ratios.

Table 101. SerDes PLL Bank *n* to SD_REF_CLK*n* Ratios

Binary Value of SRDS_RATIO_B1	SRDS_PLL_*n*:SD_REF_CLK*n* Ratio	
	***n* = 1 (Bank)**	***n* = 2 (Bank 2)**
000	Reserved	Reserved
001	Reserved	20:1
010	25:1	25:1
011	40:1	40:1
100	50:1	50:1
101	Reserved	24:1
110	Reserved	30:1
All Others	Reserved	Reserved

These tables list the supported SerDes PLL dividers.

This table shows the PLL divider support for each pair of lanes on SerDes Bank 1.

Table 102. SerDes Bank 1 PLL Dividers

Binary Value of SRDS_DIV_B1[0:4]	SerDes Bank 1 PLL Divider
0b0	Divide by 1 off Bank 1 PLL
0b1	Divide by 2 off Bank 1 PLL

Note: 1 bit (of 5 total SRDS_DIV_B1 bits) controls each pair of lanes.

This table shows the PLL dividers supported for each 4-lane for SerDes Banks 2.

Table 103. SerDes Banks 2 PLL Dividers

Binary Value of SRDS_DIV_B2	SerDes Bank *2* PLL Divider
0b0	Divide by 1 off Bank *2* PLL
0b1	Divide by 2 off Bank *2* PLL

Note: 1 bit controls all four lanes of bank 2.

3.1.8 Frame Manager (FMan) Clock Select

The Frame Managers (FM) can each be synchronous to the platform.

Table 105. I/O Voltage Selection

Signals	Value (Binary)	VDD Voltage Selection		
		BVDD	CVDD	LVDD
IO_VSEL[0:4] Default (0_0000)	0_0000	3.3 V	3.3 V	3.3 V
	0_0001			2.5 V
	0_0010			Reserved
	0_0011	3.3 V	2.5 V	3.3 V
	0_0100			2.5 V
	0_0101			Reserved
	0_0110	3.3 V	1.8 V	3.3 V
	0_0111			2.5 V
	0_1000			Reserved
	0_1001	2.5 V	3.3 V	3.3 V
	0_1010			2.5 V
	0_1011			Reserved
	0_1100	2.5 V	2.5 V	3.3 V
	0_1101			2.5 V
	0_1110			Reserved
	0_1111	2.5 V	1.8 V	3.3 V
	1_0000			2.5 V
	1_0001			Reserved
	1_0010	1.8 V	3.3 V	3.3 V
	1_0011			2.5 V
	1_0100			Reserved
	1_0101	1.8 V	2.5 V	3.3 V
	1_0110			2.5 V
	1_0111			Reserved
	1_1000	1.8 V	1.8 V	3.3 V
	1_1001			2.5 V
	1_1010			Reserved
	1_1011	3.3 V	3.3 V	3.3 V
	1_1100			
	1_1101			
	1_1110			
	1_1111			

3.3 Power Supply Design

This section discusses the power supply design.

3.3.1 PLL Power Supply Filtering

Each of the PLLs described in Section 3.1, "System Clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, AV_{DD_CCn} and AV_{DD_DDR} voltages must be derived directly from the $V_{DD\_CA\_CB\_PL}$ source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 50, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 50 shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%

C1 = 10µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH

C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD}.

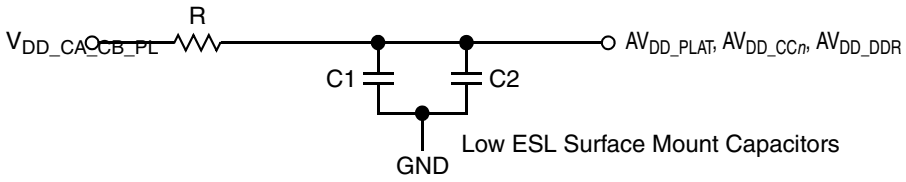
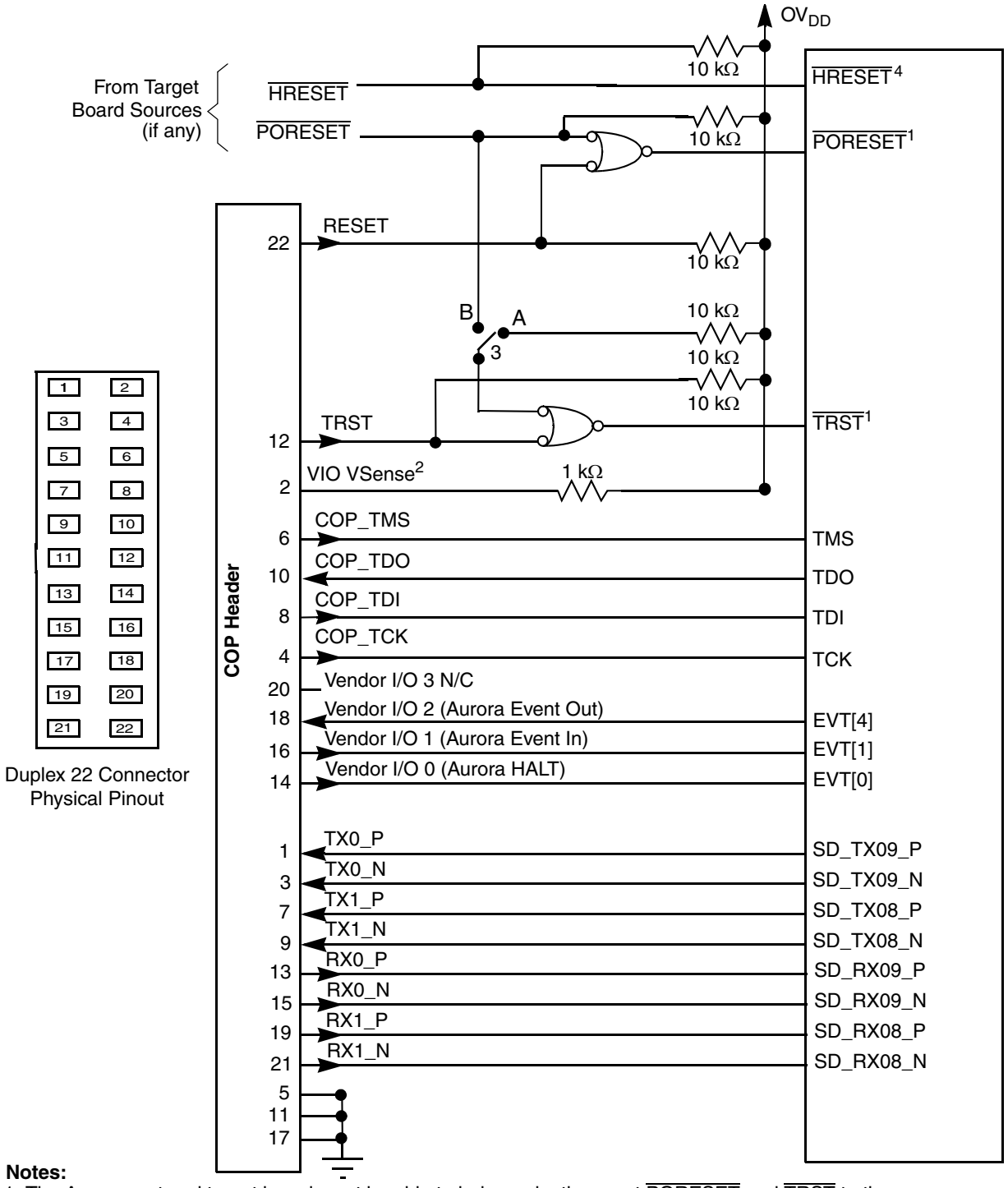


Figure 50. PLL Power Supply Filter Circuit

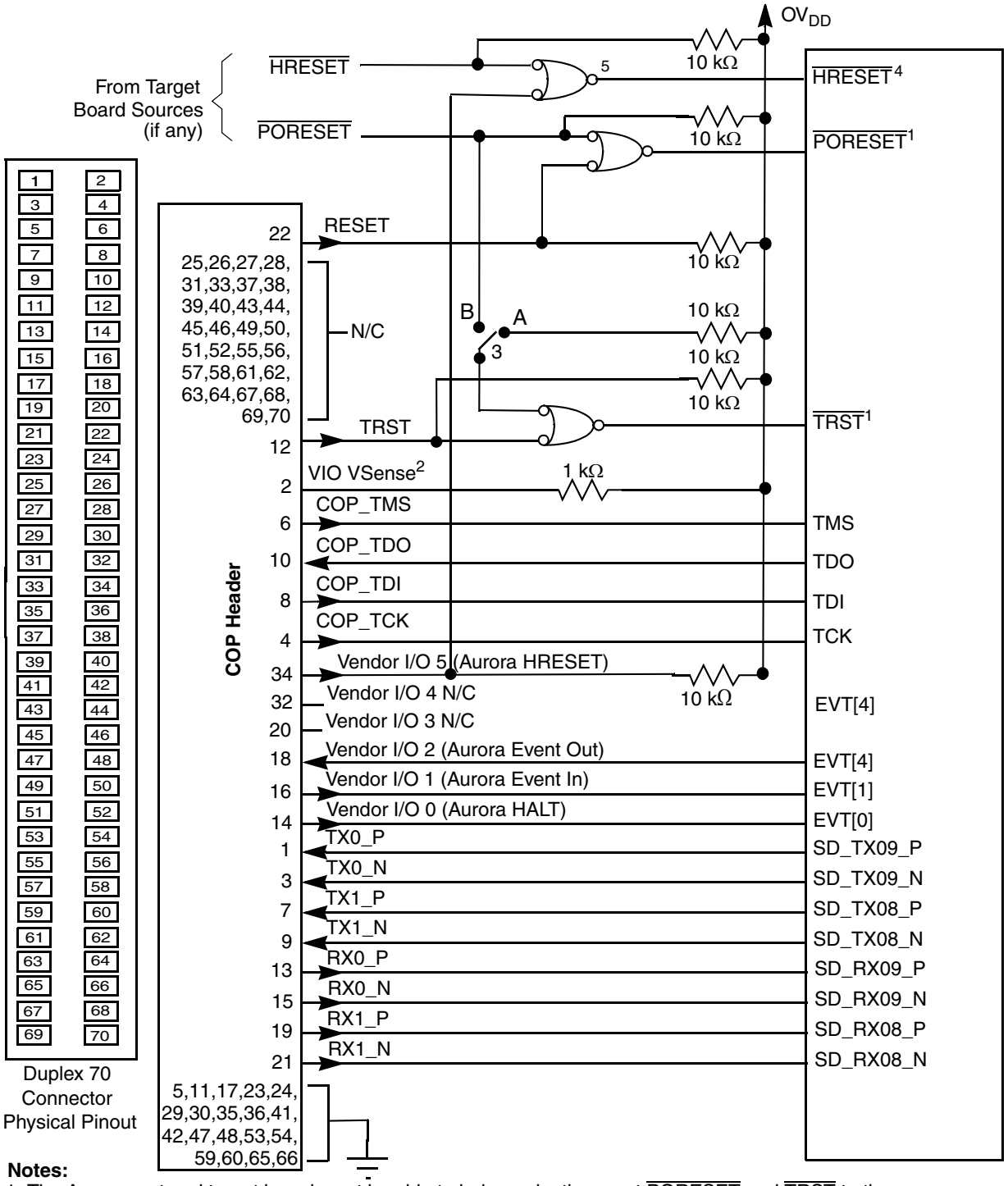
The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 51. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn}



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device. $\overline{\text{HRESET}}$ is not used by the Aurora 22 pin connector.

Figure 58. Aurora 22 Pin Connector Duplex Interface Connection



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.
5. This is an open-drain gate.

Figure 59. Aurora 70 Pin Connector Duplex Interface Connection

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.8.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 61).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.8.3 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

- Operating range: 10 – 230µA
- Ideality factor over 13.5 – 220 µA: n = 1.00589 ± 0.008

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm × 23 mm, 780 flip chip plastic ball grid array (FC-PBGA).

Package outline	23 mm × 23mm
Interconnects	780
Ball Pitch	0.8 mm
Ball Diameter (typical)	0.40 mm
Solder Balls	96.5% Sn, 3% Ag, 0.5% Cu
Module height (typical)	2.21 mm to 2.51 mm (Maximum)

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02/2013