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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Security; SEC 4.2
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator, Secure Fusebox
Package / Case	-
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2040nxe1flb

1.1 780 FC-PBGA Ball Layout Diagrams

These figures show the FC-PBGA ball map diagrams.

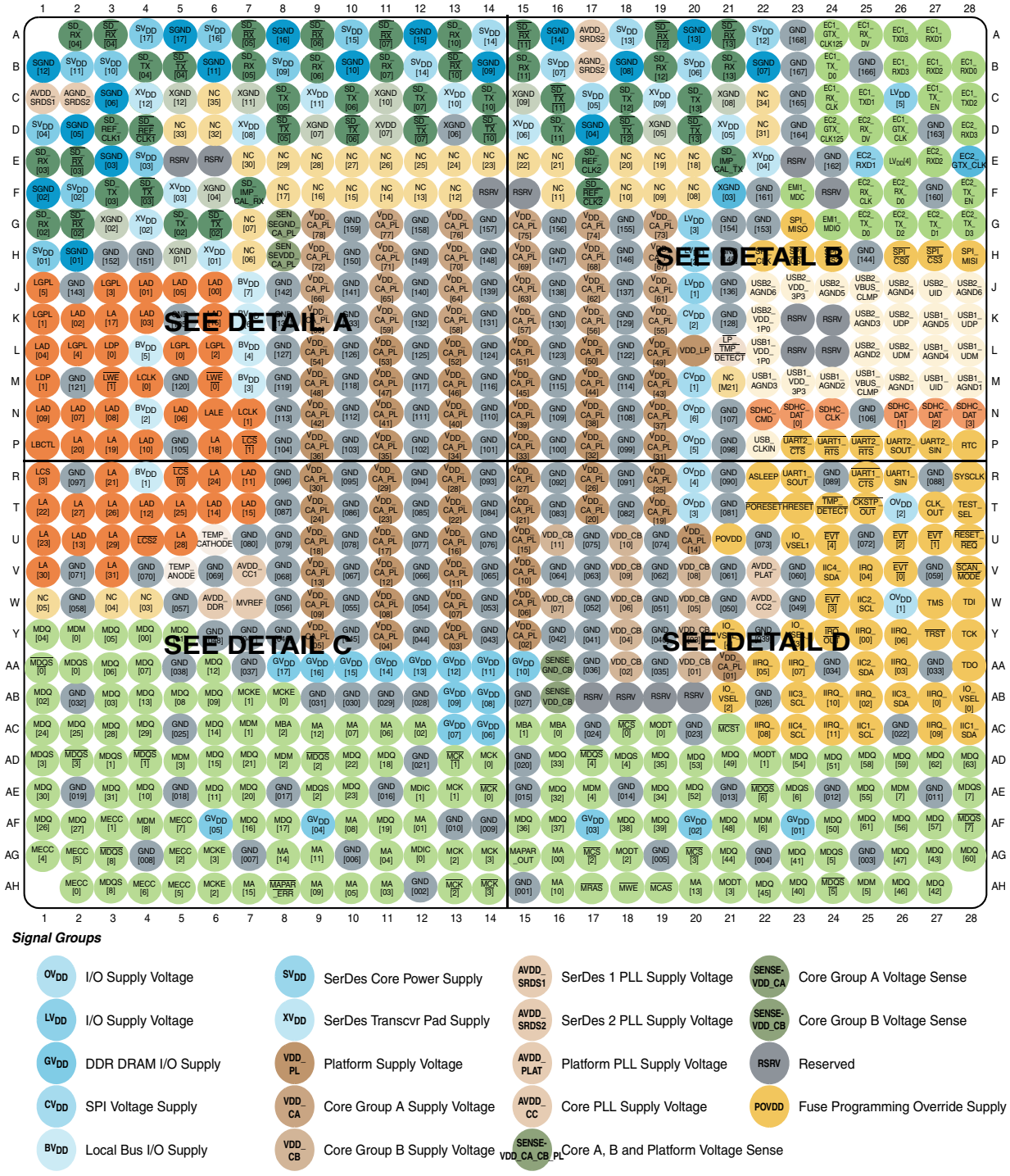


Figure 2. 780 BGA Ball Map Diagram (Top View)

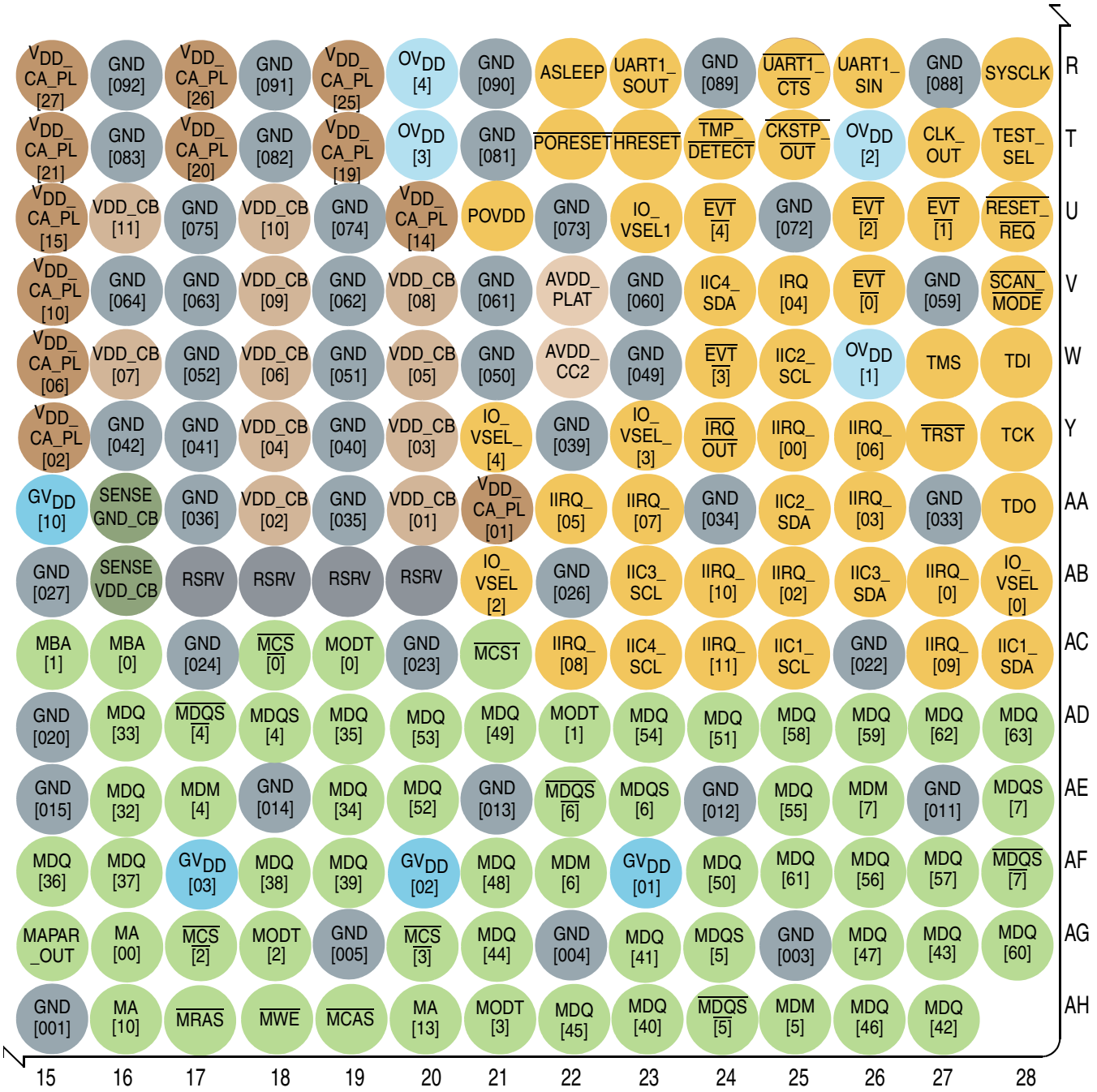


Figure 6. 780 BGA Ball Map Diagram (Detail View D)

1.2 Pinout List

This table provides the pinout listing for the 780 FC-PBGA package by bus. Pins for multiplexed signals appear in the bus group for their default status and have a corresponding note stating that they have multiple functionality depending on the mode in which they are configured.

Table 1. Pin List by Bus

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
DDR SDRAM Memory Interface					
MDQ00	Data	Y4	I/O	GV_{DD}	—
MDQ01	Data	Y5	I/O	GV_{DD}	—
MDQ02	Data	AB1	I/O	GV_{DD}	—
MDQ03	Data	AB3	I/O	GV_{DD}	—
MDQ04	Data	Y1	I/O	GV_{DD}	—
MDQ05	Data	Y3	I/O	GV_{DD}	—
MDQ06	Data	AA3	I/O	GV_{DD}	—
MDQ07	Data	AA4	I/O	GV_{DD}	—
MDQ08	Data	AB5	I/O	GV_{DD}	—
MDQ09	Data	AB6	I/O	GV_{DD}	—
MDQ10	Data	AE4	I/O	GV_{DD}	—
MDQ11	Data	AE6	I/O	GV_{DD}	—
MDQ12	Data	AA6	I/O	GV_{DD}	—
MDQ13	Data	AB4	I/O	GV_{DD}	—
MDQ14	Data	AC6	I/O	GV_{DD}	—
MDQ15	Data	AD6	I/O	GV_{DD}	—
MDQ16	Data	AF7	I/O	GV_{DD}	—
MDQ17	Data	AF8	I/O	GV_{DD}	—
MDQ18	Data	AD11	I/O	GV_{DD}	—
MDQ19	Data	AF11	I/O	GV_{DD}	—
MDQ20	Data	AE7	I/O	GV_{DD}	—
MDQ21	Data	AD7	I/O	GV_{DD}	—
MDQ22	Data	AD10	I/O	GV_{DD}	—
MDQ23	Data	AE10	I/O	GV_{DD}	—
MDQ24	Data	AC1	I/O	GV_{DD}	—
MDQ25	Data	AC2	I/O	GV_{DD}	—
MDQ26	Data	AF1	I/O	GV_{DD}	—
MDQ27	Data	AF2	I/O	GV_{DD}	—
MDQ28	Data	AC3	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ63	Data	AD28	I/O	GV_{DD}	—
MECC0	Error Correcting Code	AH2	I/O	GV_{DD}	—
MECC1	Error Correcting Code	AF3	I/O	GV_{DD}	—
MECC2	Error Correcting Code	AG5	I/O	GV_{DD}	—
MECC3	Error Correcting Code	AH5	I/O	GV_{DD}	—
MECC4	Error Correcting Code	AG1	I/O	GV_{DD}	—
MECC5	Error Correcting Code	AG2	I/O	GV_{DD}	—
MECC6	Error Correcting Code	AH4	I/O	GV_{DD}	—
MECC7	Error Correcting Code	AF5	I/O	GV_{DD}	—
$\overline{\text{MAPAR\_ERR}}$	Address Parity Error	AH8	I	GV_{DD}	4
MAPAR_OUT	Address Parity Out	AG15	O	GV_{DD}	—
MDM0	Data Mask	Y2	O	GV_{DD}	—
MDM1	Data Mask	AC7	O	GV_{DD}	—
MDM2	Data Mask	AD8	O	GV_{DD}	—
MDM3	Data Mask	AD5	O	GV_{DD}	—
MDM4	Data Mask	AE17	O	GV_{DD}	—
MDM5	Data Mask	AH25	O	GV_{DD}	—
MDM6	Data Mask	AF22	O	GV_{DD}	—
MDM7	Data Mask	AE26	O	GV_{DD}	—
MDM8	Data Mask	AF4	O	GV_{DD}	—
MDQS0	Data Strobe	AA2	I/O	GV_{DD}	—
MDQS1	Data Strobe	AD3	I/O	GV_{DD}	—
MDQS2	Data Strobe	AE9	I/O	GV_{DD}	—
MDQS3	Data Strobe	AD1	I/O	GV_{DD}	—
MDQS4	Data Strobe	AD18	I/O	GV_{DD}	—
MDQS5	Data Strobe	AG24	I/O	GV_{DD}	—
MDQS6	Data Strobe	AE23	I/O	GV_{DD}	—
MDQS7	Data Strobe	AE28	I/O	GV_{DD}	—
MDQS8	Data Strobe	AH3	I/O	GV_{DD}	—
$\overline{\text{MDQS0}}$	Data Strobe	AA1	I/O	GV_{DD}	—
$\overline{\text{MDQS1}}$	Data Strobe	AD4	I/O	GV_{DD}	—
$\overline{\text{MDQS2}}$	Data Strobe	AD9	I/O	GV_{DD}	—
$\overline{\text{MDQS3}}$	Data Strobe	AD2	I/O	GV_{DD}	—
$\overline{\text{MDQS4}}$	Data Strobe	AD17	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LVDD05	Ethernet Controller 1 and 2 Supply	C26	—	LV_{DD}	—
LVDD04	Ethernet Controller 1 and 2 Supply	E26	—	LV_{DD}	—
LVDD03	Ethernet Controller 1 and 2 Supply	G20	—	LV_{DD}	—
LVDD02	Ethernet Controller 1 and 2 Supply	H20	—	LV_{DD}	—
LVDD01	Ethernet Controller 1 and 2 Supply	J20	—	LV_{DD}	—
POVDD	Fuse Programming Override Supply	U21	—	POV_{DD}	30
VDD_CA_PL78	Core Group A and Platform Supply	G9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL77	Core Group A and Platform Supply	G11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL76	Core Group A and Platform Supply	G13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL75	Core Group A and Platform Supply	G15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL74	Core Group A and Platform Supply	G17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL73	Core Group A and Platform Supply	G19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL72	Core Group A and Platform Supply	H9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL71	Core Group A and Platform Supply	H11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL70	Core Group A and Platform Supply	H13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL69	Core Group A and Platform Supply	H15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL68	Core Group A and Platform Supply	H17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL67	Core Group A and Platform Supply	H19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL66	Core Group A and Platform Supply	J9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL65	Core Group A and Platform Supply	J11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL64	Core Group A and Platform Supply	J13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL63	Core Group A and Platform Supply	J15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL62	Core Group A and Platform Supply	J17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL61	Core Group A and Platform Supply	J19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL60	Core Group A and Platform Supply	K9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL59	Core Group A and Platform Supply	K11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL58	Core Group A and Platform Supply	K13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL57	Core Group A and Platform Supply	K15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL56	Core Group A and Platform Supply	K17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL55	Core Group A and Platform Supply	K19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL54	Core Group A and Platform Supply	L9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL53	Core Group A and Platform Supply	L11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL52	Core Group A and Platform Supply	L13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL51	Core Group A and Platform Supply	L15	—	$V_{DD\_CA\_PL}$	37

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_CA_PL50	Core Group A and Platform Supply	L17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL49	Core Group A and Platform Supply	L19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL48	Core Group A and Platform Supply	M9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL47	Core Group A and Platform Supply	M11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL46	Core Group A and Platform Supply	M13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL45	Core Group A and Platform Supply	M15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL44	Core Group A and Platform Supply	M17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL43	Core Group A and Platform Supply	M19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL42	Core Group A and Platform Supply	N9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL41	Core Group A and Platform Supply	N11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL40	Core Group A and Platform Supply	N13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL39	Core Group A and Platform Supply	N15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL38	Core Group A and Platform Supply	N17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL37	Core Group A and Platform Supply	N19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL36	Core Group A and Platform Supply	P9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL35	Core Group A and Platform Supply	P11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL34	Core Group A and Platform Supply	P13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL33	Core Group A and Platform Supply	P15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL32	Core Group A and Platform Supply	P17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL31	Core Group A and Platform Supply	P19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL30	Core Group A and Platform Supply	R9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL29	Core Group A and Platform Supply	R11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL28	Core Group A and Platform Supply	R13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL27	Core Group A and Platform Supply	R15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL26	Core Group A and Platform Supply	R17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL25	Core Group A and Platform Supply	R19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL24	Core Group A and Platform Supply	T9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL23	Core Group A and Platform Supply	T11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL22	Core Group A and Platform Supply	T13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL21	Core Group A and Platform Supply	T15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL20	Core Group A and Platform Supply	T17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL19	Core Group A and Platform Supply	T19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL18	Core Group A and Platform Supply	U9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL17	Core Group A and Platform Supply	U11	—	$V_{DD\_CA\_PL}$	37

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
Reserve	—	AB20	—	GND	19

Note:

1. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD} in order to ensure no random chip select assertion due to possible noise, etc.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the corresponding power and ground nets internally. They may be connected as a differential pair to be used by the voltage regulators with remote sense function. For Rev1.1 silicon, the better solution is to use the far sense pins relative to the power supply location, the other pair can be left as no connected. The DC power simulation should be done during the board layout process to approve the selected solution.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
10. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
11. Do not connect.
12. These are test signals for factory use only and must be pulled low (1 KΩ–2 kΩ) to ground (GND) for normal machine operation.
13. Independent supplies derived from board $V_{DD\_CA\_CB\_PL}$ (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD} if I^2C interface is used.
15. This pin requires an external 1 KΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
17. These pins must be pulled up to 1.2 V through a 180 $\Omega \pm 1\%$ resistor for EM2_MDC and a 330 $\Omega \pm 1\%$ resistor for EM2_MDIO.
18. Pin has a weak internal pull-up.
19. These pins must be pulled to ground (GND).
20. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
21. This pin requires a 200-Ω pull-up to XV_{DD}.
22. This pin requires a 200-Ω pull-up to SV_{DD}.
23. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
24. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
25. See Section 3.6, "Connection Recommendations," for additional details on this signal.

Table 7. P2040 I/O Power Supply Estimated Values (continued)

IEEE 1588	—	LVdd (2.5V)	0.004	0.005	W	1,3,6
eLBC	32-bit, 100Mhz	BVdd (1.8V)	0.048	0.120	W	1,3,6
		BVdd (2.5V)	0.072	0.193		
		BVdd (3.3V)	0.120	0.277		
	16-bit, 100Mhz	BVdd (1.8V)	0.021	0.030	W	1,3,6
		BVdd (2.5V)	0.036	0.046		
		BVdd (3.3V)	0.057	0.076		
eSDHC	—	Ovdd (3.3V)	0.014	0.150	W	1,3,6
eSPI	—	CVdd (1.8V)	0.004	0.005	W	1,3,6
		CVdd (2.5V)	0.006	0.008		
		CVdd (3.3V)	0.010	0.013		
USB	—	USB_Vdd_3P3	0.012	0.015	W	1,3,6
I2C	—	OVdd (3.3V)	0.002	0.003	W	1,3,6
DUART	—	OVdd (3.3V)	0.006	0.008	W	1,3,6
GPIO	x8	OVdd (1.8V)	0.005	0.006	W	1,3,4,6
		OVdd (2.5V)	0.007	0.009		
		OVdd (3.3V)	0.009	0.011		
Others (Reset, System Clock, JTAG & Misc)	—	OVdd (3.3V)	0.003	0.015	W	1,3,4,6

Note:

1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load.
4. GPIO's are supported on 1.8 V, 2.5 V and 3.3 V rails as specified in the hardware specification.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guranteed current.
7. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configuration combination possible for the device. To get the XVDD power numbers, the user should add the combined lanes to match to the total SerDes lanes used, not simply multiply the power numbers by the number of lanes.

Table 13. SYSCLK AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	67	—	133	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	±150	ps	—
SYSCLK jitter phase noise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD} \div 2$.
3. Slew rate as measured from ± 0.3 $\Delta \mathbf{V_{AC}}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.6.2 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the device input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the device is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread Spectrum Clock Source Recommendations

For recommended operating conditions, see Table 3.

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

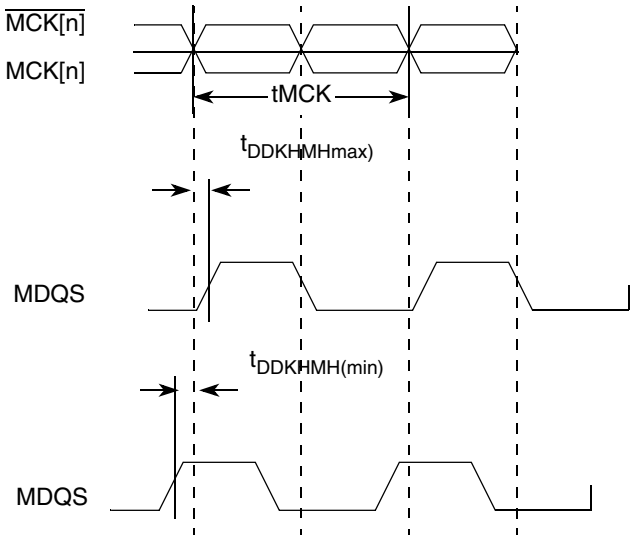


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

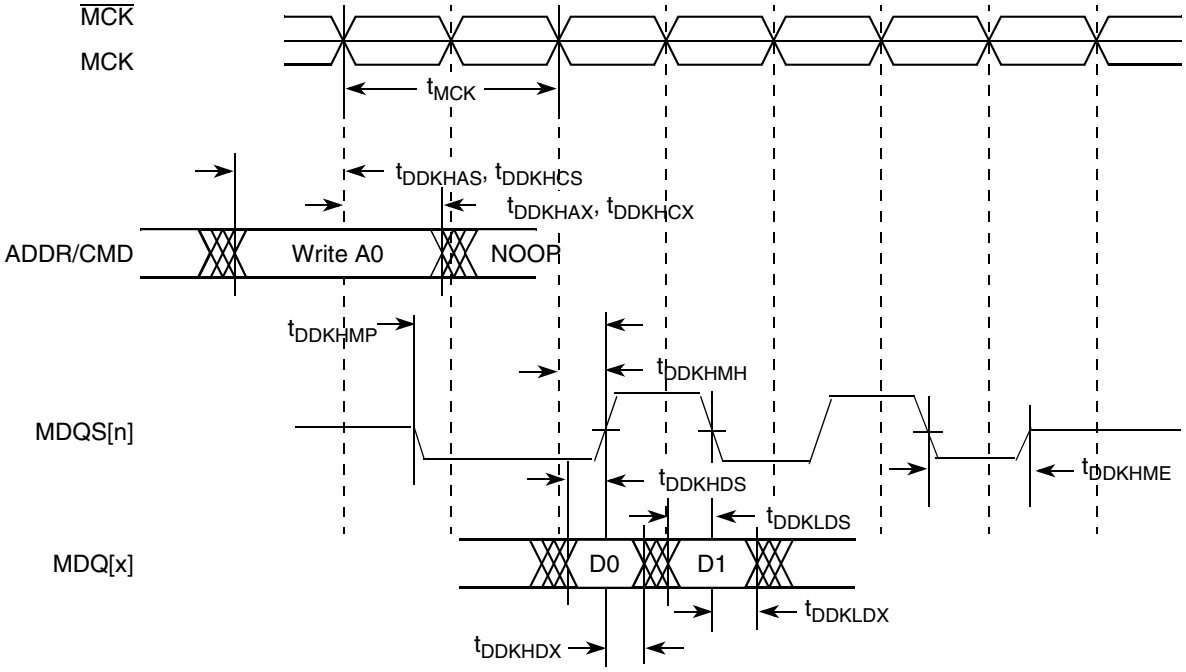


Figure 11. DDR3 and DDR3L Output Timing Diagram

Table 43. eTSEC IEEE 1588 AC Timing Specifications (continued)

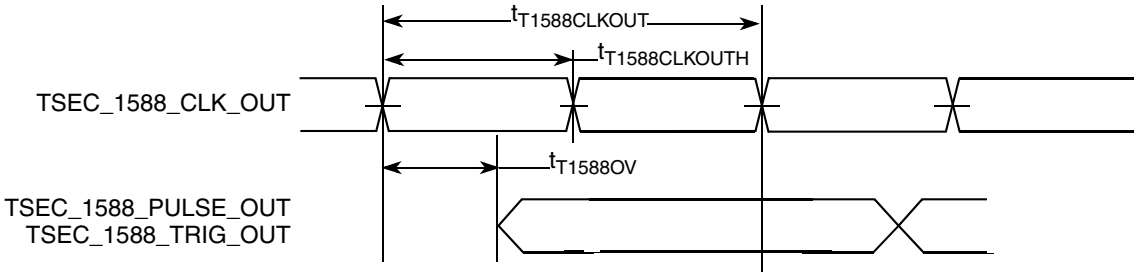
For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

Figure 18. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

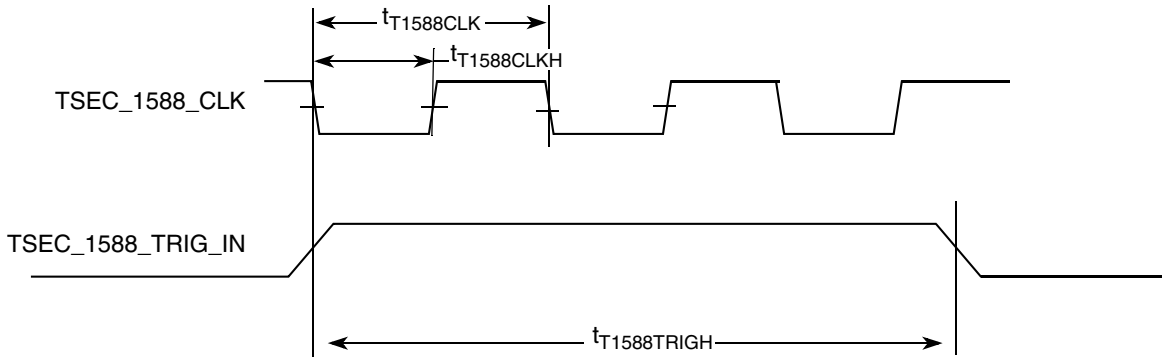
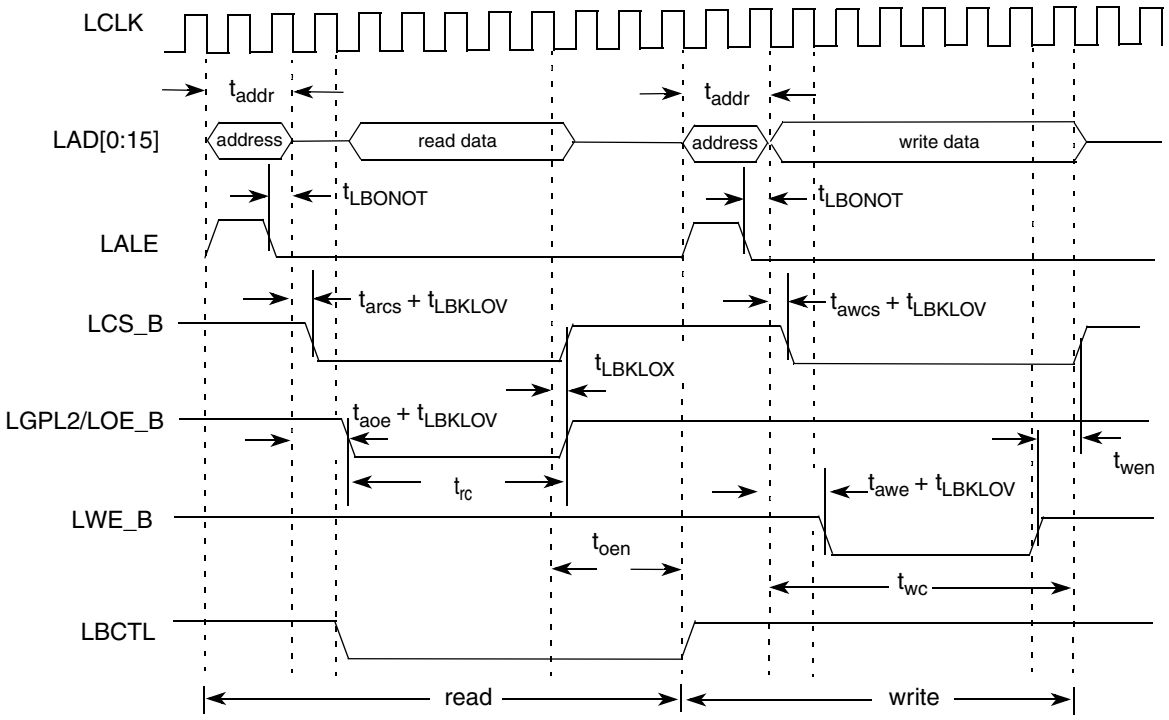


Figure 19. eTSEC IEEE 1588 Input AC Timing

This figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the chip reference manual.

Figure 22. GPCM Output Timing Diagram

2.15 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.15.1 eSDHC DC Electrical Characteristics

This table provides the eSDHC electrical characteristics.

Table 50. eSDHC Interface DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	$0.625 \times CV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	—	$0.25 \times CV_{DD}$	V	1
Input/output leakage current	I_{IN}/I_{OZ}	—	–50	50	μA	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at CV_{DD} min	$0.75 \times CV_{DD}$	—	V	—

This figure provides the JTAG clock input timing diagram.

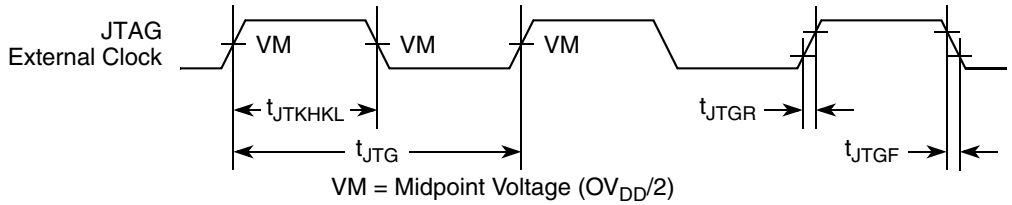


Figure 26. JTAG Clock Input Timing Diagram

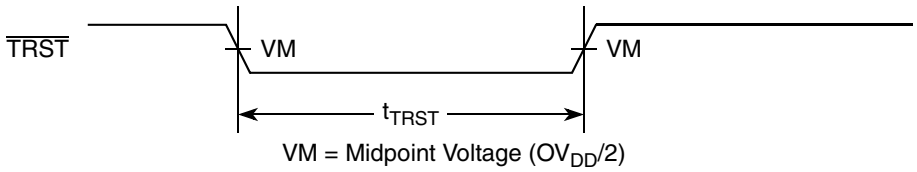


Figure 27. $\overline{\text{TRST}}$ Timing Diagram

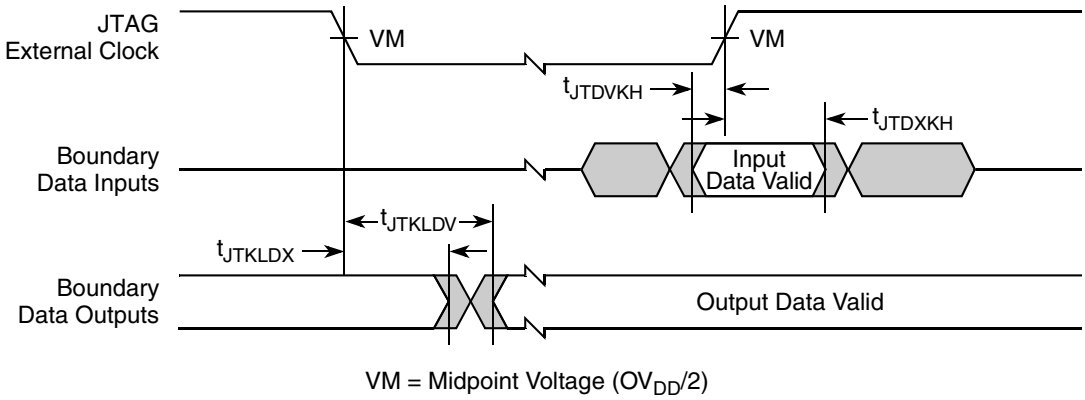


Figure 28. Boundary-Scan Timing Diagram

2.18 I²C

This section describes the DC and AC electrical characteristics for the I^2C interface.

2.18.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 56. I^2C DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2

2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V.

Table 58. GPIO DC Electrical Characteristics (CV_{DD}, LV_{DD} or OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max L/OV_{IN} respective values found in Table 3.
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} or LV_{DD} = 2.5 V.

Table 59. GPIO DC Electrical Characteristics (CV_{DD} or LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- Section 2.20.4, “PCI Express”
- Section 2.20.5, “Serial RapidIO (sRIO)”
- Section 2.20.6, “Aurora”
- Section 2.20.7, “Serial ATA (SATA)
- Section 2.20.8, “SGMII Interface”

2.20.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

2.20.4.1 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

2.20.4.2 PCI Express Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

SerDes banks 1–2 (SD_REF_CLK[1:2] and $\overline{\text{SD\_REF\_CLK}[1:2]}$) may be used for various SerDes PCI Express configurations based on the RCW configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, “SerDes Reference Clocks.”

2.20.4.3 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.3.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 62. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	—	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Tx DC differential mode low Impedance

Table 65. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = $2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Note:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.20.4.5 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.5.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Table 77. Aurora Receiver AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps	—

Note:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

2.20.7 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

2.20.7.1 SATA DC Electrical Characteristics

This section describes the DC electrical characteristics for SATA.

2.20.7.1.1 SATA DC Transmitter Output Characteristics

This table provides the DC differential transmitter output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 78. Gen1i/1.5G Transmitter (Tx) DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	—	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Note:
1. Terminated by 50 Ω load.
2. DC impedance

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 79. Gen 2i/3G Transmitter (Tx) DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Tx diff output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 2i/3G Receiver (Rx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:
1. Measured at receiver.

2.20.8 SGMII Interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the device, as shown in Figure 44, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 39.

2.20.8.0.1 SGMII Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK[1:2] and $\overline{\text{SD\_REF\_CLK}[1:2]}$ pins. SerDes banks 1–2 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, “SerDes Reference Clocks.”

2.20.8.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.1.1 SGMII Transmit DC Timing Specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) as shown in Figure 45.

Table 87. SGMII DC Transmitter Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1

3.1.2 Platform to SYSCLK PLL Ratio

This table shows the allowed platform clock-to-SYSCLK ratios.

The chip platform clock frequency is always below 666 MHz frequencies; set the RCW configuration field SYS_PLL_CFG = 0b01.

Table 94. Platform to SYSCLK PLL Ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0100	4:1
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
0_1001	9:1
All Others	Reserved

3.1.3 e500mc Core Cluster to SYSCLK PLL Ratio

The clock ratio between SYSCLK and each of the two core cluster PLLs is determined at power up by the binary value of the RCW field CCn_PLL_RAT. This table describes the supported ratios. Note that a core cluster PLL frequency targeting 1 GHz and above must set RCW field CCn_PLL_CFG = 0b00 for frequency targeting below 1 GHz set CCn_PLL_CFG = 0b01.

This table lists the supported Core Cluster to SYSCLK ratios.

Table 95. e500mc Core Cluster PLL to SYSCLK Ratios

Binary Value of CCn_PLL_RAT	Core Cluster:SYSCLK Ratio
0_1000	8:1
0_1001	9:1
0_1010	10:1
0_1011	11:1
0_1100	12:1
0_1101	13:1
0_1110	14:1
0_1111	15:1
1_0000	16:1
1_0001	17:1
1_0010	18:1
All Others	Reserved

isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, or TDO.

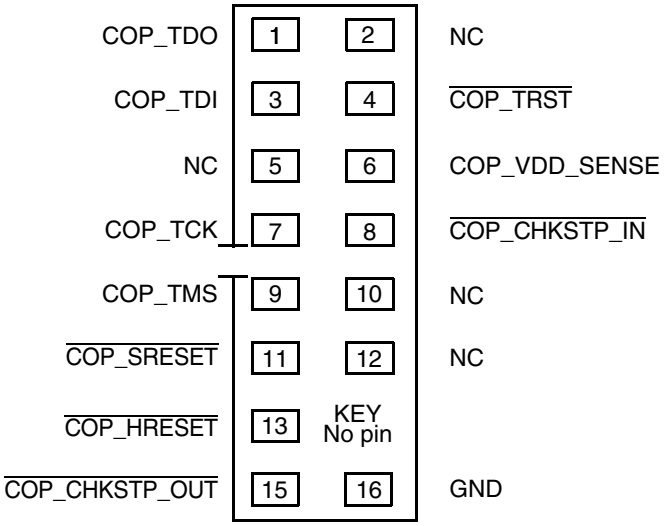


Figure 54. Legacy COP Connector Physical Pinout