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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Security; SEC 4.2
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator, Secure Fusebox
Package / Case	-
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2040nxe1mmb

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MCK0	Clock	AD14	O	GV_{DD}	—
MCK1	Clock	AE13	O	GV_{DD}	—
MCK2	Clock	AG13	O	GV_{DD}	—
MCK3	Clock	AG14	O	GV_{DD}	—
$\overline{\text{MCK0}}$	Clock Complements	AE14	O	GV_{DD}	—
$\overline{\text{MCK1}}$	Clock Complements	AD13	O	GV_{DD}	—
$\overline{\text{MCK2}}$	Clock Complements	AH13	O	GV_{DD}	—
$\overline{\text{MCK3}}$	Clock Complements	AH14	O	GV_{DD}	—
MODT0	On Die Termination	AC19	O	GV_{DD}	—
MODT1	On Die Termination	AD22	O	GV_{DD}	—
MODT2	On Die Termination	AG18	O	GV_{DD}	—
MODT3	On Die Termination	AH21	O	GV_{DD}	—
MDIC0	Driver Impedance Calibration	AG12	I/O	GV_{DD}	16
MDIC1	Driver Impedance Calibration	AE12	I/O	GV_{DD}	16
Local Bus Controller Interface					
LAD00	Muxed Data/Address	J6	I/O	BV_{DD}	3
LAD01	Muxed Data/Address	J4	I/O	BV_{DD}	3
LAD02	Muxed Data/Address	K2	I/O	BV_{DD}	3
LAD03	Muxed Data/Address	K4	I/O	BV_{DD}	3
LAD04	Muxed Data/Address	L1	I/O	BV_{DD}	3
LAD05	Muxed Data/Address	J5	I/O	BV_{DD}	3
LAD06	Muxed Data/Address	N5	I/O	BV_{DD}	3
LAD07	Muxed Data/Address	N2	I/O	BV_{DD}	3
LAD08	Muxed Data/Address	N3	I/O	BV_{DD}	3
LAD09	Muxed Data/Address	N1	I/O	BV_{DD}	3
LAD10	Muxed Data/Address	P4	I/O	BV_{DD}	3
LAD11	Muxed Data/Address	R7	I/O	BV_{DD}	3
LAD12	Muxed Data/Address	T4	I/O	BV_{DD}	3
LAD13	Muxed Data/Address	U2	I/O	BV_{DD}	3
LAD14	Muxed Data/Address	T6	I/O	BV_{DD}	3
LAD15	Muxed Data/Address	T7	I/O	BV_{DD}	3
LA16	Address	K6	I/O	BV_{DD}	31
LA17	Address	K3	I/O	BV_{DD}	31
LA18	Address	P6	I/O	BV_{DD}	31

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
DMA					
DMA1_DREQ0/IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/GPIO18	DMA1 Channel 0 Request	AC23	I	OV_{DD}	24
DMA1_DACK0/IIC3_SCL/GPIO16/SDHC_CD/ M1DVAL/LB_DVAL	DMA1 Channel 0 Acknowledge	AB23	O	OV_{DD}	2, 14
DMA1_DDONE0/IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0/SDHC_WP	DMA1 Channel 0 Done	AB26	O	OV_{DD}	2, 14
DMA2_DREQ0/IRQ03/GPIO21	DMA2 Channel 0 Request	AA26	I	OV_{DD}	24
DMA2_DACK0/IRQ04/GPIO22	DMA2 Channel 0 Acknowledge	V25	O	OV_{DD}	24
DMA2_DDONE0/IRQ05/GPIO23	DMA2 Channel 0 Done	AA22	O	OV_{DD}	24
USB Host Port 1					
USB1_UDP	USB1 PHY Data Plus	K28	I/O	$USB\_V_{DD}\_3P3$	—
USB1_UDM	USB1 PHY Data Minus	L28	I/O	$USB\_V_{DD}\_3P3$	—
USB1_VBUS_CLMP	USB1 PHY VBUS Divided Signals	M25	I	$USB\_V_{DD}\_3P3$	34
USB1_UID	USB1 PHY ID Detect	M27	I	$USB\_V_{DD}\_3P3$	—
USB_CLKIN	USB PHY Clock Input	P22	I	OV_{DD}	—
USB1_DRVVBUS/GPIO24/IRQ6	USB1 5V Supply Enable	Y26	O	OV_{DD}	—
USB1_PWRFAULT/GPIO25/IRQ7	USB Power Fault	AA23	I	OV_{DD}	—
USB Host Port 2					
USB2_UDP	USB2 PHY Data Plus	K26	I/O	$USB\_V_{DD}\_3P3$	—
USB2_UDM	USB2 PHY Data Minus	L26	I/O	$USB\_V_{DD}\_3P3$	—
USB2_VBUS_CLMP	USB2 PHY VBUS Divided Signals	J25	I	$USB\_V_{DD}\_3P3$	34
USB2_UID	USB2 PHY ID Detect	J27	I	$USB\_V_{DD}\_3P3$	—
USB2_DRVVBUS/GPIO26/IRQ8	USB2 5V Supply Enable	AC22	I/O	OV_{DD}	—
USB2_PWRFAULT/GPIO27/IRQ9	USB2 Power Fault	AC27	I/O	OV_{DD}	—
Programmable Interrupt Controller					
IRQ00	External Interrupts	Y25	I	OV_{DD}	—
IRQ01	External Interrupts	AB27	I	OV_{DD}	—
IRQ02	External Interrupts	AB25	I	OV_{DD}	—
IRQ03/GPIO21/DMA2_DREQ0	External Interrupts	AA26	I	OV_{DD}	24
IRQ04/GPIO22/DMA2_DACK0	External Interrupts	V25	I	OV_{DD}	24

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IEEE 1588					
TSEC_1588_CLK_IN/EC1_RXD2	Clock In	B27	I	LV_{DD}	—
TSEC_1588_TRIG_IN1/EC1_RXD0	Trigger In 1	B28	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RXD1	Trigger In 2	A27	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1/EC1_TXD0	Alarm Out 1	B24	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/ EC1_TXD1/GPIO30	Alarm Out 2	C25	O	LV_{DD}	23
TSEC_1588_CLK_OUT/EC1_RXD3	Clock Out	B26	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1/EC1_TXD2	Pulse Out1	C28	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_TXD3/GPIO31	Pulse Out2	A26	O	LV_{DD}	23
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	F23	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	G24	I/O	LV_{DD}	—
Ethernet Reference Clock					
EC1_GTX_CLK125/EC_XTRNL_TX_STMP2	Reference Clock (RGMII)	A24	I	LV_{DD}	25
EC2_GTX_CLK125	Reference Clock (RGMII)	D24	I	LV_{DD}	25
Ethernet External Timestamping					
EC_XTRNL_TX_STMP1/EC1_TX_EN	External Timestamp Transmit 1	C27	I	LV_{DD}	—
EC_XTRNL_RX_STMP1/EC1_RX_DV	External Timestamp Receive 1	A25	I	LV_{DD}	—
EC_XTRNL_TX_STMP2/EC1_GTX_CLK125	External Timestamp Transmit 2	A24	I	LV_{DD}	—
EC_XTRNL_RX_STMP2/EC1_RX_CLK	External Timestamp Receive 2	C24	I	LV_{DD}	—
Three-Speed Ethernet Controller 1					
EC1_TXD3/TSEC_1588_PULSE_OUT2/GPIO31	Transmit Data	A26	O	LV_{DD}	—
EC1_TXD2/TSEC_1588_PULSE_OUT1	Transmit Data	C28	O	LV_{DD}	—
EC1_TXD1/TSEC_1588_ALARM_OUT2/GPIO30	Transmit Data	C25	O	LV_{DD}	—
EC1_TXD0/TSEC_1588_ALARM_OUT1	Transmit Data	B24	O	LV_{DD}	—
EC1_TX_EN/EC_XTRNL_TX_STMP1	Transmit Enable	C27	O	LV_{DD}	15
EC1_GTX_CLK	Transmit Clock Out (RGMII)	D26	O	LV_{DD}	24
EC1_RXD3/TSEC_1588_CLK_OUT	Receive Data	B26	I	LV_{DD}	25
EC1_RXD2/TSEC_1588_CLK_IN	Receive Data	B27	I	LV_{DD}	25

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
Reserve	—	AB20	—	GND	19

Note:

1. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD} in order to ensure no random chip select assertion due to possible noise, etc.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the corresponding power and ground nets internally. They may be connected as a differential pair to be used by the voltage regulators with remote sense function. For Rev1.1 silicon, the better solution is to use the far sense pins relative to the power supply location, the other pair can be left as no connected. The DC power simulation should be done during the board layout process to approve the selected solution.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
10. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
11. Do not connect.
12. These are test signals for factory use only and must be pulled low (1 KΩ–2 kΩ) to ground (GND) for normal machine operation.
13. Independent supplies derived from board $V_{DD\_CA\_CB\_PL}$ (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD} if I^2C interface is used.
15. This pin requires an external 1 KΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
17. These pins must be pulled up to 1.2 V through a 180 $\Omega \pm 1\%$ resistor for EM2_MDC and a 330 $\Omega \pm 1\%$ resistor for EM2_MDIO.
18. Pin has a weak internal pull-up.
19. These pins must be pulled to ground (GND).
20. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
21. This pin requires a 200-Ω pull-up to XV_{DD}.
22. This pin requires a 200-Ω pull-up to SV_{DD}.
23. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
24. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
25. See Section 3.6, "Connection Recommendations," for additional details on this signal.

Table 6. Device Power Dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	667	534	1067	467	1.0	65	8.7	—	8.2	—	—	2, 3
Thermal						105	12.0	—	11.8	—	—	5, 7
Maximum							12.3	11.1	11.9	10.6	1.4	4, 6, 7

Note:

1. Combined power of $V_{DD\_CA\_CB\_PL}$, SVDD with the DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P2040 I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.705	1.764	W	1,2,5,6
	800 MT/s data rate		0.714	1.785		
	1066 MT/s data rate		0.731	1.827		
	1200 MT/s data rate		0.739	1.848		
	1333 MT/s data rate		0.747	1.869		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1, 7
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC Per Controller	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6

Table 7. P2040 I/O Power Supply Estimated Values (continued)

IEEE 1588	—	LVdd (2.5V)	0.004	0.005	W	1,3,6
eLBC	32-bit, 100Mhz	BVdd (1.8V)	0.048	0.120	W	1,3,6
		BVdd (2.5V)	0.072	0.193		
		BVdd (3.3V)	0.120	0.277		
	16-bit, 100Mhz	BVdd (1.8V)	0.021	0.030	W	1,3,6
		BVdd (2.5V)	0.036	0.046		
		BVdd (3.3V)	0.057	0.076		
eSDHC	—	Ovdd (3.3V)	0.014	0.150	W	1,3,6
eSPI	—	CVdd (1.8V)	0.004	0.005	W	1,3,6
		CVdd (2.5V)	0.006	0.008		
		CVdd (3.3V)	0.010	0.013		
USB	—	USB_Vdd_3P3	0.012	0.015	W	1,3,6
I2C	—	OVdd (3.3V)	0.002	0.003	W	1,3,6
DUART	—	OVdd (3.3V)	0.006	0.008	W	1,3,6
GPIO	x8	OVdd (1.8V)	0.005	0.006	W	1,3,4,6
		OVdd (2.5V)	0.007	0.009		
		OVdd (3.3V)	0.009	0.011		
Others (Reset, System Clock, JTAG & Misc)	—	OVdd (3.3V)	0.003	0.015	W	1,3,4,6

Note:

1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load.
4. GPIO's are supported on 1.8 V, 2.5 V and 3.3 V rails as specified in the hardware specification.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guranteed current.
7. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configuration combination possible for the device. To get the XVDD power numbers, the user should add the combined lanes to match to the total SerDes lanes used, not simply multiply the power numbers by the number of lanes.

2.7 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 17. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit[1]	Note
Required assertion time of $\overline{\text{PORESET}}$	1	—	ms	3
Required input assertion time of $\overline{\text{HRESET}}$	32	—	SYSCLKs	1, 2
Input setup time for POR configs with respect to negation of $\overline{\text{PORESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Note:
1. SYSCLK is the primary clock input for the device.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1, “Power-On Reset Sequence,” in the chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. Refer to Section 2.2, “Power Up Sequencing.”

Table 18. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

2.8 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 19. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (For example exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.9.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	1, 2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed the $MV_{REF}n$ DC level by more than ±1% of the DC value (that is, ±15mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $MV_{REF}n$ with a min value of $MV_{REF}n$ – 0.04 and a max value of $MV_{REF}n$ + 0.04. V_{TT} should track variations in the DC level of $MV_{REF}n$.
4. The voltage regulator for $MV_{REF}n$ must meet the specifications stated in Table 23.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.35 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	1, 2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.090	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.8	mA	7, 8
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.8	—	mA	7, 8

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

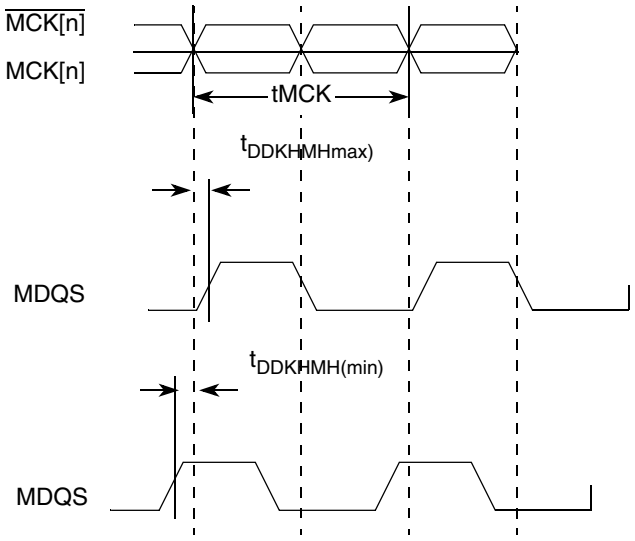


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

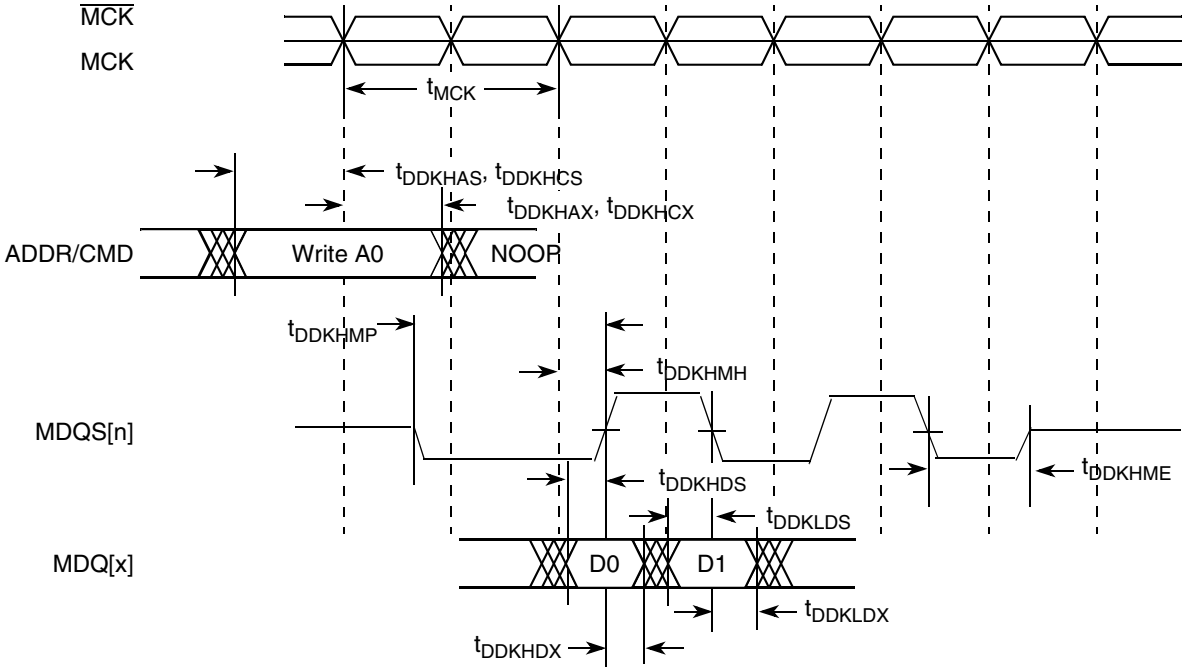


Figure 11. DDR3 and DDR3L Output Timing Diagram

2.10 eSPI

This section describes the DC and AC electrical specifications for the eSPI interface.

2.10.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 3.3 V.

Table 30. eSPI DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 2.5 V.

Table 31. eSPI DC Electrical Characteristics (CV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 32. eSPI DC Electrical Characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1

Table 38. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

The Ethernet management interface is defined to operate at a supply voltage of 2.5 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 39. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

2.12.3.2 Ethernet Management Interface AC Timing Specifications

This table provides the Ethernet management interface AC timing specifications.

Table 40. Ethernet Management Interface AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 6$	—	$(16 \times t_{plb\_clk}) + 6$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 1.8 V.

Table 48. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.14.2 Enhanced Local Bus AC Timing Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

This figure shows the eLBC AC test load.

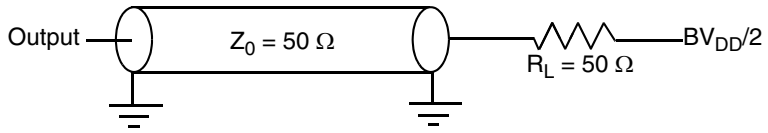


Figure 20. Enhanced Local Bus AC Test Load

2.14.2.1 Local Bus AC Timing Specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table provides the eLBC timing specifications.

Table 49. Enhanced Local Bus Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—

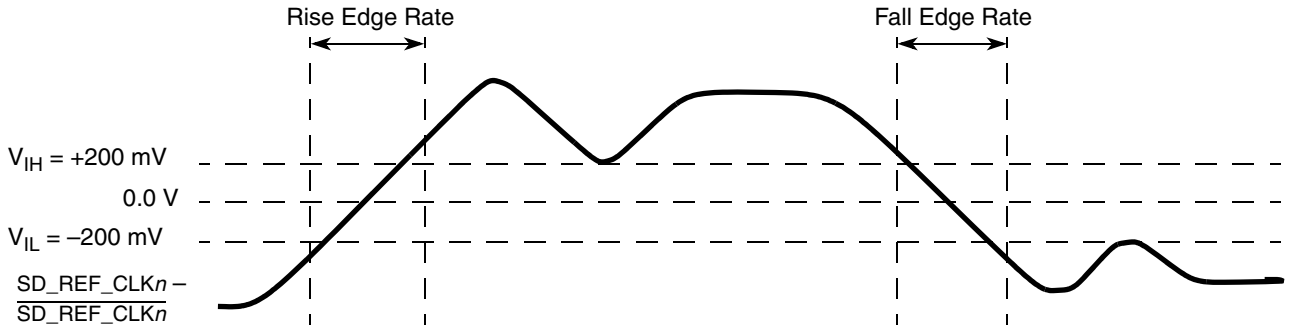


Figure 37. Differential Measurement Points for Rise and Fall Time

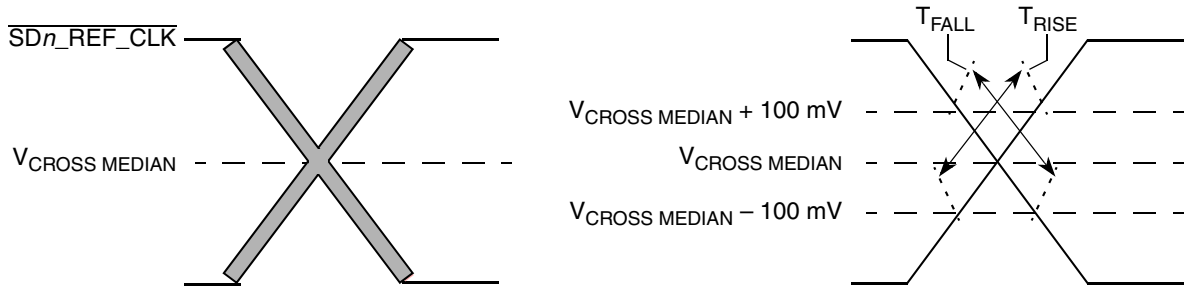


Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 Spread Spectrum Clock

SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

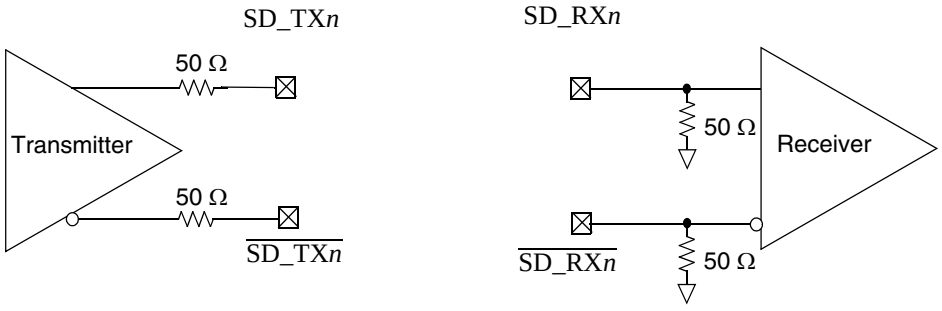


Figure 39. SerDes Transmitter and Receiver Reference Circuits

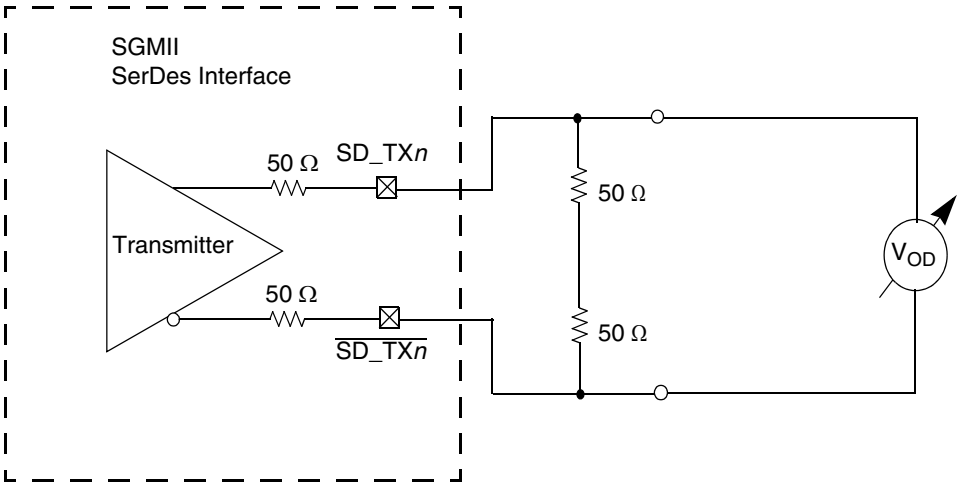


Figure 45. SGMII Transmitter DC Measurement Circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 88. SGMII 2.5x Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Output voltage	V_O	–0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—

Note:
1. Absolute output voltage limit

2.20.8.1.2 SGMII DC Receiver Electrical Characteristics

This table lists the SGMII DC receiver electrical characteristics for 1.25 GBaud. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 89. SGMII DC Receiver Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Typ	Max	Unit	Note
DC Input voltage range		—		N/A		—	1
Input differential voltage	REIDL_CTL = 001xx	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	REIDL_CTL = 100xx		175	—			
Loss of signal threshold	REIDL_CTL = 001xx	V_{LOS}	30	—	100	mV	3, 4
	REIDL_CTL = 100xx		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

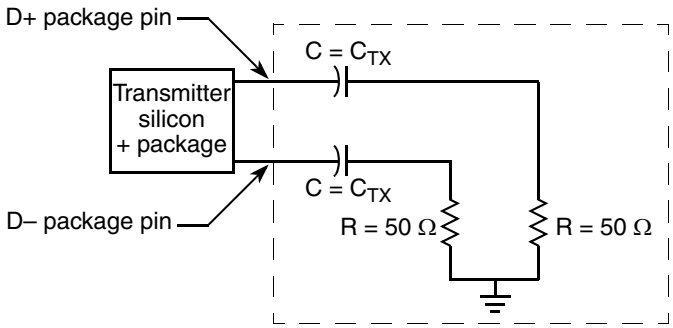


Figure 46. SGMII AC Test/Measurement Load

2.20.8.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 92. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Note:
1. Measured at receiver
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 System Clocking

This section describes the PLL configuration of the device.

This device includes six PLLs, as follows:

- There are two selectable core cluster PLLs that generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL; core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3,

Table 98. Asynchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:SYSCLK Ratio	Set MEM_PLL_CFG = 01 for SYSCLK Freq[1]
0_0101	5:1	>96.7 MHz
0_0110	6:1	>80.6 MHz
0_1000	8:1	>120.9 MHz
0_1001	9:1	>107.4 MHz
0_1010	10:1	>96.7 MHz
0_1100	12:1	>80.6 MHz
0_1101	13:1	>74.4 MHz
1_0000	16:1	>60.4 MHz
1_0010	18:1	>53.7 MHz
All Others	Reserved	—

Note:

1. Set RCW field MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock (SYSCLK) frequency is greater than the given cutoff; otherwise, set to 0b00 for a frequency that is less than or equal to the cutoff.

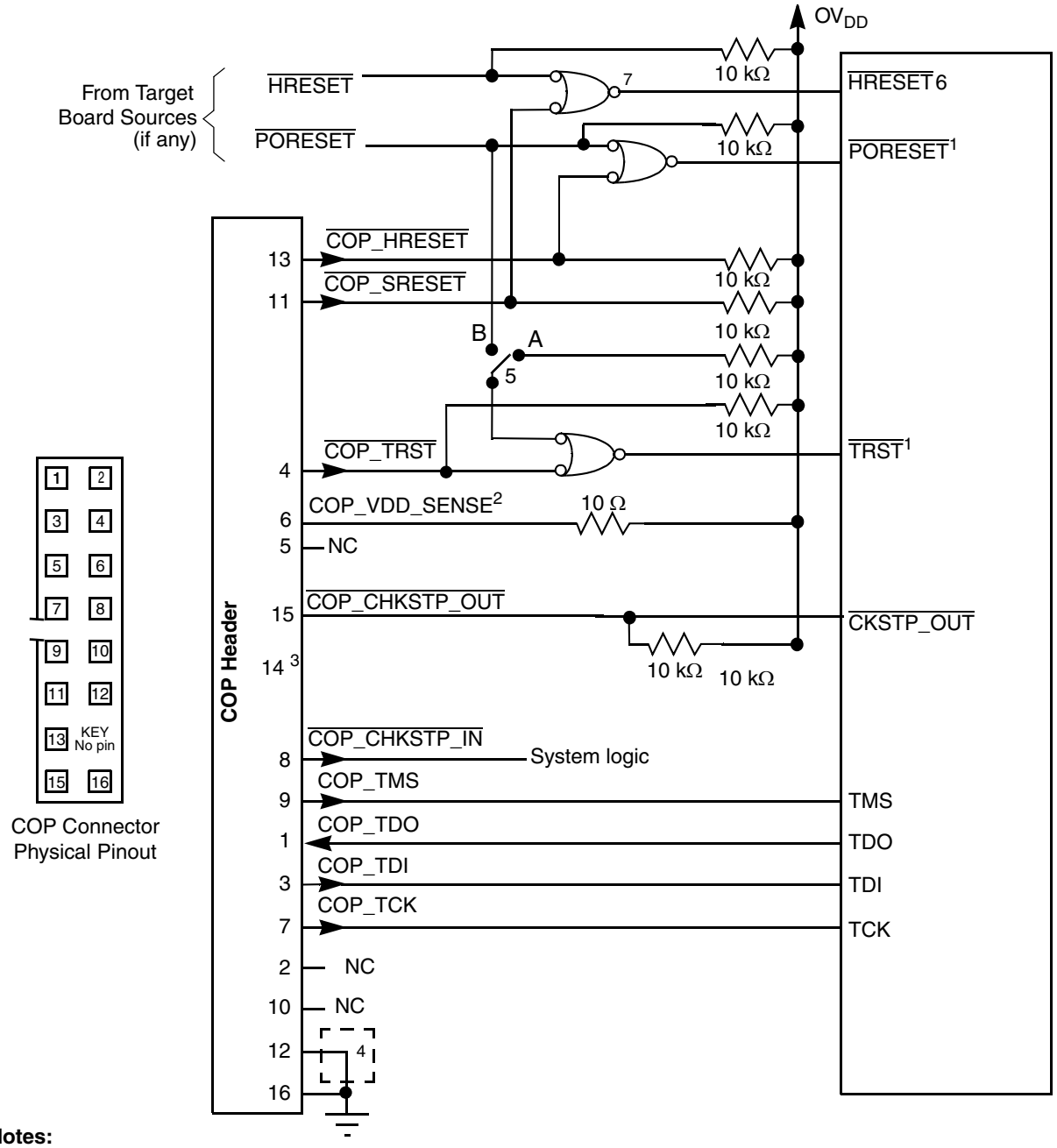
In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 99. Synchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:Platform CLK Ratio	Set MEM_PLL_CFG=01 for Platform CLK Freq[1]
0_0001	1:1	>600 MHz
All Others	Reserved	—

Note:

1. Set MEM_PLL_CFG=0b01 if the applied DDR PLL reference clock (Platform clock) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.



Notes:

1. The COP port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
6. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.
7. This is an open-drain gate.

Figure 55. Legacy JTAG Interface Connection

3.6.4.1 USB Divider Network

This figure shows the required divider network for the VBUS interface for the device. Additional requirements for the external components are as follows:

- Both resistors require 0.1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V–5.25 V.
- The 0.6 V diode requires an I_F = 10 mA, I_R < 500 nA and $V_{F(Max)}$ = 0.8 V.

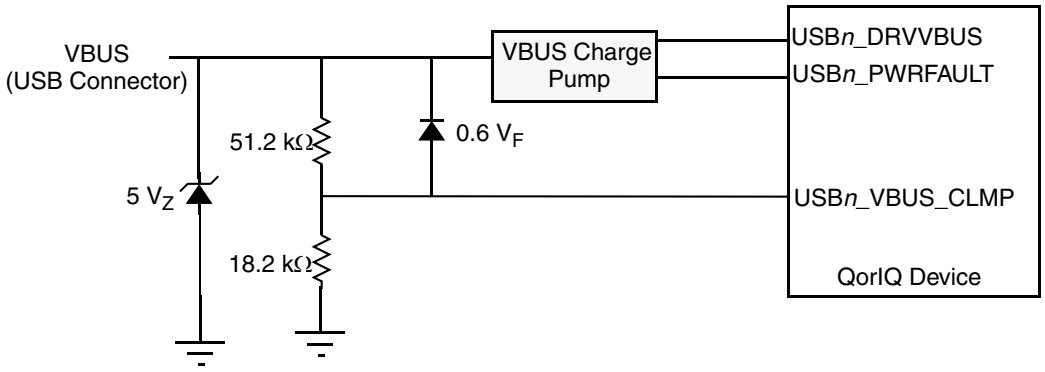


Figure 60. Divider Network at VBUS

USB1_DRVVBUS and USB1_PWRFAULT are muxed on GPIO[25] and GPIO[27] pins, respectively. USB2_DRVVBUS and USB2_PWRFAULT are muxed on GPIO[6:7] pins, respectively. Setting RCW[GPIO] selects USB functionality on the GPIO pins.

3.6.4.2 USB*n*_V_{DD}_1P8_DECAP Capacitor Options

The USB*n*_V_{DD}_1P8_DECAP pins require a capacitor connected to GND.

This table lists the recommended capacitors for the USBn_VDD_1P8_DECAP signal.

Table 106. Recommended Capacitor Parts for USB*n*_V_{DD}_1P8_DECAP

Manufacturer	Part Number	Value	ESR	Package
Kemet	T494B105(1)025A(2)	1 uF, 25 V	2 Ω	B(3528)
	T494B155(1)025A(2)	1.5 uF, 25 V	1.5 Ω	—
NIC	NMC0603X7R106KTRPF	1 uF, 10 V	Low ESR	0603
TDK Corporation	CERB2CX5R0G105M	1 uF, 4 V	200 m-Ω	0603
Vishay	TR3B105(1)035(2)1500	1 uF, 35 V	1.5 Ω	B(3528)

3.7 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

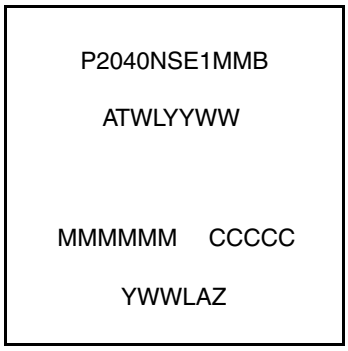
3.8 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow,

Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
P2040NSE1FLB P2040NSE7FLC	P	2	04 = 4 core	1	N = Industrial qualification	S = Std temp	E = SEC present	1= FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	F = 667 MHz	L = 1067 MT/s	B C
P2040NSN1FLB P2040NSN7FLC							N = SEC not present				
P2040NSE1HLB P2040NSE7HLC							E = SEC present		H = 800 MHz		
P2040NSN1HLB P2040NSN7HLC							N = SEC not present				
P2040NSE1KLB P2040NSE7KLC							E = SEC Present		K = 1000 MHz		
P2040NSN1KLB P2040NSN7KLC							N = SEC not present				
P2040NSE1MMB P2040NSE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NSN1MMB P2040NSN7MMC							N = SEC not present				
P2040NXE1FLB P2040NXE7FLC						X = Extended temp	E = SEC Present		F = 667 MHz	L = 1067 MT/s	
P2040NXN1FLB P2040NXN7FLC							N = SEC not present				
P2040NXE1MMB P2040NXE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NXN1MMB P2040NXN7MMC							N = SEC not present				

6.2.1 Part Marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Notes:

P2040NSE1MMB is the orderable part number. See Table 107 for details.

ATWLYYWW is the test traceability code.
MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

Figure 64. Part Marking for FC-PBGA Device

7 Revision History

This table provides a revision history for this document.

Table 108. Revision History

Rev. Number	Date	Description
2	02/2013	• In Table 7, “P2040 I/O Power Supply Estimated Values,” updated the USB power supply with USB_Vdd_3P3 and updated the typical value with “0.003” in the Others (Reset, System Clock, JTAG & Misc.) row. • In Table 8, “Device AVDD Power Dissipation,” removed V_{DD_LP} from table. • Added Table 10, “VDD_LP Power Dissipation.” • In Table 53, “MPIC Input AC Timing Specifications,” added Trust inputs AC timing and footnote 2. • In Table 93, “Processor Clocking Specifications,” updated footnote 8 with Rev 1.1 silicon. • In Table 107, “Part Numbering Nomenclature,” added “C” in the Die Revision collumn. • In Section 6.2, “Orderable Part Numbers Addressed by this Document,” added the device part numbers for Rev 2.0 silicon.