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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Security; SEC 4.2
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator, Secure Fusebox
Package / Case	780-BFBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2040nxe7mmc

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IRQ05/GPIO23/DMA2_DDONE0	External Interrupts	AA22	I	OV_{DD}	24
IRQ06/GPIO24/USB1_DRVVBUS	External Interrupts	Y26	I	OV_{DD}	24
IRQ07/GPIO25/USB1_PWRFAULT	External Interrupts	AA23	I	OV_{DD}	24
IRQ08/GPIO26/USB2_DRVVBUS	External Interrupts	AC22	I	OV_{DD}	24
IRQ09/GPIO27/USB2_PWRFAULT	External Interrupts	AC27	I	OV_{DD}	24
IRQ10/GPIO28/EVT7	External Interrupts	AB24	I	OV_{DD}	24
IRQ11/GPIO29/EVT8	External Interrupts	AC24	I	OV_{DD}	24
IRQ_OUT/EVT9	Interrupt Output	Y24	O	OV_{DD}	1, 2, 24
Trust					
TMP_DETECT	Tamper Detect	T24	I	OV_{DD}	25
LP_TMP_DETECT	Low Power Tamper Detect	L21	I	V_{DD_LP}	25
eSDHC					
SDHC_CMD	Command/Response	N22	I/O	CV_{DD}	—
SDHC_DAT0	Data	N23	I/O	CV_{DD}	—
SDHC_DAT1	Data	N26	I/O	CV_{DD}	—
SDHC_DAT2	Data	N27	I/O	CV_{DD}	—
SDHC_DAT3	Data	N28	I/O	CV_{DD}	—
SDHC_DAT4/SPI_CS0/GPIO00	Data	H26	I/O	CV_{DD}	24, 28
SDHC_DAT5/SPI_CS1/GPIO01	Data	H23	I/O	CV_{DD}	24, 28
SDHC_DAT6/SPI_CS2/GPIO02	Data	H27	I/O	CV_{DD}	24, 28
SDHC_DAT7/SPI_CS3/GPIO03	Data	H24	I/O	CV_{DD}	24, 28
SDHC_CLK	Host to Card Clock	N24	O	OV_{DD}	—
SDHC_CD/IIC3_SCL/GPIO16/ M1DVAL/LB_DVAL/DMA1_DACK0	Card Detection	AB23	I/O	OV_{DD}	24, 28
SDHC_WP/IIC3_SDA/GPIO17/ M1SRCID0/LB_SRCID0/DMA1_DDONE0	Card Write Protection	AB26	I	OV_{DD}	24, 28
eSPI					
SPI_MOSI	Master Out Slave In	H28	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	G23	I	CV_{DD}	—
SPI_CLK	eSPI Clock	H22	O	CV_{DD}	—
SPI_CS0/SDHC_DAT4/GPIO00	eSPI Chip Select	H26	O	CV_{DD}	24
SPI_CS1/SDHC_DAT5/GPIO01	eSPI Chip Select	H23	O	CV_{DD}	24
SPI_CS2/SDHC_DAT6/GPIO02	eSPI Chip Select	H27	O	CV_{DD}	24
SPI_CS3/SDHC_DAT7/GPIO03	eSPI Chip Select	H24	O	CV_{DD}	24

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_CA_PL16	Core Group A and Platform Supply	U13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL15	Core Group A and Platform Supply	U15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL14	Core Group A and Platform Supply	U20	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL13	Core Group A and Platform Supply	V9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL12	Core Group A and Platform Supply	V11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL11	Core Group A and Platform Supply	V13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL10	Core Group A and Platform Supply	V15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL09	Core Group A and Platform Supply	W9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL08	Core Group A and Platform Supply	W11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL07	Core Group A and Platform Supply	W13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL06	Core Group A and Platform Supply	W15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL05	Core Group A and Platform Supply	Y9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL04	Core Group A and Platform Supply	Y11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL03	Core Group A and Platform Supply	Y13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL02	Core Group A and Platform Supply	Y15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL01	Core Group A and Platform Supply	AA21	—	$V_{DD\_CA\_PL}$	37
VDD_CB11	Core Group B Supply	U16	—	V_{DD_CB}	37
VDD_CB10	Core Group B Supply	U18	—	V_{DD_CB}	37
VDD_CB09	Core Group B Supply	V18	—	V_{DD_CB}	37
VDD_CB08	Core Group B Supply	V20	—	V_{DD_CB}	37
VDD_CB07	Core Group B Supply	W16	—	V_{DD_CB}	37
VDD_CB06	Core Group B Supply	W18	—	V_{DD_CB}	37
VDD_CB05	Core Group B Supply	W20	—	V_{DD_CB}	37
VDD_CB04	Core Group B Supply	Y18	—	V_{DD_CB}	37
VDD_CB03	Core Group B Supply	Y20	—	V_{DD_CB}	37
VDD_CB02	Core Group B Supply	AA18	—	V_{DD_CB}	37
VDD_CB01	Core Group B Supply	AA20	—	V_{DD_CB}	37
VDD_LP	Low Power Security Monitor Supply	L20	—	V_{DD_LP}	25
AVDD_CC1	Core Cluster PLL1 Supply	V7	—	—	13
AVDD_CC2	Core Cluster PLL2 Supply	W22	—	—	13
AVDD_PLAT	Platform PLL Supply	V22	—	—	13
AVDD_DDR	DDR PLL Supply	W6	—	—	13
AVDD_SRDS1	SerDes PLL1 Supply	C1	—	—	13
AVDD_SRDS2	SerDes PLL2 Supply	A17	—	—	13

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
NC13	No Connection	F12	—	—	11
NC14	No Connection	F11	—	—	11
NC15	No Connection	F10	—	—	11
NC16	No Connection	F9	—	—	11
NC17	No Connection	F8	—	—	11
NC18	No Connection	E20	—	—	11
NC19	No Connection	E19	—	—	11
NC20	No Connection	E18	—	—	11
NC21	No Connection	E16	—	—	11
NC22	No Connection	E15	—	—	11
NC23	No Connection	E14	—	—	11
NC24	No Connection	E13	—	—	11
NC25	No Connection	E12	—	—	11
NC26	No Connection	E11	—	—	11
NC27	No Connection	E10	—	—	11
NC28	No Connection	E9	—	—	11
NC29	No Connection	E8	—	—	11
NC30	No Connection	E7	—	—	11
NC31	No Connection	D22	—	—	11
NC32	No Connection	D6	—	—	11
NC33	No Connection	D5	—	—	11
NC34	No Connection	C22	—	—	11
NC35	No Connection	C6	—	—	11
NC_M21	No Connection	M21	—	—	11
Reserved Pins					
Reserve	—	F24	—	1.2 V	20
Reserve	—	E23	—	1.2 V	20
Reserve	—	E5	—	—	11
Reserve	—	E6	—	—	11
Reserve	—	F14	—	—	11
Reserve	—	F15	—	—	11
Reserve	—	AB17	—	GND	19
Reserve	—	AB18	—	GND	19
Reserve	—	AB19	—	GND	19

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply Power Default Setting."

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the $V_{DD\_CA\_CB\_PL}$ supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power Up Sequencing," it is required that POV_{DD} = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5.

$V_{DD\_CA\_CB\_PL}$ and USB_V_{DD}_1P0 must be ramped down simultaneously. USB_V_{DD}_1P8_DECAP should starts ramping down only after USB_V_{DD}_3P3 is below 1.65 V.

2.4 Power Characteristics

This table shows the power dissipations of the $V_{DD\_CA\_CB\_PL}$ supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 6. Device Power Dissipation

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	1200	600	1200	500	1.0	65	10.3	—	9.8	—	—	2, 3
Thermal						105	14.2	—	13.8	—	—	5, 7
Maximum							14.8	13.5	14.0	12.8	1.4	4, 6, 7
Typical	1000	533	1067	467	1.0	65	9.2	—	8.6	—	—	2, 3
Thermal						105	12.5	—	12.1	—	—	5, 7
Maximum							13.0	11.7	12.3	11.0	1.4	4, 6, 7
Typical	800	534	1067	467	1.0	65	9.0	—	8.4	—	—	2, 3
Thermal						105	12.2	—	12.0	—	—	5, 7
Maximum							12.6	11.4	12.1	10.9	1.4	4, 6, 7

Table 11. Package Thermal Characteristics (continued)[6]

Rating	Board	Symbol	Value	Unit	Note
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	15	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	11	°C/W	1, 2
Junction to board	—	$R_{\Theta JB}$	6	°C/W	3
Junction to case top	—	$R_{\Theta JCtop}$	.53	°C/W	4
Junction to lid top	—	$R_{\Theta JClid}$	.16	°C/W	5

Note:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51–3 and JESD51-6 with the board (JESD51–9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51–8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.
6. Reference Section 3.8, "Thermal Management Information," for additional details.

2.6 Input Clocks

2.6.1 System Clock (SYSCLK) Timing Specifications

This table shows the SYSCLK DC electrical characteristics.

Table 12. SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	—	**15**	pf	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	±50	μA	2

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table shows the SYSCLK AC timing specifications.

2.12.2.2 RGMII AC Timing Specifications

This table shows the RGMII AC timing specifications.

Table 37. RGMII AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Note:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300ppm.

2.14 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 46. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 47. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 1.8 V.

Table 48. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.14.2 Enhanced Local Bus AC Timing Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

This figure shows the eLBC AC test load.

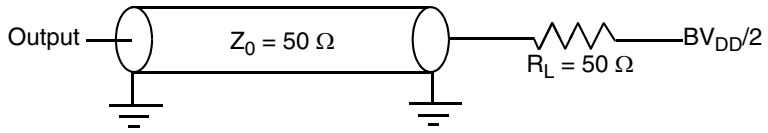


Figure 20. Enhanced Local Bus AC Test Load

2.14.2.1 Local Bus AC Timing Specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

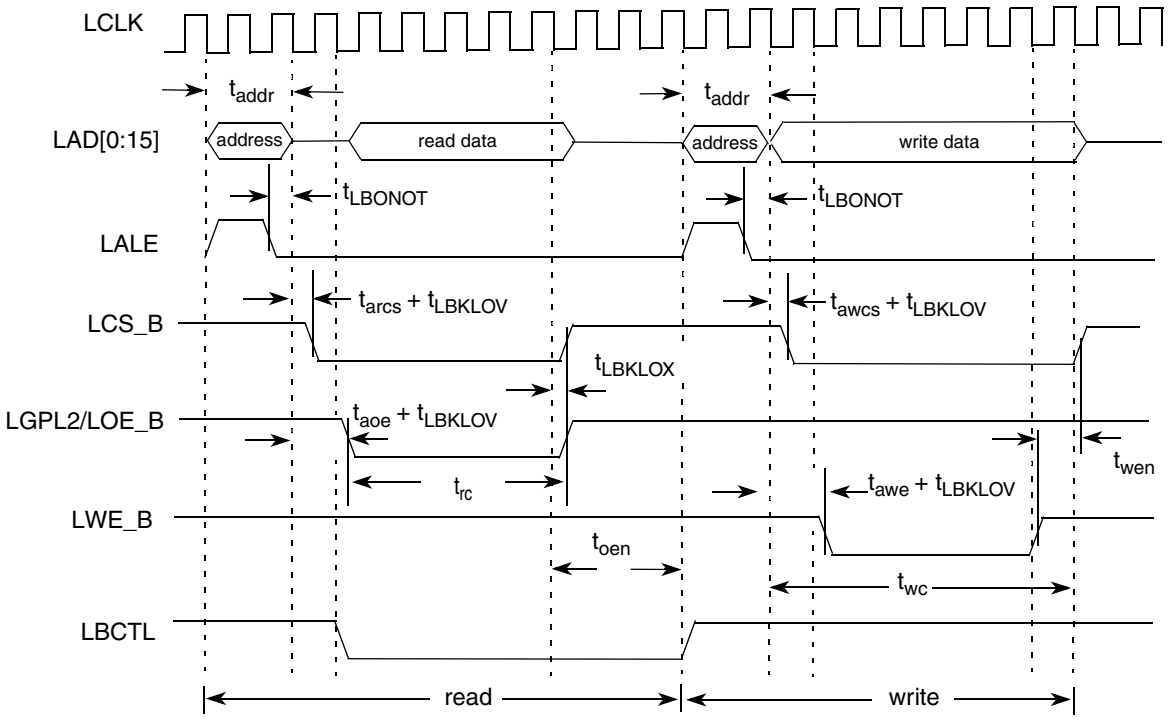
This table provides the eLBC timing specifications.

Table 49. Enhanced Local Bus Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—

This figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the chip reference manual.

Figure 22. GPCM Output Timing Diagram

2.15 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.15.1 eSDHC DC Electrical Characteristics

This table provides the eSDHC electrical characteristics.

Table 50. eSDHC Interface DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	$0.625 \times CV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	—	$0.25 \times CV_{DD}$	V	1
Input/output leakage current	I_{IN}/I_{OZ}	—	–50	50	μA	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at CV_{DD} min	$0.75 \times CV_{DD}$	—	V	—

2.17.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 25 through Figure 28.

Table 55. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at OVDD/2 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times Boundary-scan USB only Boundary (except USB) TDI, TMS	t_{JTDVKH}	 14 4 4	—	ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times Boundary-scan data TDO	t_{JTKLDV}	—	 15 10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3

Note:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

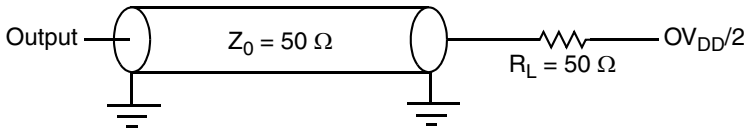


Figure 25. AC Test Load for the JTAG Interface

Table 65. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = $2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Note:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.20.4.5 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.5.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

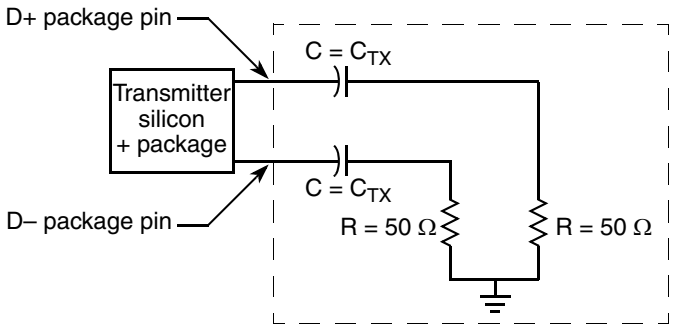


Figure 46. SGMII AC Test/Measurement Load

2.20.8.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 92. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Note:
1. Measured at receiver
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 System Clocking

This section describes the PLL configuration of the device.

This device includes six PLLs, as follows:

- There are two selectable core cluster PLLs that generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL; core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3,

"e500mc Core Cluster to SYSCLK PLL Ratio." The frequency for each core complex 0–3 is selected using the configuration bits as described in Table 96.

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Platform to SYSCLK PLL Ratio."
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in Section 3.1.5, "DDR Controller PLL Ratios."
- Each of the three SerDes blocks has a PLL which generate a core clock from their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.6, "Frequency Options."

3.1.1 Clock Ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 93. Processor Clocking Specifications

Parameter	Maximum Processor Core Frequency								Unit	Note
	667 MHz		800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500mc core PLL frequency	667	667	667	800	667	1000	667	1200	MHz	1,4
e500mc core frequency	333	667	333	800	333	1000	333	1200	MHz	4, 8
Platform clock frequency	400	533	400	533	400	533	400	600	MHz	1
Memory bus clock frequency	400	533	400	533	400	533	400	600	MHz	1,2,5,6
Local bus clock frequency	—	67	—	67	—	67	—	75	MHz	3
PME	—	267	—	267	—	267	—	300	MHz	7
FMan	—	467	—	467	—	467	—	500	MHz	—

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500-mc core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e500mc (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3 memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the chip reference manual for more information.
4. The e500mc core can run at e500mc core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 667 MHz, this results in a minimum allowable e500mc core frequency of 333 MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. The PME runs synchronously to the platform clock, running at a frequency of platform clock/2.
8. Core frequency must be at least as fast as the platform frequency (Rev 1.1 silicon).

3.1.4 e500mc Core Complex PLL Select

The clock frequency of each the e500mc core 0–3 complex is determined by the binary value of the RCW field CC*n*_PLL_SEL. These tables describe the supported ratios for each core complex 0–3, where each individual core complex can select a frequency from the table.

Table 96. e500mc Core Complex [0,1] PLL Select

Binary Value of C*n*_PLL_SEL for n=[0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0001	CC1 PLL /2
0100	CC2 PLL /1
All Others	Reserved

Table 97. e500mc Core Complex [2,3] PLL Select

Binary Value of C*n*_PLL_SEL for n=[0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0100	CC2 PLL /1
0101	CC2 PLL /2
All Others	Reserved

3.1.5 DDR Controller PLL Ratios

The single DDR memory controller complexes can be asynchronous to the platform, depending on configuration.

Table 98 describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in this table. This ratio is determined by the binary value of the RCW configuration field MEM_PLL_RAT[10:14].

The RCW configuration field MEM_PLL_CFG[8:9] must be set to MEM_PLL_CFG[8:9] = 0b01 if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in Table 98 for asynchronous DDR clock ratios; otherwise, set MEM_PLL_CFG[8:9] = 0b00.

NOTE

The RCW Configuration field DDR_SYNC (bit 184) must be set to 0b0 for asynchronous mode.

The RCW Configuration field DDR_RATE (bit 232) must be set to b’0 for asynchronous mode

The RCW Configuration field DDR_RSV0 (bit 234) must be set to b’0 for all ratios.

3.1.6 Frequency Options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and Platform Frequency Options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 100. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	66.66	83.33	100.00	111.11	133.33
	Platform Frequency (MHz)[1]				
4:1					533
5:1				555	
6:1			600		
7:1		583			
8:1	533				

[1] Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 47. Gen 1 PCI Express Minimum Platform Frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 48. Gen 2 PCI Express Minimum Platform Frequency

See Section 18.1.3.2, “Link Width,” in the chip reference manual for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width of the single widest port used (not combined width of the number ports used) as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times 0.8512 \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

Figure 49. sRIO Minimum Platform Frequency

Table 105. I/O Voltage Selection

Signals	Value (Binary)	VDD Voltage Selection		
		BVDD	CVDD	LVDD
IO_VSEL[0:4] Default (0_0000)	0_0000	3.3 V	3.3 V	3.3 V
	0_0001			2.5 V
	0_0010			Reserved
	0_0011	3.3 V	2.5 V	3.3 V
	0_0100			2.5 V
	0_0101			Reserved
	0_0110	3.3 V	1.8 V	3.3 V
	0_0111			2.5 V
	0_1000			Reserved
	0_1001	2.5 V	3.3 V	3.3 V
	0_1010			2.5 V
	0_1011			Reserved
	0_1100	2.5 V	2.5 V	3.3 V
	0_1101			2.5 V
	0_1110			Reserved
	0_1111	2.5 V	1.8 V	3.3 V
	1_0000			2.5 V
	1_0001			Reserved
	1_0010	1.8 V	3.3 V	3.3 V
	1_0011			2.5 V
	1_0100			Reserved
	1_0101	1.8 V	2.5 V	3.3 V
	1_0110			2.5 V
	1_0111			Reserved
	1_1000	1.8 V	1.8 V	3.3 V
	1_1001			2.5 V
	1_1010			Reserved
	1_1011	3.3 V	3.3 V	3.3 V
	1_1100			
	1_1101			
	1_1110			
	1_1111			

to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide, and direct.

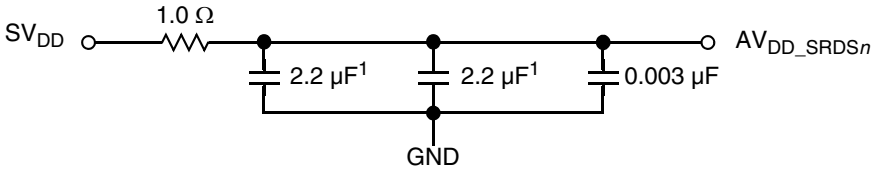


Figure 51. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD_SRDSn} must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn}.
- A 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} Power Supply Filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered GV_{DD}. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where XV_{DD} is sourced from GV_{DD}, is illustrated in Figure 52. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

C2 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

F1 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

F2 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

Bulk and decoupling capacitors are added, as needed, per power supply design.

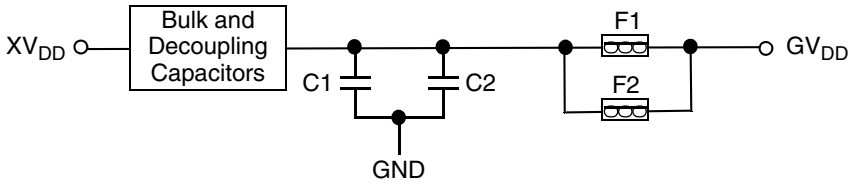


Figure 52. XV_{DD} Power Supply Filter Circuit

3.3.3 $USB\_V_{DD}\_1P0$ Power Supply Filtering

$USB\_V_{DD}\_1P0$ must be sourced by a filtered $V_{DD\_CA\_CB\_PL}$ using a star connection. An example solution for $USB\_V_{DD}\_1P0$ filtering, where $USB\_V_{DD}\_1P0$ is sourced from $V_{DD\_CA\_CB\_PL}$, is illustrated in Figure 53. The component values in this example filter is system dependent and are still under characterization; component values may need adjustment based on the system or environment noise.

Where:

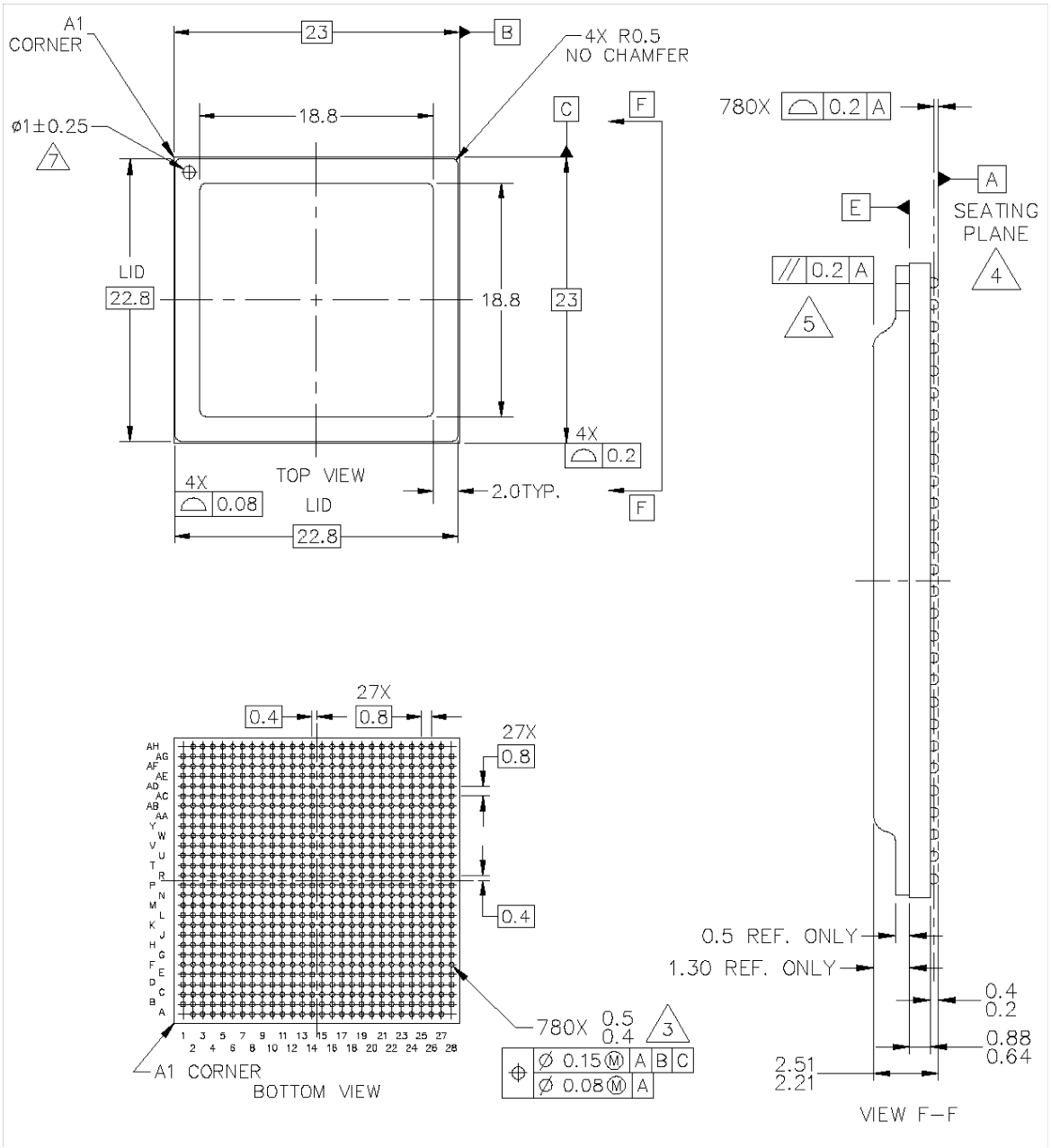
C1 = 2.2 µF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)

F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)

Bulk and decoupling capacitors are added, as needed, per power supply design.

4.2 Mechanical Dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the device.



Notes:

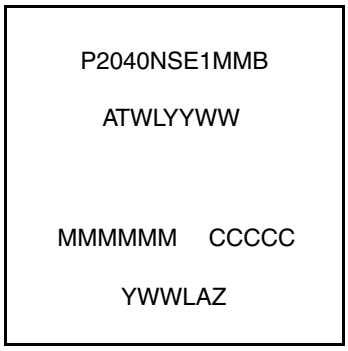
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement excludes any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
7. Pin 1 thru hole is centered within foot area.

Figure 63. Mechanical Dimensions of the FC-PBGA with Full Lid

Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
P2040NSE1FLB P2040NSE7FLC	P	2	04 = 4 core	1	N = Industrial qualification	S = Std temp	E = SEC present	1= FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	F = 667 MHz	L = 1067 MT/s	B C
P2040NSN1FLB P2040NSN7FLC							N = SEC not present				
P2040NSE1HLB P2040NSE7HLC							E = SEC present		H = 800 MHz		
P2040NSN1HLB P2040NSN7HLC							N = SEC not present				
P2040NSE1KLB P2040NSE7KLC							E = SEC Present		K = 1000 MHz		
P2040NSN1KLB P2040NSN7KLC							N = SEC not present				
P2040NSE1MMB P2040NSE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NSN1MMB P2040NSN7MMC							N = SEC not present				
P2040NXE1FLB P2040NXE7FLC						X = Extended temp	E = SEC Present		F = 667 MHz	L = 1067 MT/s	
P2040NXN1FLB P2040NXN7FLC							N = SEC not present				
P2040NXE1MMB P2040NXE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NXN1MMB P2040NXN7MMC							N = SEC not present				

6.2.1 Part Marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Notes:

P2040NSE1MMB is the orderable part number. See Table 107 for details.

ATWLYYWW is the test traceability code.
MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

Figure 64. Part Marking for FC-PBGA Device

7 Revision History

This table provides a revision history for this document.

Table 108. Revision History

Rev. Number	Date	Description
2	02/2013	• In Table 7, “P2040 I/O Power Supply Estimated Values,” updated the USB power supply with USB_Vdd_3P3 and updated the typical value with “0.003” in the Others (Reset, System Clock, JTAG & Misc.) row. • In Table 8, “Device AVDD Power Dissipation,” removed V_{DD_LP} from table. • Added Table 10, “VDD_LP Power Dissipation.” • In Table 53, “MPIC Input AC Timing Specifications,” added Trust inputs AC timing and footnote 2. • In Table 93, “Processor Clocking Specifications,” updated footnote 8 with Rev 1.1 silicon. • In Table 107, “Part Numbering Nomenclature,” added “C” in the Die Revision collumn. • In Section 6.2, “Orderable Part Numbers Addressed by this Document,” added the device part numbers for Rev 2.0 silicon.