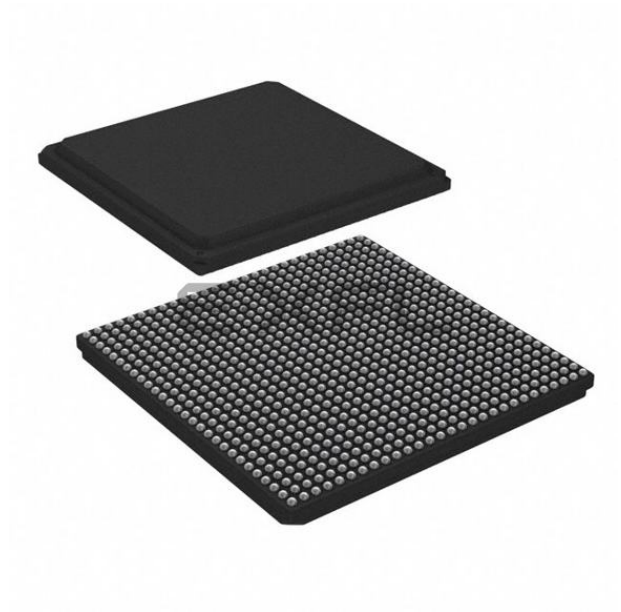

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500mc |
| Number of Cores/Bus Width | 4 Core, 32-Bit |
| Speed | 1.2GHz |
| Co-Processors/DSP | Security; SEC 4.2 |
| RAM Controllers | DDR3, DDR3L |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (5), 10Gbps (1) |
| SATA | SATA 3Gbps (2) |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Boot Security, Cryptography, Random Number Generator, Secure Fusebox |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-FCPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2041nse1mmb |

This figure shows the major functional units within the chip.

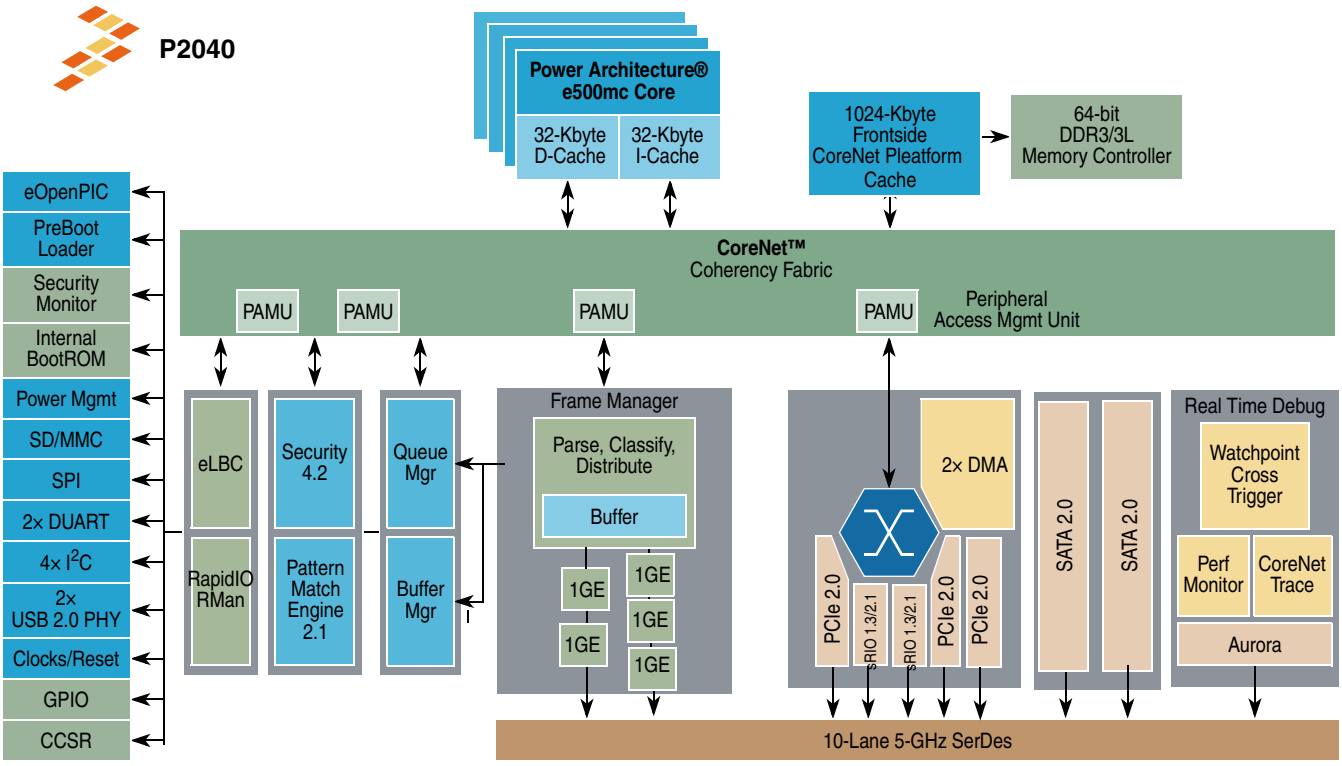



**Figure 1. Block Diagram**

# 1 Pin Assignments and Reset States

This section provides a top view of the ball layout diagram and four detailed views by quadrant. It also provides a pinout listing by bus.

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| MCK0 | Clock | AD14 | O | $GV_{DD}$ | — |
| MCK1 | Clock | AE13 | O | $GV_{DD}$ | — |
| MCK2 | Clock | AG13 | O | $GV_{DD}$ | — |
| MCK3 | Clock | AG14 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK0}}$ | Clock Complements | AE14 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK1}}$ | Clock Complements | AD13 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK2}}$ | Clock Complements | AH13 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK3}}$ | Clock Complements | AH14 | O | $GV_{DD}$ | — |
| MODT0 | On Die Termination | AC19 | O | $GV_{DD}$ | — |
| MODT1 | On Die Termination | AD22 | O | $GV_{DD}$ | — |
| MODT2 | On Die Termination | AG18 | O | $GV_{DD}$ | — |
| MODT3 | On Die Termination | AH21 | O | $GV_{DD}$ | — |
| MDIC0 | Driver Impedance Calibration | AG12 | I/O | $GV_{DD}$ | 16 |
| MDIC1 | Driver Impedance Calibration | AE12 | I/O | $GV_{DD}$ | 16 |
| **Local Bus Controller Interface** | | | | | |
| LAD00 | Muxed Data/Address | J6 | I/O | $BV_{DD}$ | 3 |
| LAD01 | Muxed Data/Address | J4 | I/O | $BV_{DD}$ | 3 |
| LAD02 | Muxed Data/Address | K2 | I/O | $BV_{DD}$ | 3 |
| LAD03 | Muxed Data/Address | K4 | I/O | $BV_{DD}$ | 3 |
| LAD04 | Muxed Data/Address | L1 | I/O | $BV_{DD}$ | 3 |
| LAD05 | Muxed Data/Address | J5 | I/O | $BV_{DD}$ | 3 |
| LAD06 | Muxed Data/Address | N5 | I/O | $BV_{DD}$ | 3 |
| LAD07 | Muxed Data/Address | N2 | I/O | $BV_{DD}$ | 3 |
| LAD08 | Muxed Data/Address | N3 | I/O | $BV_{DD}$ | 3 |
| LAD09 | Muxed Data/Address | N1 | I/O | $BV_{DD}$ | 3 |
| LAD10 | Muxed Data/Address | P4 | I/O | $BV_{DD}$ | 3 |
| LAD11 | Muxed Data/Address | R7 | I/O | $BV_{DD}$ | 3 |
| LAD12 | Muxed Data/Address | T4 | I/O | $BV_{DD}$ | 3 |
| LAD13 | Muxed Data/Address | U2 | I/O | $BV_{DD}$ | 3 |
| LAD14 | Muxed Data/Address | T6 | I/O | $BV_{DD}$ | 3 |
| LAD15 | Muxed Data/Address | T7 | I/O | $BV_{DD}$ | 3 |
| LA16 | Address | K6 | I/O | $BV_{DD}$ | 31 |
| LA17 | Address | K3 | I/O | $BV_{DD}$ | 31 |
| LA18 | Address | P6 | I/O | $BV_{DD}$ | 31 |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| **DMA** | | | | | |
| DMA1_DREQ0/IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/GPIO18 | DMA1 Channel 0 Request | AC23 | I | $OV_{DD}$ | 24 |
| DMA1_DACK0/IIC3_SCL/GPIO16/SDHC_CD/ M1DVAL/LB_DVAL | DMA1 Channel 0 Acknowledge | AB23 | O | $OV_{DD}$ | 2, 14 |
| DMA1_DDONE0/IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0/SDHC_WP | DMA1 Channel 0 Done | AB26 | O | $OV_{DD}$ | 2, 14 |
| DMA2_DREQ0/IRQ03/GPIO21 | DMA2 Channel 0 Request | AA26 | I | $OV_{DD}$ | 24 |
| DMA2_DACK0/IRQ04/GPIO22 | DMA2 Channel 0 Acknowledge | V25 | O | $OV_{DD}$ | 24 |
| DMA2_DDONE0/IRQ05/GPIO23 | DMA2 Channel 0 Done | AA22 | O | $OV_{DD}$ | 24 |
| **USB Host Port 1** | | | | | |
| USB1_UDP | USB1 PHY Data Plus | K28 | I/O | $USB\_V_{DD}\_3P3$ | — |
| USB1_UDM | USB1 PHY Data Minus | L28 | I/O | $USB\_V_{DD}\_3P3$ | — |
| USB1_VBUS_CLMP | USB1 PHY VBUS Divided Signals | M25 | I | $USB\_V_{DD}\_3P3$ | 34 |
| USB1_UID | USB1 PHY ID Detect | M27 | I | $USB\_V_{DD}\_3P3$ | — |
| USB_CLKIN | USB PHY Clock Input | P22 | I | $OV_{DD}$ | — |
| USB1_DRVVBUS/GPIO24/IRQ6 | USB1 5V Supply Enable | Y26 | O | $OV_{DD}$ | — |
| USB1_PWRFAULT/GPIO25/IRQ7 | USB Power Fault | AA23 | I | $OV_{DD}$ | — |
| **USB Host Port 2** | | | | | |
| USB2_UDP | USB2 PHY Data Plus | K26 | I/O | $USB\_V_{DD}\_3P3$ | — |
| USB2_UDM | USB2 PHY Data Minus | L26 | I/O | $USB\_V_{DD}\_3P3$ | — |
| USB2_VBUS_CLMP | USB2 PHY VBUS Divided Signals | J25 | I | $USB\_V_{DD}\_3P3$ | 34 |
| USB2_UID | USB2 PHY ID Detect | J27 | I | $USB\_V_{DD}\_3P3$ | — |
| USB2_DRVVBUS/GPIO26/IRQ8 | USB2 5V Supply Enable | AC22 | I/O | $OV_{DD}$ | — |
| USB2_PWRFAULT/GPIO27/IRQ9 | USB2 Power Fault | AC27 | I/O | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | | |
| IRQ00 | External Interrupts | Y25 | I | $OV_{DD}$ | — |
| IRQ01 | External Interrupts | AB27 | I | $OV_{DD}$ | — |
| IRQ02 | External Interrupts | AB25 | I | $OV_{DD}$ | — |
| IRQ03/GPIO21/DMA2_DREQ0 | External Interrupts | AA26 | I | $OV_{DD}$ | 24 |
| IRQ04/GPIO22/DMA2_DACK0 | External Interrupts | V25 | I | $OV_{DD}$ | 24 |

**Table 1. Pin List by Bus (continued)**

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|---|
| USB1_AGND01 | USB1 PHY Transceiver GND | M28 | — | — | — |
| USB2_AGND06 | USB2 PHY Transceiver GND | J22 | — | — | — |
| USB2_AGND05 | USB2 PHY Transceiver GND | J24 | — | — | — |
| USB2_AGND04 | USB2 PHY Transceiver GND | J26 | — | — | — |
| USB2_AGND03 | USB2 PHY Transceiver GND | K25 | — | — | — |
| USB2_AGND02 | USB2 PHY Transceiver GND | L25 | — | — | — |
| USB2_AGND01 | USB2 PHY Transceiver GND | M26 | — | — | — |
| OVDD06 | General I/O Supply | N20 | — | $OV_{DD}$ | — |
| OVDD05 | General I/O Supply | P20 | — | $OV_{DD}$ | — |
| OVDD04 | General I/O Supply | R20 | — | $OV_{DD}$ | — |
| OVDD03 | General I/O Supply | T20 | — | $OV_{DD}$ | — |
| OVDD02 | General I/O Supply | T26 | — | $OV_{DD}$ | — |
| OVDD01 | General I/O Supply | W26 | — | $OV_{DD}$ | — |
| CVDD2 | eSPI and eSDHC Supply | K20 | — | $CV_{DD}$ | — |
| CVDD1 | eSPI and eSDHC Supply | M20 | — | $CV_{DD}$ | — |
| GVDD17 | DDR Supply | AA8 | — | $GV_{DD}$ | — |
| GVDD16 | DDR Supply | AA9 | — | $GV_{DD}$ | — |
| GVDD15 | DDR Supply | AA10 | — | $GV_{DD}$ | — |
| GVDD14 | DDR Supply | AA11 | — | $GV_{DD}$ | — |
| GVDD13 | DDR Supply | AA12 | — | $GV_{DD}$ | — |
| GVDD12 | DDR Supply | AA13 | — | $GV_{DD}$ | — |
| GVDD11 | DDR Supply | AA14 | — | $GV_{DD}$ | — |
| GVDD10 | DDR Supply | AA15 | — | $GV_{DD}$ | — |
| GVDD09 | DDR Supply | AB13 | — | $GV_{DD}$ | — |
| GVDD08 | DDR Supply | AB14 | — | $GV_{DD}$ | — |
| GVDD07 | DDR Supply | AC13 | — | $GV_{DD}$ | — |
| GVDD06 | DDR Supply | AC14 | — | $GV_{DD}$ | — |
| GVDD05 | DDR Supply | AF6 | — | $GV_{DD}$ | — |
| GVDD04 | DDR Supply | AF9 | — | $GV_{DD}$ | — |
| GVDD03 | DDR Supply | AF17 | — | $GV_{DD}$ | — |
| GVDD02 | DDR Supply | AF20 | — | $GV_{DD}$ | — |
| GVDD01 | DDR Supply | AF23 | — | $GV_{DD}$ | — |
| BVDD07 | Local Bus Supply | J7 | — | $BV_{DD}$ | — |
| BVDD06 | Local Bus Supply | K7 | — | $BV_{DD}$ | — |

This table shows the estimated power dissipation on the $AV_{DD}$ and $AV_{DD\_SRDS}$ supplies for the device PLLs, at allowable voltage levels.

**Table 8. Device $AV_{DD}$ Power Dissipation**

| $AV_{DD}$s | Typical | Maximum | Unit | Note |
|---|---|---|---|---|
| $AV_{DD\_DDR}$ | 5 | 15 | mW | 1 |
| $AV_{DD\_CC1}$ | | | | |
| $AV_{DD\_CC2}$ | | | | |
| $AV_{DD\_PLAT}$ | | | | |
| $AV_{DD\_SRDS1}$ | — | 36 | mW | 2 |
| $AV_{DD\_SRDS2}$ | | | | |
| USB_$V_{DD_1P0}$ | — | 10 | mW | 3 |

**Note:**

1. $V_{DD\_CA\_CB\_PL}$, $T_A$ = 80°C, $T_J$ = 105°C
2. $SV_{DD}$ = 1.0 V, $T_A$ = 80°C, $T_J$ = 105°C
3. USB_$V_{DD_1P0}$ = 1.0V, $T_A$ = 80°C, $T_J$ = 105°C

This table shows the estimated power dissipation on the $POV_{DD}$ supply for the chip at allowable voltage levels.

**Table 9. $POV_{DD}$ Power Dissipation**

| Supply | Maximum | Unit | Notes |
|---|---|---|---|
| $POV_{DD}$ | 450 | mW | 1 |

**Note:**

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the $V_{DD\_LP}$ supply for the device, at allowable voltage levels.

**Table 10. $V_{DD\_LP}$ Power Dissipation**

| Supply | Maximum | Unit | Notes |
|---|---|---|---|
| $V_{DD\_LP}$ (Device on, 105C) | 1.5 | mW | 1 |
| $V_{DD\_LP}$ (Device off, 70C) | 195 | uW | 2 |
| $V_{DD\_LP}$ (Device off, 40C) | 132 | uW | 2 |

**Note:**

1. $V_{DD\_LP}$ = 1.0 V, $T_J$ = 105°C.
2. When the device is off, $V_{DD\_LP}$ may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC, which switches $V_{DD\_LP}$ to battery when the SoC is powered down. See the Trust Architecture chapter in the device reference manual for more information.

## 2.5 Thermal

**Table 11. Package Thermal Characteristics [6]**

| Rating | Board | Symbol | Value | Unit | Note |
|---|---|---|---|---|---|
| Junction to ambient, natural convection | Single-layer board (1s) | $R_{\Theta JA}$ | 21 | °C/W | 1, 2 |
| Junction to ambient, natural convection | Four-layer board (2s2p) | $R_{\Theta JA}$ | 15 | °C/W | 1, 3 |

**Table 13. SYSCLK AC Timing Specifications**

For recommended operating conditions, see Table 3.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | 67 | — | 133 | MHz | 1, 2 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 7.5 | — | 15 | ns | 1, 2 |
| SYSCLK duty cycle | $t_{KHK}/t_{SYSCLK}$ | 40 | — | 60 | % | 2 |
| SYSCLK slew rate | — | 1 | — | 4 | V/ns | 3 |
| SYSCLK peak period jitter | — | — | — | ±150 | ps | — |
| SYSCLK jitter phase noise at – 56dBc | — | — | — | 500 | KHz | 4 |
| AC Input Swing Limits at 3.3 V $OV_{DD}$ | $\Delta V_{AC}$ | 1.9 | — | — | V | — |

**Note:**

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD} \div 2$.
3. Slew rate as measured from ± 0.3 $\Delta \mathbf{V_{AC}}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

## 2.6.2 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the device input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the device is compatible with spread spectrum sources if the recommendations listed in this table are observed.

**Table 14. Spread Spectrum Clock Source Recommendations**

For recommended operating conditions, see Table 3.

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| Frequency modulation | — | 60 | kHz | — |
| Frequency spread | — | 1.0 | % | 1, 2 |

**Note:**

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

**CAUTION**

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

## 2.9.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

**Table 20. DDR3 SDRAM Interface DC Electrical Characteristics ($GV_{DD}$ = 1.5 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| I/O reference voltage | $MV_{REF}n$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 1, 2, 3, 4 |
| Input high voltage | $V_{IH}$ | $MV_{REF}n$ + 0.100 | $GV_{DD}$ | V | 5 |
| Input low voltage | $V_{IL}$ | GND | $MV_{REF}n$ – 0.100 | V | 5 |
| I/O leakage current | $I_{OZ}$ | –50 | 50 | μA | 6 |

**Note:**

1. $GV_{DD}$ is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. $MV_{REF}n$ is expected to be equal to 0.5 × $GV_{DD}$ and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed the $MV_{REF}n$ DC level by more than ±1% of the DC value (that is, ±15mV).
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $MV_{REF}n$ with a min value of $MV_{REF}n$ – 0.04 and a max value of $MV_{REF}n$ + 0.04. $V_{TT}$ should track variations in the DC level of $MV_{REF}n$.
4. The voltage regulator for $MV_{REF}n$ must meet the specifications stated in Table 23.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

**Table 21. DDR3L SDRAM Interface DC Electrical Characteristics ($GV_{DD}$ = 1.35 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| I/O reference voltage | $MV_{REF}n$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 1, 2, 3, 4 |
| Input high voltage | $V_{IH}$ | $MV_{REF}n$ + 0.090 | $GV_{DD}$ | V | 5 |
| Input low voltage | $V_{IL}$ | GND | $MV_{REF}n$ – 0.090 | V | 5 |
| I/O leakage current | $I_{OZ}$ | –50 | 50 | μA | 6 |
| Output high current ($V_{OUT}$ = 0.641 V) | $I_{OH}$ | — | –23.8 | mA | 7, 8 |
| Output low current ($V_{OUT}$ = 0.641 V) | $I_{OL}$ | 23.8 | — | mA | 7, 8 |

### 2.9.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

**Table 24. DDR3 SDRAM Interface Input AC Timing Specifications**

For recommended operating conditions, see Table 3.

| Parameter | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| AC input low voltage | > 1200 MT/s data rate | $V_{ILAC}$ | — | MVREF*n* – 0.150 | V | — |
| | ≤ 1200 MT/s data rate | | | MVREF*n* – 0.175 | | |
| AC input high voltage | > 1200 MT/s data rate | $V_{IHAC}$ | MVREF*n* + 0.150 | — | V | — |
| | ≤ 1200 MT/s data rate | | MVREF*n* + 0.175 | | | |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

**Table 25. DDR3L SDRAM Interface Input AC Timing Specifications**

For recommended operating conditions, see Table 3.

| Parameter | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| AC input low voltage | > 1200 MT/s data rate | $V_{ILAC}$ | — | MVREF*n* – 0.135 | V | — |
| | ≤ 1200 MT/s data rate | | — | MVREF*n* – 0.160 | | |
| AC input high voltage | > 1200 MT/s data rate | $V_{IHAC}$ | MVREF*n* + 0.135 | — | V | — |
| | ≤ 1200 MT/s data rate | | MVREF*n* + 0.160 | — | | |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

**Table 26. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Controller Skew for MDQS—MDQ/MECC | $t_{CISKEW}$ | | | ps | 1 |
| 1200 MT/s data rate | | –142 | 142 | | |
| 1066 MT/s data rate | | –170 | 170 | | |
| 800 MT/s data rate | | –200 | 200 | | |
| Tolerated Skew for MDQS—MDQ/MECC | $t_{DISKEW}$ | | | ps | 2 |
| 1200 MT/s data rate | | –275 | 275 | | |
| 1066 MT/s data rate | | –300 | 300 | | |
| 800 MT/s data rate | | –425 | 425 | | |

**Note:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of $t_{CISKEW}$.

This figure represents the AC timing from Table 33 in master mode (internal clock). Note that although timing specifications generally refer to the rising edge of the clock, this figure also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

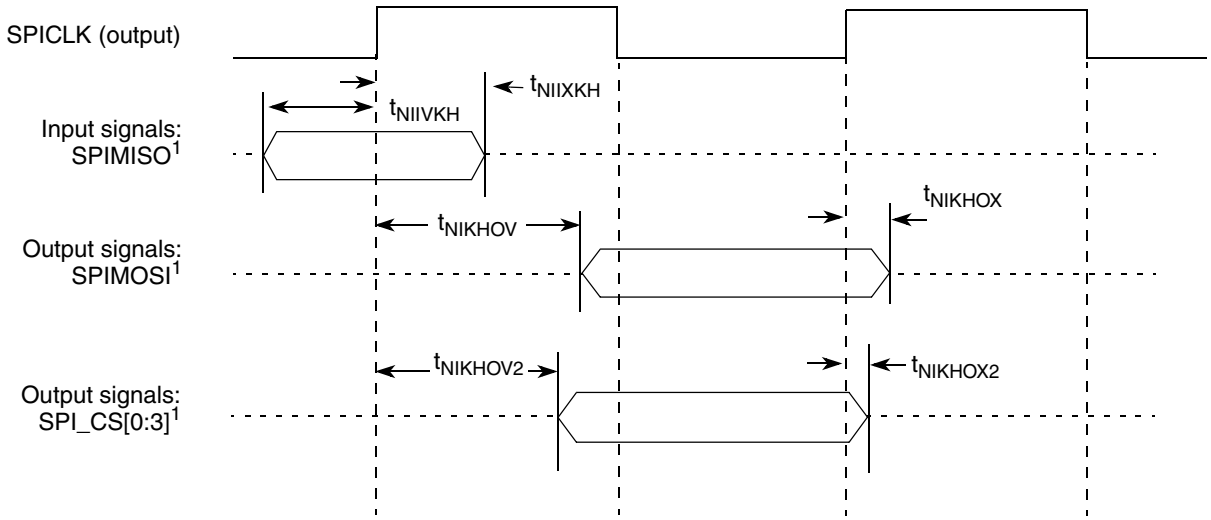



**Figure 15. eSPI AC Timing in Master Mode (Internal Clock) Diagram**

## 2.11 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

### 2.11.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 34. DUART DC Electrical Characteristics ($OV_{DD}$ = 3.3 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The symbol $OV_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 3.
2. The symbol $OV_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This figure shows the AC timing diagram of the local bus interface.

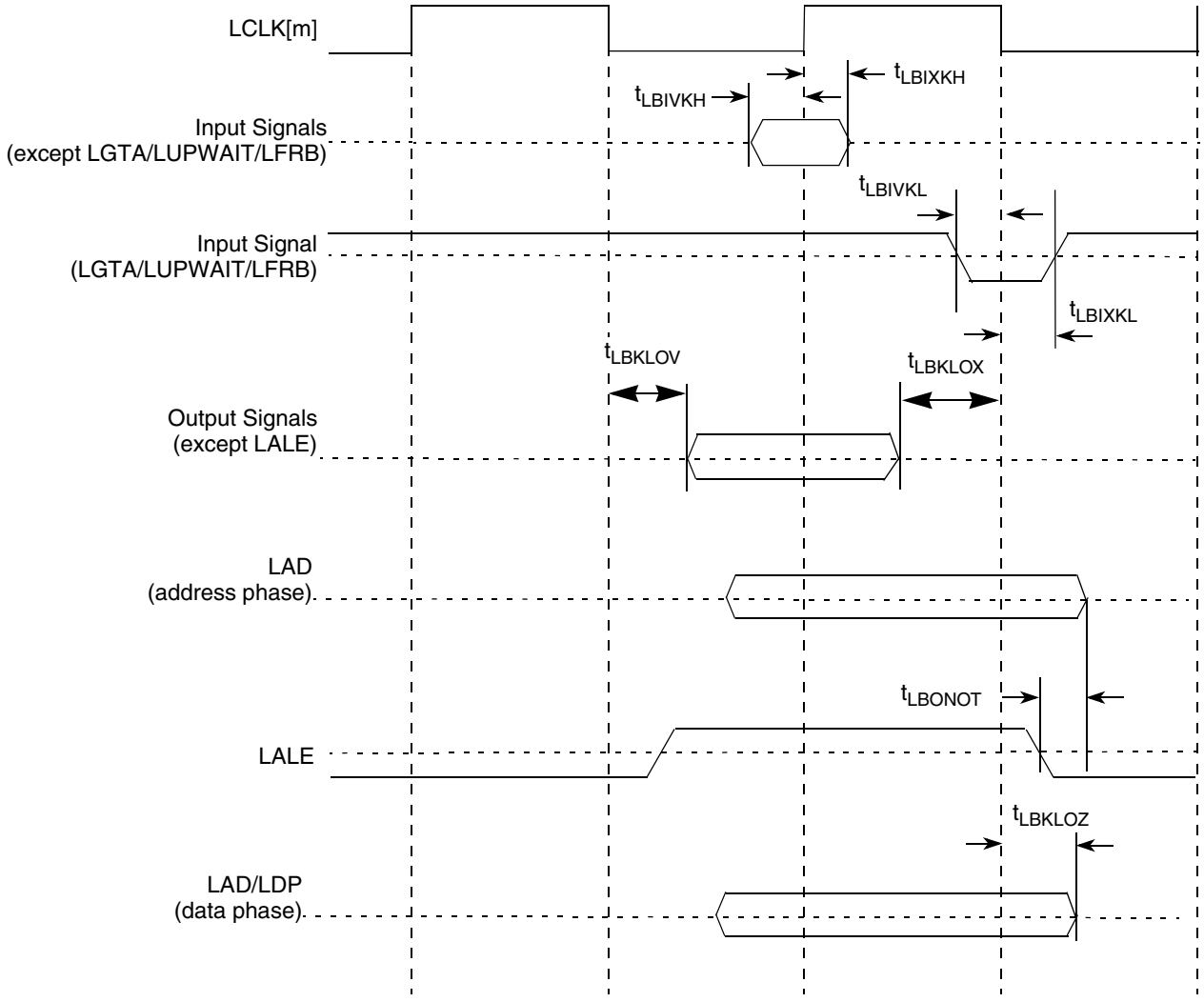



**Figure 21. Enhanced Local Bus Signals**

Figure 22 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by $t_{acs}$ (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

### 2.20.2.3 AC Requirements for SerDes Reference Clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO, SATA and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

**Table 61. SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ Input Clock Requirements ($SV_{DD}$ = 1.0 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range | $t_{CLK\_REF}$ | — | 100/125/156.25 | — | MHz | 1 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance | $t_{CLK\_TOL}$ | –350 | — | 350 | ppm | — |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle | $t_{CLK\_DUTY}$ | 40 | 50 | 60 | % | 4 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at $10^{-6}$ BER | $t_{CLK\_DJ}$ | — | — | 42 | ps | — |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at $10^{-6}$ BER (peak-to-peak jitter at refClk input) | $t_{CLK\_TJ}$ | — | — | 86 | ps | 2 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate | $t_{CLKRR}/t_{CLKFR}$ | 1 | — | 4 | V/ns | 3 |
| Differential input high voltage | $V_{IH}$ | 200 | — | — | mV | 4 |
| Differential input low voltage | $V_{IL}$ | — | — | –200 | mV | 4 |
| Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching | Rise-Fall Matching | — | — | 20 | % | 5, 6 |

**Note:**

1. **Caution:** Only 100, 125 and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.

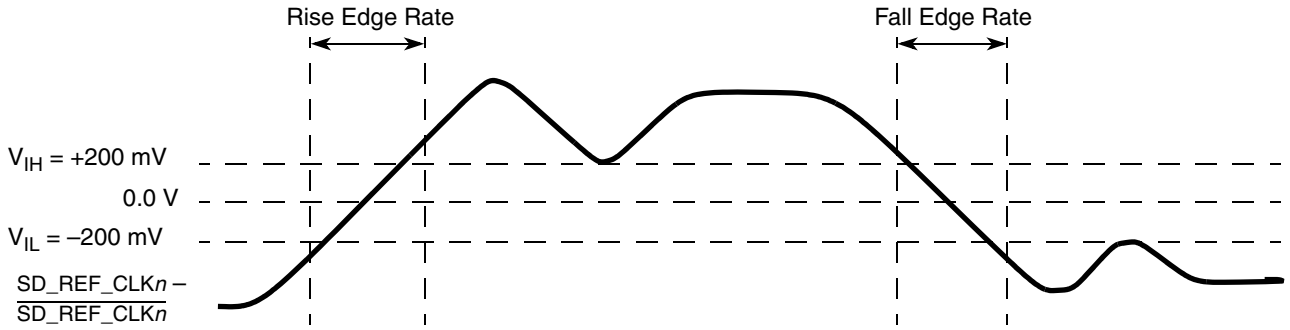



**Figure 37. Differential Measurement Points for Rise and Fall Time**

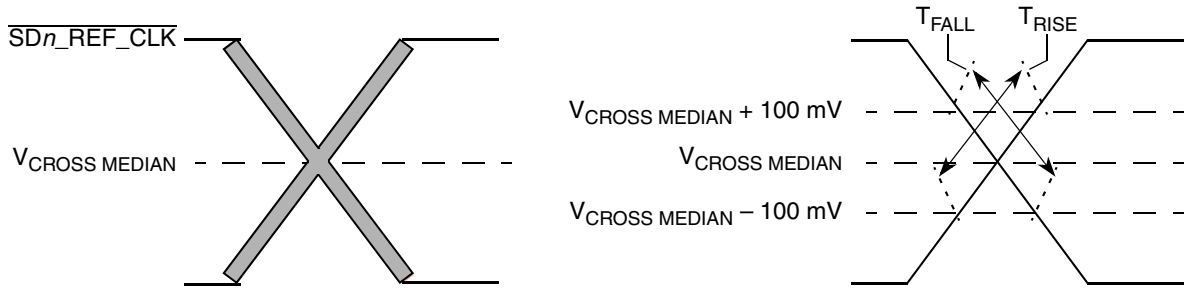



**Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching**

### 2.20.2.4 Spread Spectrum Clock

SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

## 2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

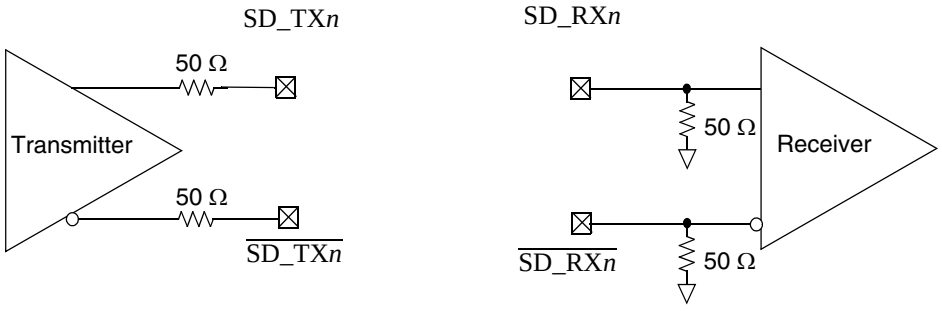



**Figure 39. SerDes Transmitter and Receiver Reference Circuits**

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

**Table 64. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input DC Specifications ($XV_{DD}$ = 1.5 V or 1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$ | 120 | — | 1200 | mV | $V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1. |
| DC differential input impedance | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Rx DC differential mode impedance. See Note 2 |
| DC input impedance | $Z_{RX-DC}$ | 40 | 50 | 60 | Ω | Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2. |
| Powered down DC input impedance | $Z_{RX-HIGH-IMP-DC}$ | 50 k | — | — | Ω | Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3. |
| Electrical idle detect threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver |

**Note:**

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

**Table 65. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications ($XV_{DD}$ = 1.5 V or 1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$ | 120 | — | 1200 | V | $V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1. |
| DC differential input impedance | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Rx DC Differential mode impedance. See Note 2 |
| DC input impedance | $Z_{RX-DC}$ | 40 | 50 | 60 | Ω | Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2. |
| Powered down DC input impedance | $Z_{RX-HIGH-IMP-DC}$ | 50 | — | — | kΩ | Required Rx D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 3. |

**Table 69. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input AC Specifications (continued)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Max Rx inherent deterministic timing error | $T_{RX-DJ-DD-CC}$ | — | — | 0.30 | UI | The maximum inherent deterministic timing error for common RefClk Rx architecture |
| Max Rx inherent deterministic timing error | $T_{RX-DJ-DD-DC}$ | — | — | 0.24 | UI | The maximum inherent deterministic timing error for common RefClk Rx architecture |

**Note:**

1. No test load is necessarily associated with this value.

### 2.20.4.6 Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in this figure.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

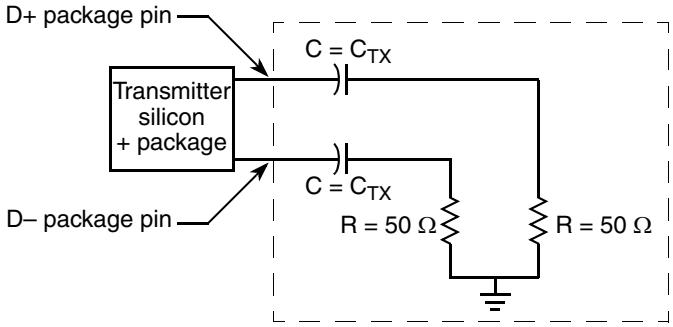



**Figure 40. Test/Measurement Load**

## 2.20.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125, and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

**Table 83. Gen1i/1.5 G Transmitter (Tx) AC Specifications (continued)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|

**Note:**
1. Measured at Tx output pins peak to peak phase variation, random data pattern

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

**Table 84. Gen 2i/3 G Transmitter (Tx) AC Specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Channel speed | $t_{CH\_SPEED}$ | — | 3.0 | — | Gbps | — |
| Unit Interval | $T_{UI}$ | 333.2167 | 333.3333 | 335.1167 | ps | — |
| Total jitter $f_{C3dB} = f_{BAUD} \div 10$ | $U_{SATA\_TXTJfB/10}$ | — | — | 0.3 | UI p-p | 1 |
| Total jitter $f_{C3dB} = f_{BAUD} \div 500$ | $U_{SATA\_TXTJfB/500}$ | — | — | 0.37 | UI p-p | 1 |
| Total jitter $f_{C3dB} = f_{BAUD} \div 1667$ | $U_{SATA\_TXTJfB/1667}$ | — | — | 0.55 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$ | $U_{SATA\_TXDJfB/10}$ | — | — | 0.17 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$ | $U_{SATA\_TXDJfB/500}$ | — | — | 0.19 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$ | $U_{SATA\_TXDJfB/1667}$ | — | — | 0.35 | UI p-p | 1 |

**Note:**
1. Measured at Tx output pins peak-to-peak phase variation, random data pattern

## 2.20.7.4 AC Differential Receiver Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

**Table 85. Gen 1i/1.5G Receiver (Rx) AC Specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | $T_{UI}$ | 666.4333 | 666.6667 | 670.2333 | ps | — |
| Total jitter data-data 5 UI | $U_{SATA\_TXTJ5UI}$ | — | — | 0.43 | UI p-p | 1 |
| Total jitter, data-data 250 UI | $U_{SATA\_TXTJ250UI}$ | — | — | 0.60 | UI p-p | 1 |
| Deterministic jitter, data-data 5 UI | $U_{SATA\_TXDJ5UI}$ | — | — | 0.25 | UI p-p | 1 |
| Deterministic jitter, data-data 250 UI | $U_{SATA\_TXDJ250UI}$ | — | — | 0.35 | UI p-p | 1 |

**Note:**
1. Measured at receiver.

**Table 89. SGMII DC Receiver Electrical Characteristics ($XV_{DD}$ = 1.5 V or 1.8 V) (continued)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|

**Note:**
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 2.20.4.4, "PCI Express DC Physical Layer Receiver Specifications," and Section 2.20.4.5.2, "PCI Express AC Physical Layer Receiver Specifications," for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1–3)GCR(lane)1[REIDL_CTL] bit field.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

**Table 90. SGMII 2.5x Receiver DC Timing Specifications ($XV_{DD}$ = 1.5 V or 1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential input voltage | $V_{IN}$ | 200 | 900 | 1600 | mV p-p | 1 |

**Note:**
1. Measured at the receiver.

## 2.20.8.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

### 2.20.8.2.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

**Table 91. SGMII Transmit AC Timing Specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Deterministic jitter | JD | — | — | 0.17 | UI p-p | — |
| Total jitter | JT | — | — | 0.35 | UI p-p | 1 |
| Unit interval: 1.25 GBaud | UI | 800 – 100 ppm | 800 | 800 + 100 ppm | ps | — |
| Unit interval: 3.125 GBaud | UI | 320 – 100 ppm | 320 | 320 + 100 ppm | ps | — |
| AC coupling capacitor | $C_{TX}$ | 10 | | 200 | nF | 2 |

**Note:**
1. See Figure 42 for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

### 2.20.8.2.2 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$) respectively, as depicted in this figure.

to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide, and direct.

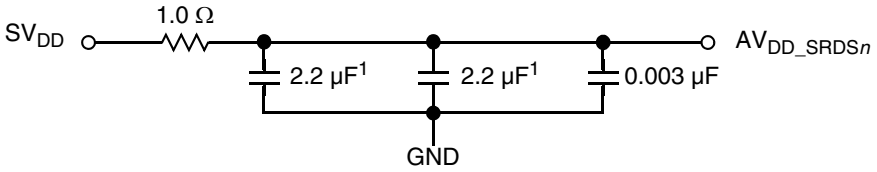



**Figure 51. SerDes PLL Power Supply Filter Circuit**

Note the following:

- $AV_{DD\_SRDSn}$ must be a filtered version of $SV_{DD}$.
- Signals on the SerDes interface are fed from the $XV_{DD}$ power plane.
- Voltage for $AV_{DD\_SRDSn}$ is defined at the PLL supply filter and not the pin of $AV_{DD\_SRDSn}$.
- A 0805 sized capacitor is recommended for system initial bring-up.

## 3.3.2 $XV_{DD}$ Power Supply Filtering

$XV_{DD}$ may be supplied by a linear regulator or sourced by a filtered $GV_{DD}$. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for $XV_{DD}$ filtering, where $XV_{DD}$ is sourced from $GV_{DD}$, is illustrated in Figure 52. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

C2 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

F1 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

F2 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

Bulk and decoupling capacitors are added, as needed, per power supply design.

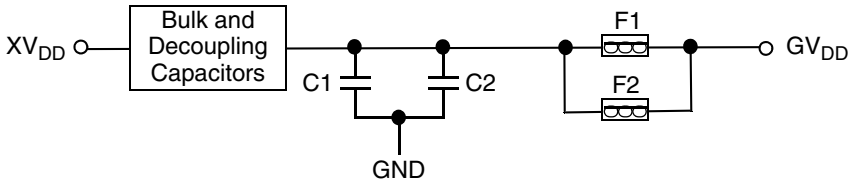



**Figure 52. $XV_{DD}$ Power Supply Filter Circuit**

## 3.3.3 $USB\_V_{DD}\_1P0$ Power Supply Filtering

$USB\_V_{DD}\_1P0$ must be sourced by a filtered $V_{DD\_CA\_CB\_PL}$ using a star connection. An example solution for $USB\_V_{DD}\_1P0$ filtering, where $USB\_V_{DD}\_1P0$ is sourced from $V_{DD\_CA\_CB\_PL}$, is illustrated in Figure 53. The component values in this example filter is system dependent and are still under characterization; component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 µF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)

F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)

Bulk and decoupling capacitors are added, as needed, per power supply design.

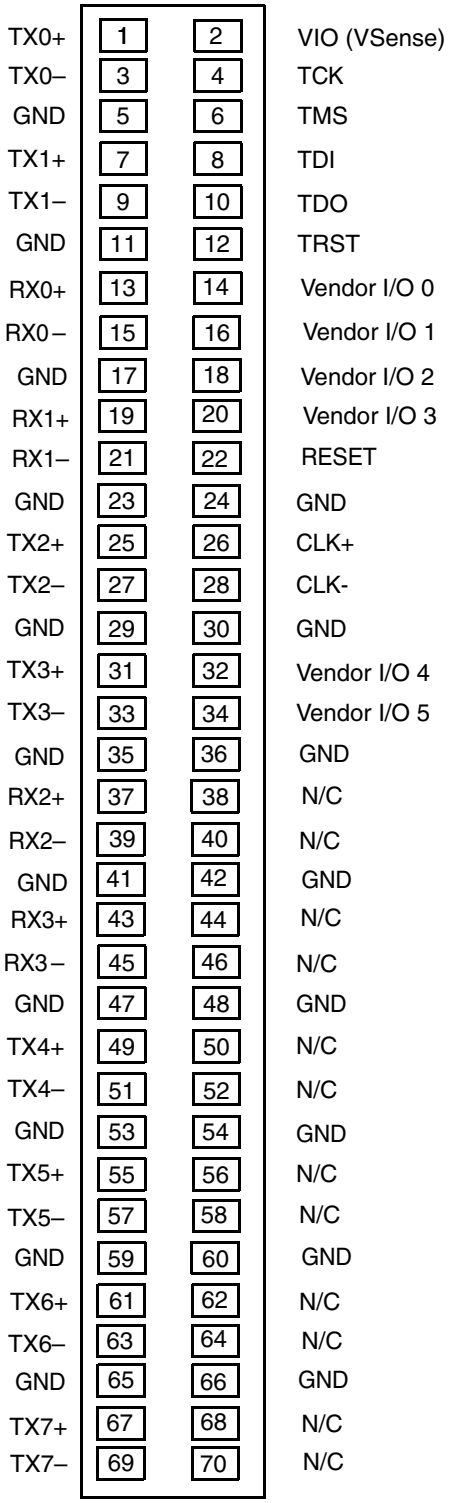



**Figure 57. Aurora 70 Pin Connector Duplex Pinout**

## 3.6.3 Guidelines for High-Speed Interface Termination

This section provides the guidelines for when the SerDes interface is either entirely unused or partly unused.

### 3.6.3.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[7:2], SD_TX[13:10]
- $\overline{\text{SD\_TX}}$[7:2], $\overline{\text{SD\_TX}}$[13:10]
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[7:2], SD_RX[13:10]
- $\overline{\text{SD\_RX}}$[13:10], $\overline{\text{SD\_RX}}$[13:10]
- SD_REF_CLK1, SD_REF_CLK2
- $\overline{\text{SD\_REF\_CLK1}}$, $\overline{\text{SD\_REF\_CLK2}}$

In the RCW configuration fields SRDS_LPD_B1 and SRDS_LPD_B2, all bits must be set to power down all the lanes in each bank.

RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN] = 0 power-downs the PLLs of both banks.

Additionally, software may configure SRDSB*n*RSTCTL[SDRD] = 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both $SV_{DD}$ and $XV_{DD}$ must remain powered.

### 3.6.3.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following unused pins must be left unconnected:

- SD_TX[*n*]
- $\overline{\text{SD\_TX}}$[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*]
- $\overline{\text{SD\_RX}}$[*n*]
- SD_REF_CLK1, $\overline{\text{SD\_REF\_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD\_REF\_CLK2}}$ (If entire SerDes bank 2 unused)

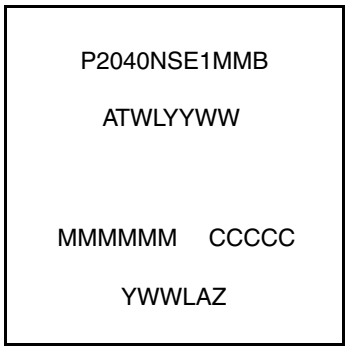
In the RCW configuration field for each bank SRDS_LPD_B*n* with unused lanes, the respective bit for each unused lane must be set to power down the lane.

## 3.6.4 USB Controller Connections

This section details the hardware connections required for the USB controllers.

### 6.2.1 Part Marking

Parts are marked as in the example shown in this figure.




FC-PBGA

**Notes:**

P2040NSE1MMB is the orderable part number. See Table 107 for details.

ATWLYYWW is the test traceability code.
MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

**Figure 64. Part Marking for FC-PBGA Device**

# 7 Revision History

This table provides a revision history for this document.

**Table 108. Revision History**

| Rev. Number | Date | Description |
|---|---|---|
| 2 | 02/2013 | • In Table 7, “P2040 I/O Power Supply Estimated Values,” updated the USB power supply with USB_Vdd_3P3 and updated the typical value with “0.003” in the Others (Reset, System Clock, JTAG & Misc.) row.<br>• In Table 8, “Device AVDD Power Dissipation,” removed $V_{DD\_LP}$ from table.<br>• Added Table 10, “VDD_LP Power Dissipation.”<br>• In Table 53, “MPIC Input AC Timing Specifications,” added Trust inputs AC timing and footnote 2.<br>• In Table 93, “Processor Clocking Specifications,” updated footnote 8 with Rev 1.1 silicon.<br>• In Table 107, “Part Numbering Nomenclature,” added “C” in the Die Revision collumn.<br>• In Section 6.2, “Orderable Part Numbers Addressed by this Document,” added the device part numbers for Rev 2.0 silicon. |