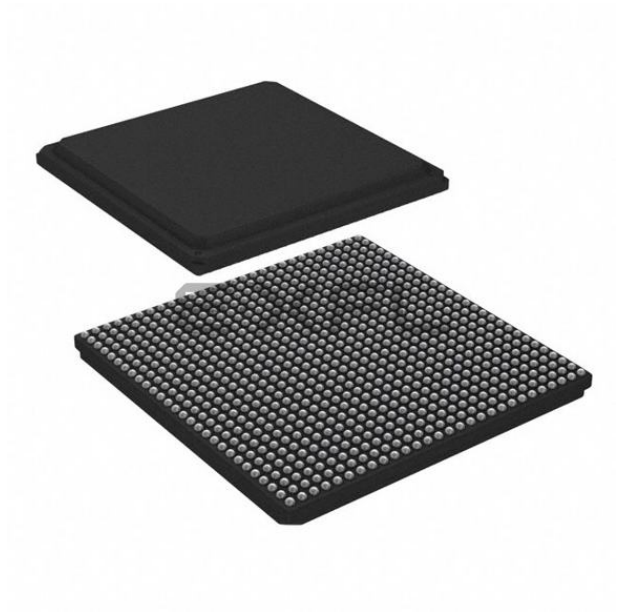

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Security; SEC 4.2
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator, Secure Fusebox
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2041nse7mmc

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MDQS5}}$	Data Strobe	AH24	I/O	GV_{DD}	—
$\overline{\text{MDQS6}}$	Data Strobe	AE22	I/O	GV_{DD}	—
$\overline{\text{MDQS7}}$	Data Strobe	AF28	I/O	GV_{DD}	—
$\overline{\text{MDQS8}}$	Data Strobe	AG3	I/O	GV_{DD}	—
MBA0	Bank Select	AC16	O	GV_{DD}	—
MBA1	Bank Select	AC15	O	GV_{DD}	—
MBA2	Bank Select	AC8	O	GV_{DD}	—
MA00	Address	AG16	O	GV_{DD}	—
MA01	Address	AF12	O	GV_{DD}	—
MA02	Address	AC12	O	GV_{DD}	—
MA03	Address	AH11	O	GV_{DD}	—
MA04	Address	AG11	O	GV_{DD}	—
MA05	Address	AH10	O	GV_{DD}	—
MA06	Address	AC11	O	GV_{DD}	—
MA07	Address	AC10	O	GV_{DD}	—
MA08	Address	AF10	O	GV_{DD}	—
MA09	Address	AH9	O	GV_{DD}	—
MA10	Address	AH16	O	GV_{DD}	—
MA11	Address	AG9	O	GV_{DD}	—
MA12	Address	AC9	O	GV_{DD}	—
MA13	Address	AH20	O	GV_{DD}	—
MA14	Address	AG8	O	GV_{DD}	—
MA15	Address	AH7	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	AH18	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	AH17	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	AH19	O	GV_{DD}	—
$\overline{\text{MCS0}}$	Chip Select	AC18	O	GV_{DD}	—
$\overline{\text{MCS1}}$	Chip Select	AC21	O	GV_{DD}	—
$\overline{\text{MCS2}}$	Chip Select	AG17	O	GV_{DD}	—
$\overline{\text{MCS3}}$	Chip Select	AG20	O	GV_{DD}	—
MCKE0	Clock Enable	AB8	O	GV_{DD}	—
MCKE1	Clock Enable	AB7	O	GV_{DD}	—
MCKE2	Clock Enable	AH6	O	GV_{DD}	—
MCKE3	Clock Enable	AG6	O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_RX04	Receive Data (positive)	A2	I	XV_{DD}	—
SD_RX03	Receive Data (positive)	E1	I	XV_{DD}	—
SD_RX02	Receive Data (positive)	G1	I	XV_{DD}	—
$\overline{\text{SD\_RX13}}$	Receive Data (negative)	A21	I	XV_{DD}	—
$\overline{\text{SD\_RX12}}$	Receive Data (negative)	A19	I	XV_{DD}	—
$\overline{\text{SD\_RX11}}$	Receive Data (negative)	A15	I	XV_{DD}	—
$\overline{\text{SD\_RX10}}$	Receive Data (negative)	B13	I	XV_{DD}	—
$\overline{\text{SD\_RX07}}$	Receive Data (negative)	A11	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive Data (negative)	A9	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive Data (negative)	A7	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive Data (negative)	A3	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive Data (negative)	E2	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive Data (negative)	G2	I	XV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	D3	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes Bank 1 PLL Reference Clock Complement	D4	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	E17	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes Bank 2 PLL Reference Clock Complement	F17	I	XV_{DD}	—
General-Purpose Input/Output					
GPIO00/$\overline{\text{SPI\_CS0}}$/SDHC_DATA4	General Purpose Input/Output	H26	I/O	CV_{DD}	—
GPIO01/$\overline{\text{SPI\_CS1}}$/SDHC_DATA5	General Purpose Input/Output	H23	I/O	CV_{DD}	—
GPIO02/$\overline{\text{SPI\_CS2}}$/SDHC_DATA6	General Purpose Input/Output	H27	I/O	CV_{DD}	—
GPIO03$\overline{\text{SPI_CS3}}$/SDHC_DATA7	General Purpose Input/Output	H24	I/O	CV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input/Output	R23	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input/Output	P26	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input/Output	R26	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input/Output	P27	I/O	OV_{DD}	—
GPIO12/$\overline{\text{UART1\_RTS}}$/UART3_SOUT	General Purpose Input/Output	P24	I/O	OV_{DD}	—
GPIO13/$\overline{\text{UART2\_RTS}}$/UART4_SOUT	General Purpose Input/Output	P25	I/O	OV_{DD}	—
GPIO14/$\overline{\text{UART1\_CTS}}$/UART3_SIN	General Purpose Input/Output	R25	I/O	OV_{DD}	—
GPIO15/$\overline{\text{UART2\_CTS}}$/UART4_SIN	General Purpose Input/Output	P23	I/O	OV_{DD}	—
GPIO16/IIC3_SCL/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/$\overline{\text{SDHC\_CD}}$	General Purpose Input/Output	AB23	I/O	OV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND132	Ground	K12	—	—	—
GND131	Ground	K14	—	—	—
GND130	Ground	K16	—	—	—
GND129	Ground	K18	—	—	—
GND128	Ground	K21	—	—	—
GND127	Ground	L8	—	—	—
GND126	Ground	L10	—	—	—
GND125	Ground	L12	—	—	—
GND124	Ground	L14	—	—	—
GND123	Ground	L16	—	—	—
GND122	Ground	L18	—	—	—
GND121	Ground	M2	—	—	—
GND120	Ground	M5	—	—	—
GND119	Ground	M8	—	—	—
GND118	Ground	M10	—	—	—
GND117	Ground	M12	—	—	—
GND116	Ground	M14	—	—	—
GND115	Ground	M16	—	—	—
GND114	Ground	M18	—	—	—
GND113	Ground	N8	—	—	—
GND112	Ground	N10	—	—	—
GND111	Ground	N12	—	—	—
GND110	Ground	N14	—	—	—
GND109	Ground	N16	—	—	—
GND108	Ground	N18	—	—	—
GND107	Ground	N21	—	—	—
GND106	Ground	N25	—	—	—
GND105	Ground	P5	—	—	—
GND104	Ground	P8	—	—	—
GND103	Ground	P10	—	—	—
GND102	Ground	P12	—	—	—
GND101	Ground	P14	—	—	—
GND100	Ground	P16	—	—	—
GND099	Ground	P18	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
USB1_AGND01	USB1 PHY Transceiver GND	M28	—	—	—
USB2_AGND06	USB2 PHY Transceiver GND	J22	—	—	—
USB2_AGND05	USB2 PHY Transceiver GND	J24	—	—	—
USB2_AGND04	USB2 PHY Transceiver GND	J26	—	—	—
USB2_AGND03	USB2 PHY Transceiver GND	K25	—	—	—
USB2_AGND02	USB2 PHY Transceiver GND	L25	—	—	—
USB2_AGND01	USB2 PHY Transceiver GND	M26	—	—	—
OVDD06	General I/O Supply	N20	—	OV_{DD}	—
OVDD05	General I/O Supply	P20	—	OV_{DD}	—
OVDD04	General I/O Supply	R20	—	OV_{DD}	—
OVDD03	General I/O Supply	T20	—	OV_{DD}	—
OVDD02	General I/O Supply	T26	—	OV_{DD}	—
OVDD01	General I/O Supply	W26	—	OV_{DD}	—
CVDD2	eSPI and eSDHC Supply	K20	—	CV_{DD}	—
CVDD1	eSPI and eSDHC Supply	M20	—	CV_{DD}	—
GVDD17	DDR Supply	AA8	—	GV_{DD}	—
GVDD16	DDR Supply	AA9	—	GV_{DD}	—
GVDD15	DDR Supply	AA10	—	GV_{DD}	—
GVDD14	DDR Supply	AA11	—	GV_{DD}	—
GVDD13	DDR Supply	AA12	—	GV_{DD}	—
GVDD12	DDR Supply	AA13	—	GV_{DD}	—
GVDD11	DDR Supply	AA14	—	GV_{DD}	—
GVDD10	DDR Supply	AA15	—	GV_{DD}	—
GVDD09	DDR Supply	AB13	—	GV_{DD}	—
GVDD08	DDR Supply	AB14	—	GV_{DD}	—
GVDD07	DDR Supply	AC13	—	GV_{DD}	—
GVDD06	DDR Supply	AC14	—	GV_{DD}	—
GVDD05	DDR Supply	AF6	—	GV_{DD}	—
GVDD04	DDR Supply	AF9	—	GV_{DD}	—
GVDD03	DDR Supply	AF17	—	GV_{DD}	—
GVDD02	DDR Supply	AF20	—	GV_{DD}	—
GVDD01	DDR Supply	AF23	—	GV_{DD}	—
BVDD07	Local Bus Supply	J7	—	BV_{DD}	—
BVDD06	Local Bus Supply	K7	—	BV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_CA_PL16	Core Group A and Platform Supply	U13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL15	Core Group A and Platform Supply	U15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL14	Core Group A and Platform Supply	U20	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL13	Core Group A and Platform Supply	V9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL12	Core Group A and Platform Supply	V11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL11	Core Group A and Platform Supply	V13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL10	Core Group A and Platform Supply	V15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL09	Core Group A and Platform Supply	W9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL08	Core Group A and Platform Supply	W11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL07	Core Group A and Platform Supply	W13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL06	Core Group A and Platform Supply	W15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL05	Core Group A and Platform Supply	Y9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL04	Core Group A and Platform Supply	Y11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL03	Core Group A and Platform Supply	Y13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL02	Core Group A and Platform Supply	Y15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL01	Core Group A and Platform Supply	AA21	—	$V_{DD\_CA\_PL}$	37
VDD_CB11	Core Group B Supply	U16	—	V_{DD_CB}	37
VDD_CB10	Core Group B Supply	U18	—	V_{DD_CB}	37
VDD_CB09	Core Group B Supply	V18	—	V_{DD_CB}	37
VDD_CB08	Core Group B Supply	V20	—	V_{DD_CB}	37
VDD_CB07	Core Group B Supply	W16	—	V_{DD_CB}	37
VDD_CB06	Core Group B Supply	W18	—	V_{DD_CB}	37
VDD_CB05	Core Group B Supply	W20	—	V_{DD_CB}	37
VDD_CB04	Core Group B Supply	Y18	—	V_{DD_CB}	37
VDD_CB03	Core Group B Supply	Y20	—	V_{DD_CB}	37
VDD_CB02	Core Group B Supply	AA18	—	V_{DD_CB}	37
VDD_CB01	Core Group B Supply	AA20	—	V_{DD_CB}	37
VDD_LP	Low Power Security Monitor Supply	L20	—	V_{DD_LP}	25
AVDD_CC1	Core Cluster PLL1 Supply	V7	—	—	13
AVDD_CC2	Core Cluster PLL2 Supply	W22	—	—	13
AVDD_PLAT	Platform PLL Supply	V22	—	—	13
AVDD_DDR	DDR PLL Supply	W6	—	—	13
AVDD_SRDS1	SerDes PLL1 Supply	C1	—	—	13
AVDD_SRDS2	SerDes PLL2 Supply	A17	—	—	13

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note

26. For reduced core (core 2 and 3 disabled) mode, this signal must be pulled high (100 Ω–1 kΩ) to OVDD.
27. Warning, incorrect voltage select settings can lead to irreversible device damage. This pin has an internal 2 kΩ pull-down resistor, to pull it high, a pull-up resistor of less than 1 kΩ to OVDD should be used. See Section 3.2, "Supply Power Default Setting."
28. SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
29. The *cfg_xvdd_sel* (LA[26]) reset configuration pin must select the correct voltage that is being supplied on the XVDD pin. Incorrect voltage select settings can lead to irreversible device damage.
30. See Section 2.2, "Power Up Sequencing," and Section 5, "Security Fuse Processor," for additional details on this signal.
31. Pin must NOT be pulled down during power-on reset.
32. This pin must be connected to GND through a 10 kΩ ± 0.1% resistor for bias generation.
33. A 1μF to 1.5 μF capacitor connected to GND is required on this signal. Section 3.6.4.2, "USBn_V_{DD}_1P8_DECAP Capacitor Options," provides a list of recommended capacitors.
34. A divider network is required on this signal. See Section 3.6.4.1, "USB Divider Network."
35. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal machine operation.
36. For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull-up on LGPL4 is required.
37. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but they are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section describes the ratings, conditions, and other electrical characteristics.

2.1.1 Absolute Maximum Ratings

Table 2. Absolute Operating Conditions[1]

Parameter	Symbol	Max Value	Unit	Note
Core Group A (cores 0–1) and platform supply voltage (Silicon Rev 1.0)	$V_{DD\_CA\_PL}$	–0.3 to 1.1	V	9, 10
Core Group B (cores 2–3) supply voltage (Silicon Rev 1.0)	V_{DD_CB}	–0.3 to 1.1	V	9, 10
Core Group A (cores 0–1), Core Group B (cores 2–3) and platform supply voltage (Silicon Rev 1.1)	$V_{DD\_CA\_CB\_PL}$	–0.3 to 1.1	V	9, 10
PLL supply voltage (core, platform, DDR)	AV_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (SerDes, filtered from SV_{DD})	AV_{DD_SRDS}	–0.3 to 1.1	V	—
Fuse programming override supply	POV_{DD}	–0.3 to 1.65	V	1
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—

While VDD is ramping, current may be supplied from VDD through the chip to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

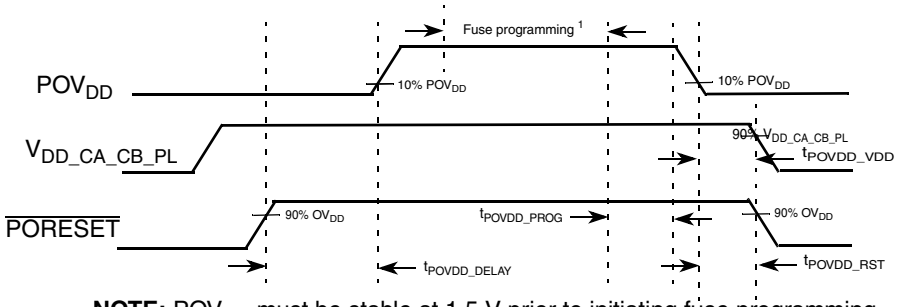
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to $V_{DD\_CA\_CB\_PL}$ ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before $V_{DD\_CA\_CB\_PL}$ is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{PORESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{PORESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

Table 6. Device Power Dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	667	534	1067	467	1.0	65	8.7	—	8.2	—	—	2, 3
Thermal						105	12.0	—	11.8	—	—	5, 7
Maximum							12.3	11.1	11.9	10.6	1.4	4, 6, 7

Note:

1. Combined power of $V_{DD\_CA\_CB\_PL}$, SVDD with the DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P2040 I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.705	1.764	W	1,2,5,6
	800 MT/s data rate		0.714	1.785		
	1066 MT/s data rate		0.731	1.827		
	1200 MT/s data rate		0.739	1.848		
	1333 MT/s data rate		0.747	1.869		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1, 7
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC Per Controller	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the device PLLs, at allowable voltage levels.

Table 8. Device AV_{DD} Power Dissipation

AV_{DD}s	Typical	Maximum	Unit	Note
AV_{DD_DDR}	5	15	mW	1
AV_{DD_CC1}				
AV_{DD_CC2}				
AV_{DD_PLAT}				
AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}				
USB_V_{DD_1P0}	—	10	mW	3

Note:

1. $V_{DD\_CA\_CB\_PL}$, T_A = 80°C, T_J = 105°C
2. SV_{DD} = 1.0 V, T_A = 80°C, T_J = 105°C
3. USB_V_{DD_1P0} = 1.0V, T_A = 80°C, T_J = 105°C

This table shows the estimated power dissipation on the POV_{DD} supply for the chip at allowable voltage levels.

Table 9. POV_{DD} Power Dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the device, at allowable voltage levels.

Table 10. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Notes
V_{DD_LP} (Device on, 105C)	1.5	mW	1
V_{DD_LP} (Device off, 70C)	195	uW	2
V_{DD_LP} (Device off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When the device is off, V_{DD_LP} may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC, which switches V_{DD_LP} to battery when the SoC is powered down. See the Trust Architecture chapter in the device reference manual for more information.

2.5 Thermal

Table 11. Package Thermal Characteristics [6]

Rating	Board	Symbol	Value	Unit	Note
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	21	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	15	°C/W	1, 3

2.9.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	1, 2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed the $MV_{REF}n$ DC level by more than ±1% of the DC value (that is, ±15mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $MV_{REF}n$ with a min value of $MV_{REF}n$ – 0.04 and a max value of $MV_{REF}n$ + 0.04. V_{TT} should track variations in the DC level of $MV_{REF}n$.
4. The voltage regulator for $MV_{REF}n$ must meet the specifications stated in Table 23.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.35 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	1, 2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.090	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.8	mA	7, 8
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.8	—	mA	7, 8

This figure represents the AC timing from Table 33 in master mode (internal clock). Note that although timing specifications generally refer to the rising edge of the clock, this figure also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

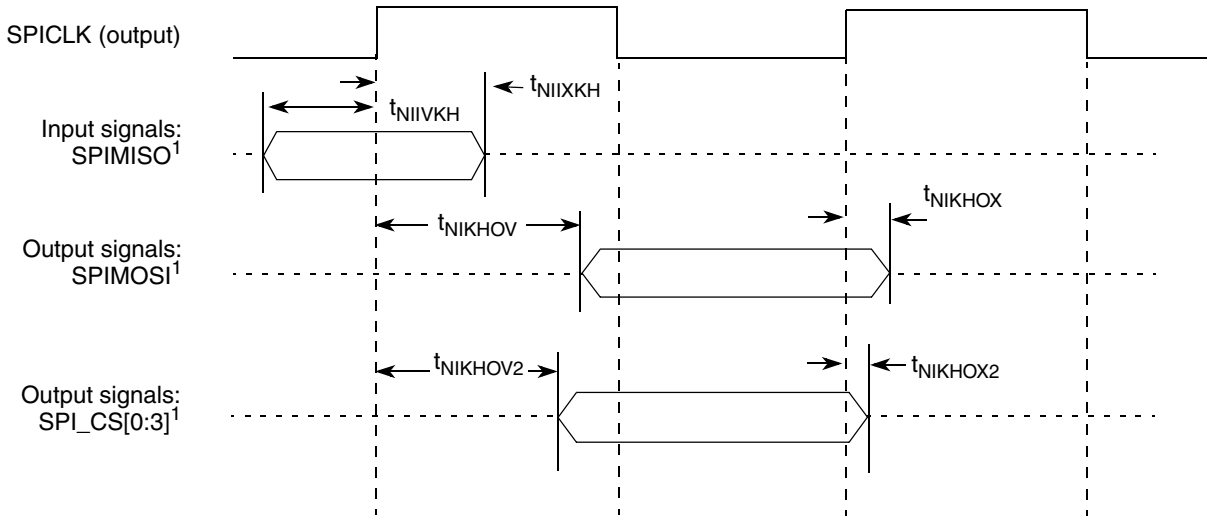


Figure 15. eSPI AC Timing in Master Mode (Internal Clock) Diagram

2.11 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.11.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 34. DUART DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). This figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

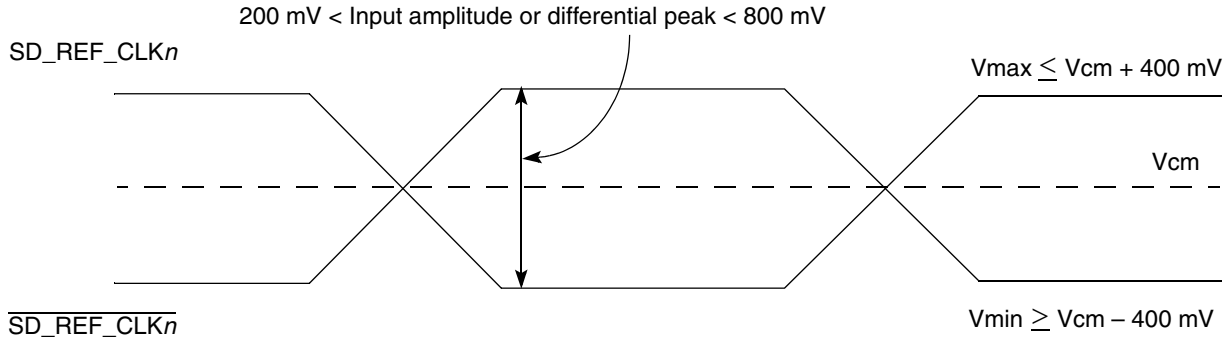


Figure 35. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SD_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}n}$ either left unconnected or tied to ground.
  — The SD_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}n}$) through the same source impedance as the clock input (SD_REF_CLK*n*) in use.

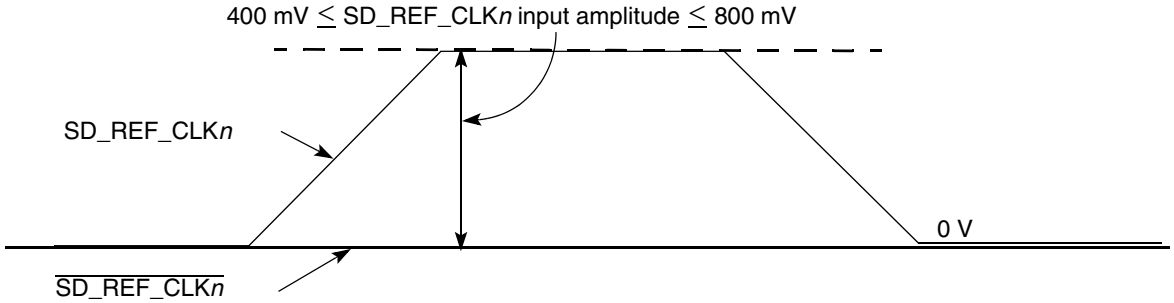


Figure 36. Single-Ended Reference Clock Input DC Requirements

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.20.5.1 Signal Definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. This figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$—each have a peak-to-peak swing of A – B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

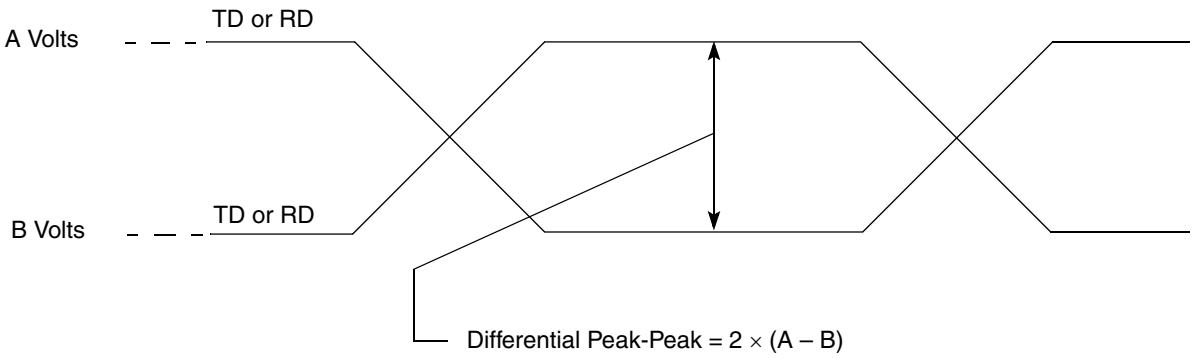


Figure 41. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.20.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.

- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.20.5.3 Serial RapidIO Clocking Requirements for SD_REF_CLK*n* and SD_REF_CLK*n*

SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for various SerDes Serial RapidIO configurations based on the RCW configuration field SRDS_PRTCL. Serial RapidIO is not supported on SerDes banks 2.

For more information on these specifications, see Section 2.20.2, "SerDes Reference Clocks."

2.20.5.4 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.20.5.4.1 DC Serial RapidIO Timing Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud and XX ps at 5 GBaud.

This table defines the transmitter DC specifications for Serial RapidIO operating at XV_{DD} = 1.5 V or 1.8 V.

Table 70. Serial RapidIO Transmitter DC Timing Specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output voltage	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.20.5.4.2 DC Serial RapidIO Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

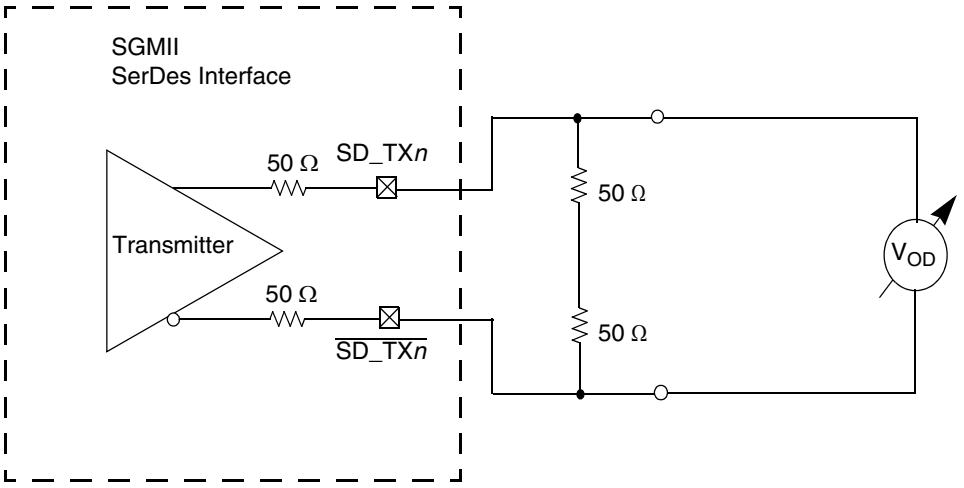


Figure 45. SGMII Transmitter DC Measurement Circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 88. SGMII 2.5x Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Output voltage	V_O	–0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—

Note:
1. Absolute output voltage limit

2.20.8.1.2 SGMII DC Receiver Electrical Characteristics

This table lists the SGMII DC receiver electrical characteristics for 1.25 GBaud. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 89. SGMII DC Receiver Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Typ	Max	Unit	Note
DC Input voltage range		—		N/A		—	1
Input differential voltage	REIDL_CTL = 001xx	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	REIDL_CTL = 100xx		175	—			
Loss of signal threshold	REIDL_CTL = 001xx	V_{LOS}	30	—	100	mV	3, 4
	REIDL_CTL = 100xx		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

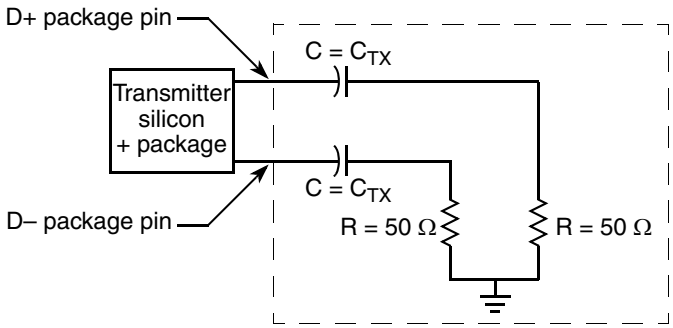


Figure 46. SGMII AC Test/Measurement Load

2.20.8.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 92. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Note:
1. Measured at receiver
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 System Clocking

This section describes the PLL configuration of the device.

This device includes six PLLs, as follows:

- There are two selectable core cluster PLLs that generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL; core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3,

3.6.2 Aurora Configuration Signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in Figure 56 and Figure 57. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Freescale recommends that the Aurora 22 pin duplex connector be designed into the system as shown in Figure 58 or the 70 pin duplex connector be designed into the system as shown in Figure 59.

If the Aurora interface is not used, Freescale recommends the legacy COP header be designed into the system as described in Section 3.6.1.1, "Termination of Unused Signals."

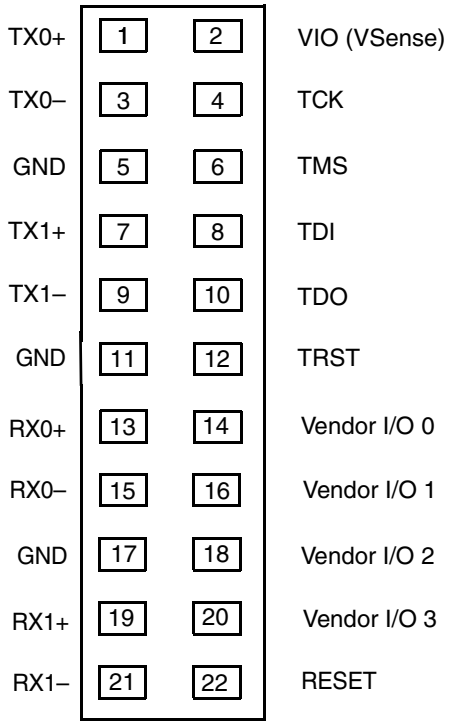


Figure 56. Aurora 22 Pin Connector Duplex Pinout

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.8.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 61).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.8.3 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

- Operating range: 10 – 230µA
- Ideality factor over 13.5 – 220 µA: n = 1.00589 ± 0.008

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm × 23 mm, 780 flip chip plastic ball grid array (FC-PBGA).

Package outline	23 mm × 23mm
Interconnects	780
Ball Pitch	0.8 mm
Ball Diameter (typical)	0.40 mm
Solder Balls	96.5% Sn, 3% Ag, 0.5% Cu
Module height (typical)	2.21 mm to 2.51 mm (Maximum)

Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
P2040NSE1FLB P2040NSE7FLC	P	2	04 = 4 core	1	N = Industrial qualification	S = Std temp	E = SEC present	1= FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	F = 667 MHz	L = 1067 MT/s	B C
P2040NSN1FLB P2040NSN7FLC							N = SEC not present				
P2040NSE1HLB P2040NSE7HLC							E = SEC present		H = 800 MHz		
P2040NSN1HLB P2040NSN7HLC							N = SEC not present				
P2040NSE1KLB P2040NSE7KLC							E = SEC Present		K = 1000 MHz		
P2040NSN1KLB P2040NSN7KLC							N = SEC not present				
P2040NSE1MMB P2040NSE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NSN1MMB P2040NSN7MMC							N = SEC not present				
P2040NXE1FLB P2040NXE7FLC						X = Extended temp	E = SEC Present		F = 667 MHz	L = 1067 MT/s	
P2040NXN1FLB P2040NXN7FLC							N = SEC not present				
P2040NXE1MMB P2040NXE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NXN1MMB P2040NXN7MMC							N = SEC not present				

Table 108. Revision History (continued)

Rev. Number	Date	Description
1	09/2012	• In Table 1, “Pin List by Bus”, added note for pin V_{DD_LP} • Updated Table 8, “Device AVDD Power Dissipation”. • In Table 12, “SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V)”, updated the input current max value and added input capacitance max value. • In Table 51, “eSDHC AC Timing Specifications”, updated input setup times from 5 ns to 2.5 ns. • In Section 3.1.6.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces”, updated the note that the “PCI Express link width” refers to “a single port”. • In Section 4.1, “Package Parameters for the FC-PBGA”, updated the solder ball composition and module height. • In Section 4.2, “Mechanical Dimensions of the FC-PBGA”, updated the figure for the mechanical dimensions. • In Section 3.6, “Connection Recommendations”, removed the sentence “If no aspect of Trust Architecture is to be used, all Trust Architecture pins can be tied to GND.”
0	06/2012	Initial public release