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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2041nsn7mmc

1.1 780 FC-PBGA Ball Layout Diagrams

These figures show the FC-PBGA ball map diagrams.

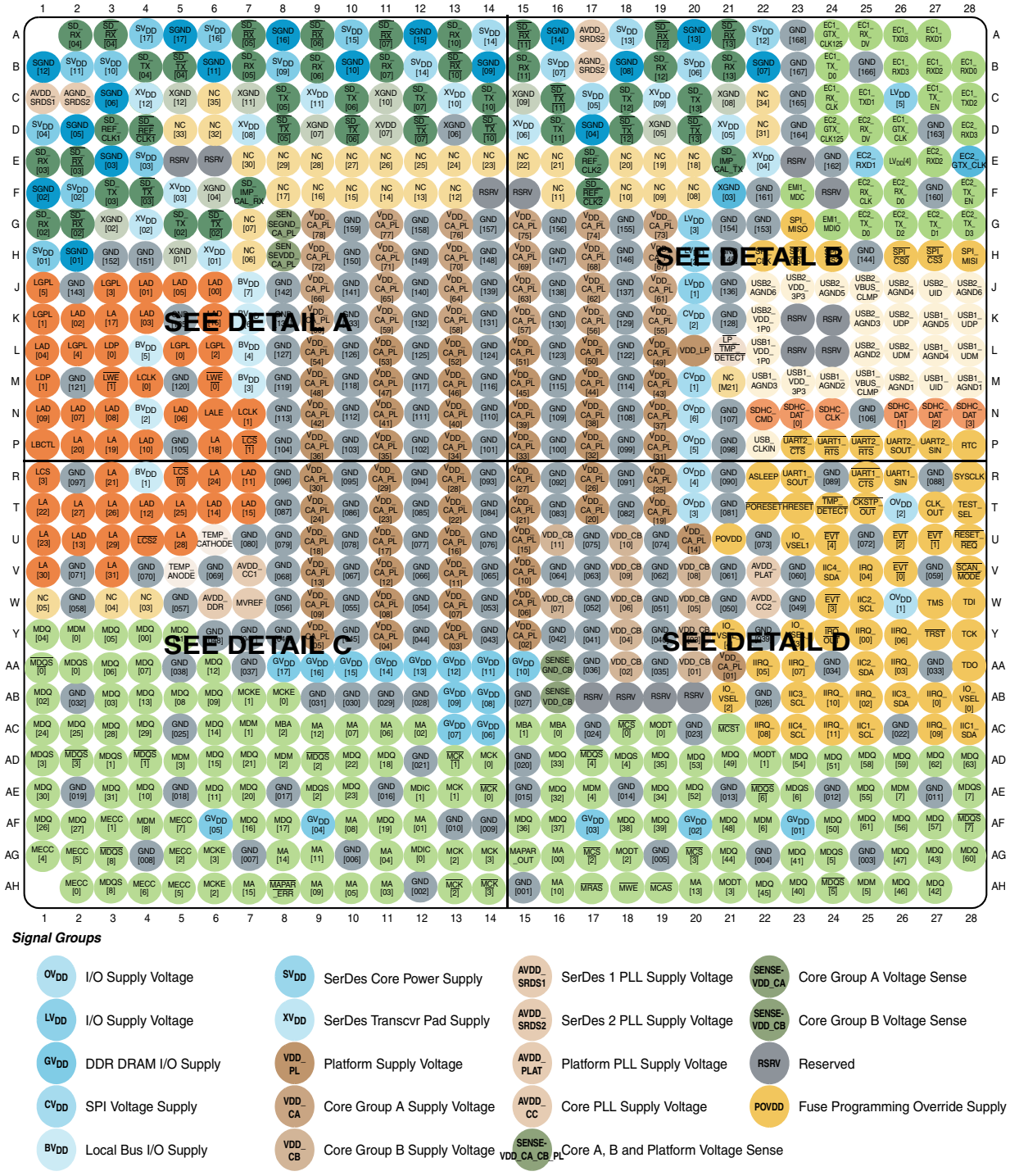

Figure 2. 780 BGA Ball Map Diagram (Top View)

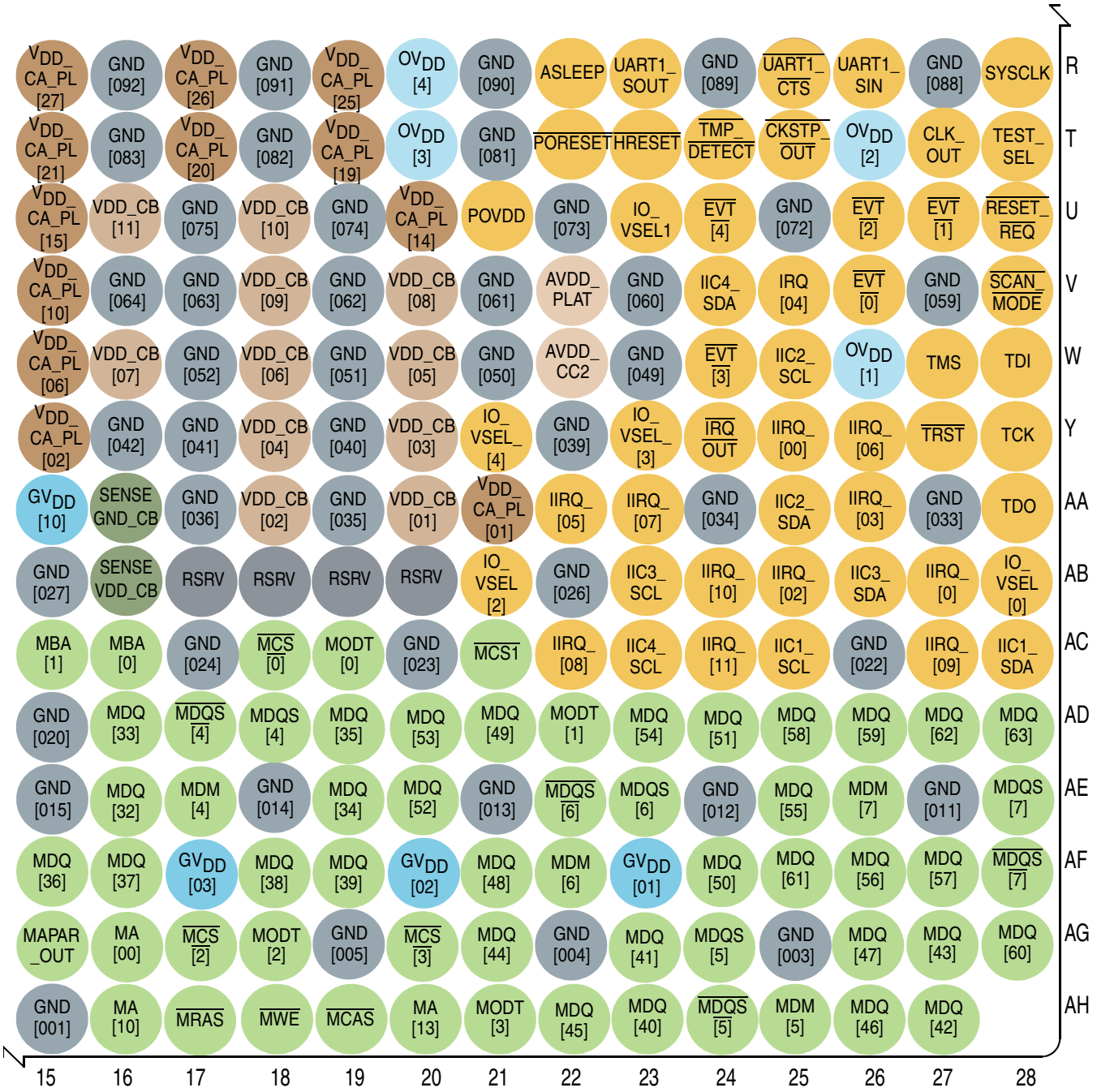

Figure 6. 780 BGA Ball Map Diagram (Detail View D)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LA19	Address	P3	I/O	BV_{DD}	31
LA20	Address	P2	I/O	BV_{DD}	31
LA21	Address	R3	I/O	BV_{DD}	31
LA22	Address	T1	I/O	BV_{DD}	31
LA23	Address	U1	I/O	BV_{DD}	3
LA24	Address	R6	I/O	BV_{DD}	3
LA25	Address	T5	I/O	BV_{DD}	31
LA26	Address	T3	I/O	BV_{DD}	3, 29
LA27	Address	T2	O	BV_{DD}	—
LA28	Address	U5	I/O	BV_{DD}	—
LA29	Address	U3	I/O	BV_{DD}	—
LA30	Address	V1	I/O	BV_{DD}	—
LA31	Address	V3	I/O	BV_{DD}	—
LDP0	Data Parity	L3	I/O	BV_{DD}	—
LDP1	Data Parity	M1	I/O	BV_{DD}	—
$\overline{\text{LCS0}}$	Chip Selects	R5	O	BV_{DD}	5
$\overline{\text{LCS1}}$	Chip Selects	P7	O	BV_{DD}	5
$\overline{\text{LCS2}}$	Chip Selects	U4	O	BV_{DD}	5
$\overline{\text{LCS3}}$	Chip Selects	R1	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write Enable	M6	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write Enable	M3	O	BV_{DD}	—
LBCTL	Buffer Control	P1	O	BV_{DD}	—
LALE	Address Latch Enable	N6	I/O	BV_{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	L5	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	K1	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	L6	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose LIne 3/ LFWP_B—FCM	J3	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	L2	I/O	BV_{DD}	36
LGPL5	UPM General Purpose Line 5 / Amux	J1	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	M4	O	BV_{DD}	—
LCLK1	Local Bus Clock	N7	O	BV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IRQ05/GPIO23/DMA2_DDONE0	External Interrupts	AA22	I	OV_{DD}	24
IRQ06/GPIO24/USB1_DRVVBUS	External Interrupts	Y26	I	OV_{DD}	24
IRQ07/GPIO25/USB1_PWRFAULT	External Interrupts	AA23	I	OV_{DD}	24
IRQ08/GPIO26/USB2_DRVVBUS	External Interrupts	AC22	I	OV_{DD}	24
IRQ09/GPIO27/USB2_PWRFAULT	External Interrupts	AC27	I	OV_{DD}	24
IRQ10/GPIO28/EVT7	External Interrupts	AB24	I	OV_{DD}	24
IRQ11/GPIO29/EVT8	External Interrupts	AC24	I	OV_{DD}	24
IRQ_OUT/EVT9	Interrupt Output	Y24	O	OV_{DD}	1, 2, 24
Trust					
TMP_DETECT	Tamper Detect	T24	I	OV_{DD}	25
LP_TMP_DETECT	Low Power Tamper Detect	L21	I	V_{DD_LP}	25
eSDHC					
SDHC_CMD	Command/Response	N22	I/O	CV_{DD}	—
SDHC_DAT0	Data	N23	I/O	CV_{DD}	—
SDHC_DAT1	Data	N26	I/O	CV_{DD}	—
SDHC_DAT2	Data	N27	I/O	CV_{DD}	—
SDHC_DAT3	Data	N28	I/O	CV_{DD}	—
SDHC_DAT4/SPI_CS0/GPIO00	Data	H26	I/O	CV_{DD}	24, 28
SDHC_DAT5/SPI_CS1/GPIO01	Data	H23	I/O	CV_{DD}	24, 28
SDHC_DAT6/SPI_CS2/GPIO02	Data	H27	I/O	CV_{DD}	24, 28
SDHC_DAT7/SPI_CS3/GPIO03	Data	H24	I/O	CV_{DD}	24, 28
SDHC_CLK	Host to Card Clock	N24	O	OV_{DD}	—
SDHC_CD/IIC3_SCL/GPIO16/ M1DVAL/LB_DVAL/DMA1_DACK0	Card Detection	AB23	I/O	OV_{DD}	24, 28
SDHC_WP/IIC3_SDA/GPIO17/ M1SRCID0/LB_SRCID0/DMA1_DDONE0	Card Write Protection	AB26	I	OV_{DD}	24, 28
eSPI					
SPI_MOSI	Master Out Slave In	H28	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	G23	I	CV_{DD}	—
SPI_CLK	eSPI Clock	H22	O	CV_{DD}	—
SPI_CS0/SDHC_DAT4/GPIO00	eSPI Chip Select	H26	O	CV_{DD}	24
SPI_CS1/SDHC_DAT5/GPIO01	eSPI Chip Select	H23	O	CV_{DD}	24
SPI_CS2/SDHC_DAT6/GPIO02	eSPI Chip Select	H27	O	CV_{DD}	24
SPI_CS3/SDHC_DAT7/GPIO03	eSPI Chip Select	H24	O	CV_{DD}	24

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND132	Ground	K12	—	—	—
GND131	Ground	K14	—	—	—
GND130	Ground	K16	—	—	—
GND129	Ground	K18	—	—	—
GND128	Ground	K21	—	—	—
GND127	Ground	L8	—	—	—
GND126	Ground	L10	—	—	—
GND125	Ground	L12	—	—	—
GND124	Ground	L14	—	—	—
GND123	Ground	L16	—	—	—
GND122	Ground	L18	—	—	—
GND121	Ground	M2	—	—	—
GND120	Ground	M5	—	—	—
GND119	Ground	M8	—	—	—
GND118	Ground	M10	—	—	—
GND117	Ground	M12	—	—	—
GND116	Ground	M14	—	—	—
GND115	Ground	M16	—	—	—
GND114	Ground	M18	—	—	—
GND113	Ground	N8	—	—	—
GND112	Ground	N10	—	—	—
GND111	Ground	N12	—	—	—
GND110	Ground	N14	—	—	—
GND109	Ground	N16	—	—	—
GND108	Ground	N18	—	—	—
GND107	Ground	N21	—	—	—
GND106	Ground	N25	—	—	—
GND105	Ground	P5	—	—	—
GND104	Ground	P8	—	—	—
GND103	Ground	P10	—	—	—
GND102	Ground	P12	—	—	—
GND101	Ground	P14	—	—	—
GND100	Ground	P16	—	—	—
GND099	Ground	P18	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND098	Ground	P21	—	—	—
GND097	Ground	R2	—	—	—
GND096	Ground	R8	—	—	—
GND095	Ground	R10	—	—	—
GND094	Ground	R12	—	—	—
GND093	Ground	R14	—	—	—
GND092	Ground	R16	—	—	—
GND091	Ground	R18	—	—	—
GND090	Ground	R21	—	—	—
GND089	Ground	R24	—	—	—
GND088	Ground	R27	—	—	—
GND087	Ground	T8	—	—	—
GND086	Ground	T10	—	—	—
GND085	Ground	T12	—	—	—
GND084	Ground	T14	—	—	—
GND083	Ground	T16	—	—	—
GND082	Ground	T18	—	—	—
GND081	Ground	T21	—	—	—
GND080	Ground	U7	—	—	—
GND079	Ground	U8	—	—	—
GND078	Ground	U10	—	—	—
GND077	Ground	U12	—	—	—
GND076	Ground	U14	—	—	—
GND075	Ground	U17	—	—	—
GND074	Ground	U19	—	—	—
GND073	Ground	U22	—	—	—
GND072	Ground	U25	—	—	—
GND071	Ground	V2	—	—	—
GND070	Ground	V4	—	—	—
GND069	Ground	V6	—	—	—
GND068	Ground	V8	—	—	—
GND067	Ground	V10	—	—	—
GND066	Ground	V12	—	—	—
GND065	Ground	V14	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LVDD05	Ethernet Controller 1 and 2 Supply	C26	—	LV_{DD}	—
LVDD04	Ethernet Controller 1 and 2 Supply	E26	—	LV_{DD}	—
LVDD03	Ethernet Controller 1 and 2 Supply	G20	—	LV_{DD}	—
LVDD02	Ethernet Controller 1 and 2 Supply	H20	—	LV_{DD}	—
LVDD01	Ethernet Controller 1 and 2 Supply	J20	—	LV_{DD}	—
POVDD	Fuse Programming Override Supply	U21	—	POV_{DD}	30
VDD_CA_PL78	Core Group A and Platform Supply	G9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL77	Core Group A and Platform Supply	G11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL76	Core Group A and Platform Supply	G13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL75	Core Group A and Platform Supply	G15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL74	Core Group A and Platform Supply	G17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL73	Core Group A and Platform Supply	G19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL72	Core Group A and Platform Supply	H9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL71	Core Group A and Platform Supply	H11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL70	Core Group A and Platform Supply	H13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL69	Core Group A and Platform Supply	H15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL68	Core Group A and Platform Supply	H17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL67	Core Group A and Platform Supply	H19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL66	Core Group A and Platform Supply	J9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL65	Core Group A and Platform Supply	J11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL64	Core Group A and Platform Supply	J13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL63	Core Group A and Platform Supply	J15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL62	Core Group A and Platform Supply	J17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL61	Core Group A and Platform Supply	J19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL60	Core Group A and Platform Supply	K9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL59	Core Group A and Platform Supply	K11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL58	Core Group A and Platform Supply	K13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL57	Core Group A and Platform Supply	K15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL56	Core Group A and Platform Supply	K17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL55	Core Group A and Platform Supply	K19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL54	Core Group A and Platform Supply	L9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL53	Core Group A and Platform Supply	L11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL52	Core Group A and Platform Supply	L13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL51	Core Group A and Platform Supply	L15	—	$V_{DD\_CA\_PL}$	37

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_CA_PL16	Core Group A and Platform Supply	U13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL15	Core Group A and Platform Supply	U15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL14	Core Group A and Platform Supply	U20	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL13	Core Group A and Platform Supply	V9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL12	Core Group A and Platform Supply	V11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL11	Core Group A and Platform Supply	V13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL10	Core Group A and Platform Supply	V15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL09	Core Group A and Platform Supply	W9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL08	Core Group A and Platform Supply	W11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL07	Core Group A and Platform Supply	W13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL06	Core Group A and Platform Supply	W15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL05	Core Group A and Platform Supply	Y9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL04	Core Group A and Platform Supply	Y11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL03	Core Group A and Platform Supply	Y13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL02	Core Group A and Platform Supply	Y15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL01	Core Group A and Platform Supply	AA21	—	$V_{DD\_CA\_PL}$	37
VDD_CB11	Core Group B Supply	U16	—	V_{DD_CB}	37
VDD_CB10	Core Group B Supply	U18	—	V_{DD_CB}	37
VDD_CB09	Core Group B Supply	V18	—	V_{DD_CB}	37
VDD_CB08	Core Group B Supply	V20	—	V_{DD_CB}	37
VDD_CB07	Core Group B Supply	W16	—	V_{DD_CB}	37
VDD_CB06	Core Group B Supply	W18	—	V_{DD_CB}	37
VDD_CB05	Core Group B Supply	W20	—	V_{DD_CB}	37
VDD_CB04	Core Group B Supply	Y18	—	V_{DD_CB}	37
VDD_CB03	Core Group B Supply	Y20	—	V_{DD_CB}	37
VDD_CB02	Core Group B Supply	AA18	—	V_{DD_CB}	37
VDD_CB01	Core Group B Supply	AA20	—	V_{DD_CB}	37
VDD_LP	Low Power Security Monitor Supply	L20	—	V_{DD_LP}	25
AVDD_CC1	Core Cluster PLL1 Supply	V7	—	—	13
AVDD_CC2	Core Cluster PLL2 Supply	W22	—	—	13
AVDD_PLAT	Platform PLL Supply	V22	—	—	13
AVDD_DDR	DDR PLL Supply	W6	—	—	13
AVDD_SRDS1	SerDes PLL1 Supply	C1	—	—	13
AVDD_SRDS2	SerDes PLL2 Supply	A17	—	—	13

Table 2. Absolute Operating Conditions[1] (continued)

Parameter		Symbol	Max Value	Unit	Note
eSPI, eSHDC, GPIO		CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
DDR3 and DDR3L DRAM I/O voltage		GV_{DD}	–0.3 to 1.65	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
SerDes core logic supply and receivers		SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	—
Ethernet I/O, Ethernet management interface 1 (EMI1), 1588, GPIO		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3
USB PHY transceiver supply voltage		$USB\_V_{DD}\_3P3$	–0.3 to 3.63	V	—
USB PHY PLL supply voltage		$USB\_V_{DD}\_1P0$	–0.3 to 1.1	V	—
Low Power Security Monitor Supply		V_{DD_LP}	–0.3 to 1.1	V	—
Input voltage[7]	DDR3 and DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 7
	DDR3 and DDR3L DRAM reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2+ 0.3)	V	2, 7
	Ethernet signals, GPIO	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 7
	eSPI, eSHDC, GPIO	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 7
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	5, 7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6, 7
	SerDes signals	XV_{IN}	–0.4 to (XV_{DD} + 0.3)	V	7
	USB PHY transceiver signals	$USB\_V_{IN}\_3P3$	–0.3 to ($USB\_V_{DD}\_3P3$ + 0.3)	V	7
Storage junction temperature range		T_{stg}	–55 to 150	°C	—

Table 2. Absolute Operating Conditions[1] (continued)

Parameter	Symbol	Max Value	Unit	Note

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. $(C,X,B,G,L,O)V_{IN}$ may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 7.
8. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
9. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
10. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Note
Core Group A (cores 0–1) and platform supply voltage (Silicon Rev 1.0)	$V_{DD\_CA\_PL}$	1.0 ± 50 mV	V	4, 5
Core Group B (cores 2–3) supply voltage (Silicon Rev 1.0)	V_{DD_CB}	1.0 ± 50 mV	V	4, 5
Core Group A (cores 0–1), Core Group B (cores 2–3) and platform supply voltage (Silicon Rev 1.1)	$V_{DD\_CA\_CB\_PL}$	1.0 ± 50 mV	V	4, 5
PLL supply voltage (core, platform, DDR)	AV_{DD}	1.0 ± 50 mV	V	—
PLL supply voltage (SerDes)	AV_{DD_SRDS}	1.0 ± 50 mV	V	—
Fuse programming override supply	POV_{DD}	1.5 ± 75 mV	V	2
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	3.3 ± 165 mV	V	—
eSPI, eSDHC, GPIO	CV_{DD}	3.3 ± 165 mV 2.5 ± 125 mV 1.8 ± 90 mV	V	—
DDR DRAM I/O voltage DDR3 DDR3L	GV_{DD}	 1.5 ± 75 mV 1.35 ± 67 mV	V	—

2.1.3 Output Driver Characteristics

This table provides information about the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	(Nominal) Supply Voltage	Note
Local Bus interface utilities signals	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR3 signal	20 (full-strength mode) 40 (half-strength mode)	GV_{DD} = 1.5 V	1
DDR3L signal	20 (full-strength mode) 40 (half-strength mode)	GV_{DD} = 1.35 V	1
eTSEC/10/100 signals	45 45	LV_{DD} = 3.3 V LV_{DD} = 2.5 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—
eSPI, eSDHC	45 45 45	CV_{DD} = 3.3 V CV_{DD} = 2.5 V CV_{DD} =1.8 V	—

Note:

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at T_j = 105 °C and at GV_{DD} (min).

2.2 Power Up Sequencing

The device requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. Bring up OV_{DD}, LV_{DD}, BV_{DD}, CV_{DD}, and USB_V_{DD}_3P3. Drive POV_{DD} = GND.
   - — $\overline{\text{PORESET}}$ input must be driven asserted and held during this step.
   - — IO_VSEL inputs must be driven during this step and held stable during normal operation.
   - — USB_V_{DD}_3P3 rise time (10% to 90%) has a minimum of 350 µs.
2. Bring up $V_{DD\_CA\_CB\_PL}$, SV_{DD}, AV_{DD} (cores, platform, SerDes) and USB_V_{DD}_1P0. $V_{DD\_CA\_CB\_PL}$ and USB_V_{DD}_1P0 must be ramped up simultaneously.
3. Bring up GV_{DD} (DDR) and XV_{DD}.
4. Negate $\overline{\text{PORESET}}$ input as long as the required assertion/hold time has been met per Table 17.
5. For secure boot fuse programming: After negation of $\overline{\text{PORESET}}$, drive POV_{DD} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD} = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5. See Section 5, "Security Fuse Processor," for additional details.

WARNING

Only two secure boot fuse programming events are permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND.

Table 13. SYSCLK AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	67	—	133	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	±150	ps	—
SYSCLK jitter phase noise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD} \div 2$.
3. Slew rate as measured from ± 0.3 $\Delta \mathbf{V_{AC}}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.6.2 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the device input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the device is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread Spectrum Clock Source Recommendations

For recommended operating conditions, see Table 3.

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

2.11.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 35. DUART AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Value	Unit	Note
Minimum baud rate	$f_{PLAT}/(2 \times 1{,}048{,}576)$	baud	1
Maximum baud rate	$f_{PLAT}/(2 \times 16)$	baud	1, 2
Oversample rate	16	—	3

Note:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled every 16th sample.

2.12 Ethernet: Data path Three-Speed Ethernet (dTSEC), Management Interface, IEEE Std 1588

This section provides the AC and DC electrical characteristics for the data path three-speed Ethernet controller, the Ethernet Management Interface, and the IEEE Std 1588 interface.

2.12.1 SGMII Timing Specifications

See Section 2.20.8, "SGMII Interface."

2.12.2 RGMII Timing Specifications

This section discusses the electrical characteristics for the MII and RGMII interfaces.

2.12.2.1 RGMII DC Electrical Characteristics

This table shows the RGMII DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 36. RGMII DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

Table 41. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

This table shows the eTSEC IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 42. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.12.5 eTSEC IEEE Std 1588 AC Specifications

This table provides the eTSEC IEEE 1588 AC timing specifications.

Table 43. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	6.4	—	$T_{RX\_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.5	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

2.14 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 46. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 47. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

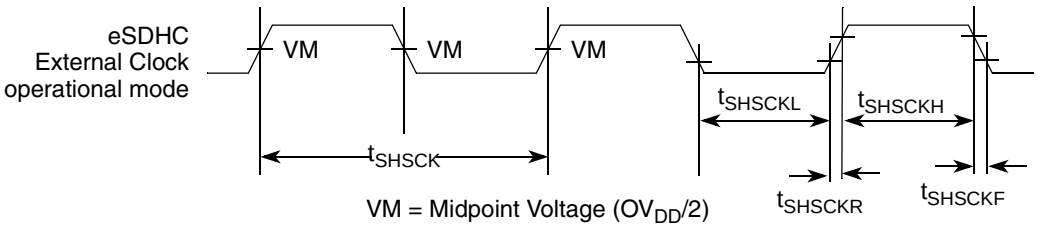

Figure 23. eSDHC Clock Input Timing Diagram

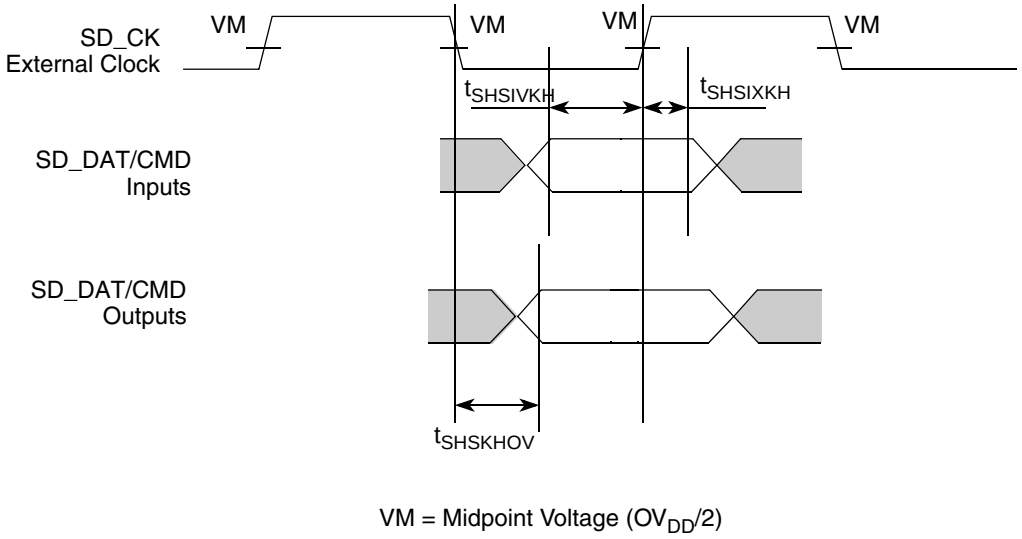

Figure 24. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.16 Multicore Programmable Interrupt Controller (MPIC) Specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC DC specifications

This table provides the DC electrical characteristics for the MPIC interface.

Table 52. MPIC DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Table 62. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 63. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	—	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.4.4 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

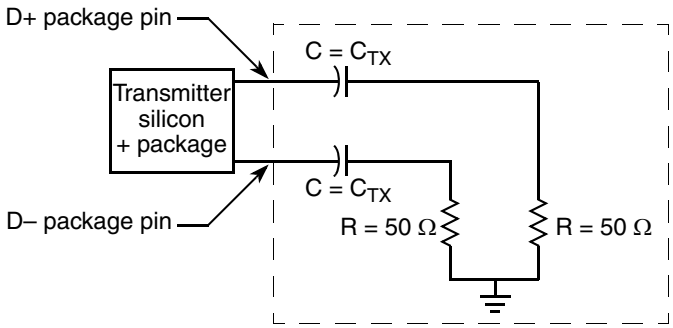

Figure 46. SGMII AC Test/Measurement Load

2.20.8.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 92. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Note:
1. Measured at receiver
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 System Clocking

This section describes the PLL configuration of the device.

This device includes six PLLs, as follows:

- There are two selectable core cluster PLLs that generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL; core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3,

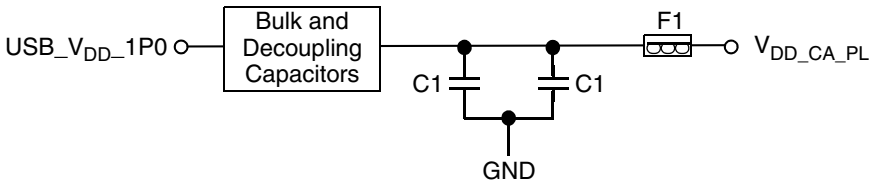

Figure 53. USB_V_{DD}_1P0 Power Supply Filter Circuit

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip's system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

3.5 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a 1-µF ceramic chip capacitor on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND pins of the device.

The Ethernet controllers 1 and/or 2 input pins may be disabled by setting their respective RCW configuration field EC1 (bits 360–361) and EC2 (bits 363–364) to 0b11 = No parallel mode Ethernet. When disabled, these inputs do not need to be externally pulled to an appropriate signal level.

isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, or TDO.

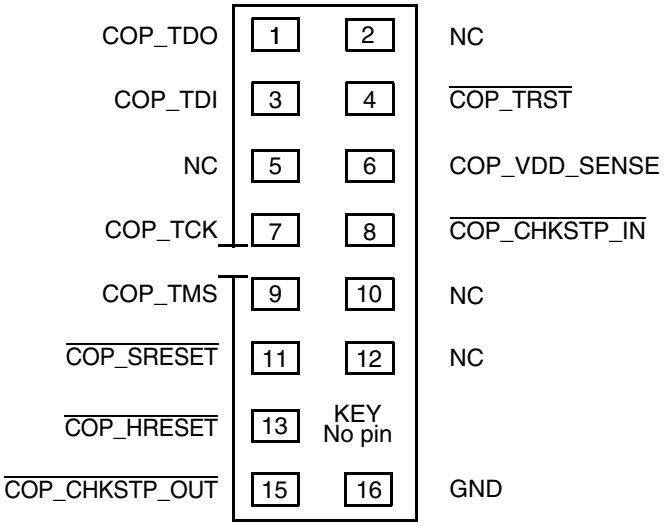

Figure 54. Legacy COP Connector Physical Pinout