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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2041nsn7pnac

This figure shows the major functional units within the chip.

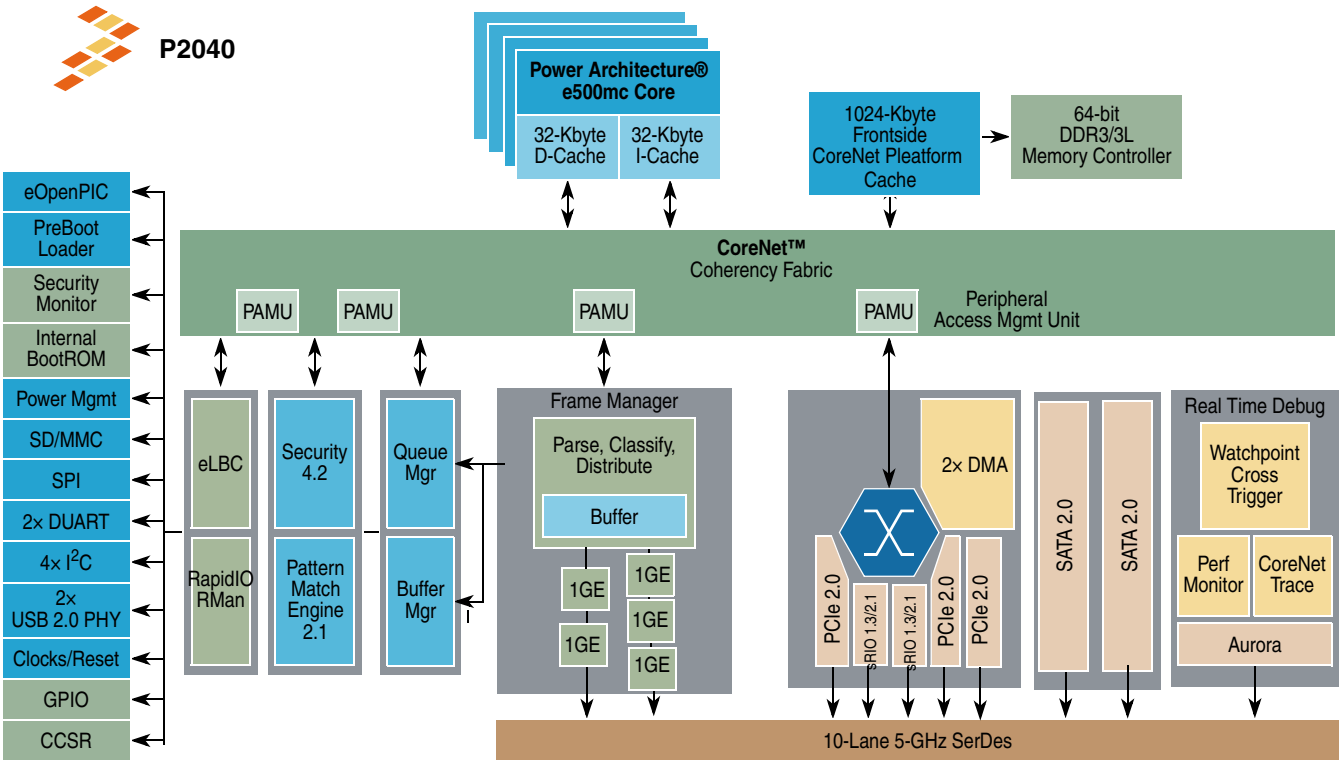


Figure 1. Block Diagram

1 Pin Assignments and Reset States

This section provides a top view of the ball layout diagram and four detailed views by quadrant. It also provides a pinout listing by bus.

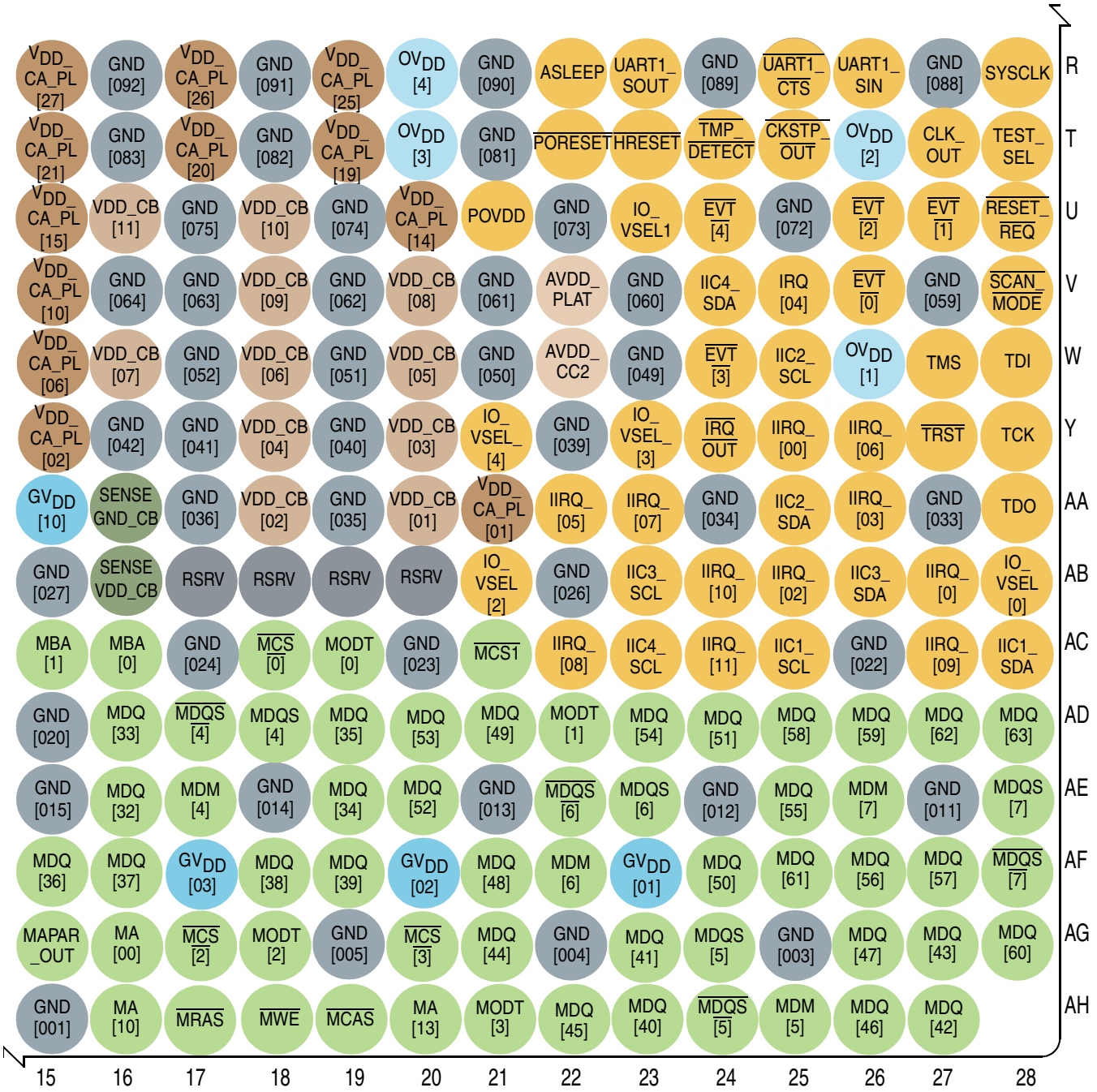


Figure 6. 780 BGA Ball Map Diagram (Detail View D)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ29	Data	AC4	I/O	GV_{DD}	—
MDQ30	Data	AE1	I/O	GV_{DD}	—
MDQ31	Data	AE3	I/O	GV_{DD}	—
MDQ32	Data	AE16	I/O	GV_{DD}	—
MDQ33	Data	AD16	I/O	GV_{DD}	—
MDQ34	Data	AE19	I/O	GV_{DD}	—
MDQ35	Data	AD19	I/O	GV_{DD}	—
MDQ36	Data	AF15	I/O	GV_{DD}	—
MDQ37	Data	AF16	I/O	GV_{DD}	—
MDQ38	Data	AF18	I/O	GV_{DD}	—
MDQ39	Data	AF19	I/O	GV_{DD}	—
MDQ40	Data	AH23	I/O	GV_{DD}	—
MDQ41	Data	AG23	I/O	GV_{DD}	—
MDQ42	Data	AH27	I/O	GV_{DD}	—
MDQ43	Data	AG27	I/O	GV_{DD}	—
MDQ44	Data	AG21	I/O	GV_{DD}	—
MDQ45	Data	AH22	I/O	GV_{DD}	—
MDQ46	Data	AH26	I/O	GV_{DD}	—
MDQ47	Data	AG26	I/O	GV_{DD}	—
MDQ48	Data	AF21	I/O	GV_{DD}	—
MDQ49	Data	AD21	I/O	GV_{DD}	—
MDQ50	Data	AF24	I/O	GV_{DD}	—
MDQ51	Data	AD24	I/O	GV_{DD}	—
MDQ52	Data	AE20	I/O	GV_{DD}	—
MDQ53	Data	AD20	I/O	GV_{DD}	—
MDQ54	Data	AD23	I/O	GV_{DD}	—
MDQ55	Data	AE25	I/O	GV_{DD}	—
MDQ56	Data	AF26	I/O	GV_{DD}	—
MDQ57	Data	AF27	I/O	GV_{DD}	—
MDQ58	Data	AD25	I/O	GV_{DD}	—
MDQ59	Data	AD26	I/O	GV_{DD}	—
MDQ60	Data	AG28	I/O	GV_{DD}	—
MDQ61	Data	AF25	I/O	GV_{DD}	—
MDQ62	Data	AD27	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_RX04	Receive Data (positive)	A2	I	XV_{DD}	—
SD_RX03	Receive Data (positive)	E1	I	XV_{DD}	—
SD_RX02	Receive Data (positive)	G1	I	XV_{DD}	—
$\overline{\text{SD\_RX13}}$	Receive Data (negative)	A21	I	XV_{DD}	—
$\overline{\text{SD\_RX12}}$	Receive Data (negative)	A19	I	XV_{DD}	—
$\overline{\text{SD\_RX11}}$	Receive Data (negative)	A15	I	XV_{DD}	—
$\overline{\text{SD\_RX10}}$	Receive Data (negative)	B13	I	XV_{DD}	—
$\overline{\text{SD\_RX07}}$	Receive Data (negative)	A11	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive Data (negative)	A9	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive Data (negative)	A7	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive Data (negative)	A3	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive Data (negative)	E2	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive Data (negative)	G2	I	XV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	D3	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes Bank 1 PLL Reference Clock Complement	D4	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	E17	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes Bank 2 PLL Reference Clock Complement	F17	I	XV_{DD}	—
General-Purpose Input/Output					
GPIO00/$\overline{\text{SPI\_CS0}}$/SDHC_DATA4	General Purpose Input/Output	H26	I/O	CV_{DD}	—
GPIO01/$\overline{\text{SPI\_CS1}}$/SDHC_DATA5	General Purpose Input/Output	H23	I/O	CV_{DD}	—
GPIO02/$\overline{\text{SPI\_CS2}}$/SDHC_DATA6	General Purpose Input/Output	H27	I/O	CV_{DD}	—
GPIO03$\overline{\text{SPI_CS3}}$/SDHC_DATA7	General Purpose Input/Output	H24	I/O	CV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input/Output	R23	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input/Output	P26	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input/Output	R26	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input/Output	P27	I/O	OV_{DD}	—
GPIO12/$\overline{\text{UART1\_RTS}}$/UART3_SOUT	General Purpose Input/Output	P24	I/O	OV_{DD}	—
GPIO13/$\overline{\text{UART2\_RTS}}$/UART4_SOUT	General Purpose Input/Output	P25	I/O	OV_{DD}	—
GPIO14/$\overline{\text{UART1\_CTS}}$/UART3_SIN	General Purpose Input/Output	R25	I/O	OV_{DD}	—
GPIO15/$\overline{\text{UART2\_CTS}}$/UART4_SIN	General Purpose Input/Output	P23	I/O	OV_{DD}	—
GPIO16/IIC3_SCL/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/$\overline{\text{SDHC\_CD}}$	General Purpose Input/Output	AB23	I/O	OV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND098	Ground	P21	—	—	—
GND097	Ground	R2	—	—	—
GND096	Ground	R8	—	—	—
GND095	Ground	R10	—	—	—
GND094	Ground	R12	—	—	—
GND093	Ground	R14	—	—	—
GND092	Ground	R16	—	—	—
GND091	Ground	R18	—	—	—
GND090	Ground	R21	—	—	—
GND089	Ground	R24	—	—	—
GND088	Ground	R27	—	—	—
GND087	Ground	T8	—	—	—
GND086	Ground	T10	—	—	—
GND085	Ground	T12	—	—	—
GND084	Ground	T14	—	—	—
GND083	Ground	T16	—	—	—
GND082	Ground	T18	—	—	—
GND081	Ground	T21	—	—	—
GND080	Ground	U7	—	—	—
GND079	Ground	U8	—	—	—
GND078	Ground	U10	—	—	—
GND077	Ground	U12	—	—	—
GND076	Ground	U14	—	—	—
GND075	Ground	U17	—	—	—
GND074	Ground	U19	—	—	—
GND073	Ground	U22	—	—	—
GND072	Ground	U25	—	—	—
GND071	Ground	V2	—	—	—
GND070	Ground	V4	—	—	—
GND069	Ground	V6	—	—	—
GND068	Ground	V8	—	—	—
GND067	Ground	V10	—	—	—
GND066	Ground	V12	—	—	—
GND065	Ground	V14	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
USB1_AGND01	USB1 PHY Transceiver GND	M28	—	—	—
USB2_AGND06	USB2 PHY Transceiver GND	J22	—	—	—
USB2_AGND05	USB2 PHY Transceiver GND	J24	—	—	—
USB2_AGND04	USB2 PHY Transceiver GND	J26	—	—	—
USB2_AGND03	USB2 PHY Transceiver GND	K25	—	—	—
USB2_AGND02	USB2 PHY Transceiver GND	L25	—	—	—
USB2_AGND01	USB2 PHY Transceiver GND	M26	—	—	—
OVDD06	General I/O Supply	N20	—	OV_{DD}	—
OVDD05	General I/O Supply	P20	—	OV_{DD}	—
OVDD04	General I/O Supply	R20	—	OV_{DD}	—
OVDD03	General I/O Supply	T20	—	OV_{DD}	—
OVDD02	General I/O Supply	T26	—	OV_{DD}	—
OVDD01	General I/O Supply	W26	—	OV_{DD}	—
CVDD2	eSPI and eSDHC Supply	K20	—	CV_{DD}	—
CVDD1	eSPI and eSDHC Supply	M20	—	CV_{DD}	—
GVDD17	DDR Supply	AA8	—	GV_{DD}	—
GVDD16	DDR Supply	AA9	—	GV_{DD}	—
GVDD15	DDR Supply	AA10	—	GV_{DD}	—
GVDD14	DDR Supply	AA11	—	GV_{DD}	—
GVDD13	DDR Supply	AA12	—	GV_{DD}	—
GVDD12	DDR Supply	AA13	—	GV_{DD}	—
GVDD11	DDR Supply	AA14	—	GV_{DD}	—
GVDD10	DDR Supply	AA15	—	GV_{DD}	—
GVDD09	DDR Supply	AB13	—	GV_{DD}	—
GVDD08	DDR Supply	AB14	—	GV_{DD}	—
GVDD07	DDR Supply	AC13	—	GV_{DD}	—
GVDD06	DDR Supply	AC14	—	GV_{DD}	—
GVDD05	DDR Supply	AF6	—	GV_{DD}	—
GVDD04	DDR Supply	AF9	—	GV_{DD}	—
GVDD03	DDR Supply	AF17	—	GV_{DD}	—
GVDD02	DDR Supply	AF20	—	GV_{DD}	—
GVDD01	DDR Supply	AF23	—	GV_{DD}	—
BVDD07	Local Bus Supply	J7	—	BV_{DD}	—
BVDD06	Local Bus Supply	K7	—	BV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_CA_PL16	Core Group A and Platform Supply	U13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL15	Core Group A and Platform Supply	U15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL14	Core Group A and Platform Supply	U20	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL13	Core Group A and Platform Supply	V9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL12	Core Group A and Platform Supply	V11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL11	Core Group A and Platform Supply	V13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL10	Core Group A and Platform Supply	V15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL09	Core Group A and Platform Supply	W9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL08	Core Group A and Platform Supply	W11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL07	Core Group A and Platform Supply	W13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL06	Core Group A and Platform Supply	W15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL05	Core Group A and Platform Supply	Y9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL04	Core Group A and Platform Supply	Y11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL03	Core Group A and Platform Supply	Y13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL02	Core Group A and Platform Supply	Y15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL01	Core Group A and Platform Supply	AA21	—	$V_{DD\_CA\_PL}$	37
VDD_CB11	Core Group B Supply	U16	—	V_{DD_CB}	37
VDD_CB10	Core Group B Supply	U18	—	V_{DD_CB}	37
VDD_CB09	Core Group B Supply	V18	—	V_{DD_CB}	37
VDD_CB08	Core Group B Supply	V20	—	V_{DD_CB}	37
VDD_CB07	Core Group B Supply	W16	—	V_{DD_CB}	37
VDD_CB06	Core Group B Supply	W18	—	V_{DD_CB}	37
VDD_CB05	Core Group B Supply	W20	—	V_{DD_CB}	37
VDD_CB04	Core Group B Supply	Y18	—	V_{DD_CB}	37
VDD_CB03	Core Group B Supply	Y20	—	V_{DD_CB}	37
VDD_CB02	Core Group B Supply	AA18	—	V_{DD_CB}	37
VDD_CB01	Core Group B Supply	AA20	—	V_{DD_CB}	37
VDD_LP	Low Power Security Monitor Supply	L20	—	V_{DD_LP}	25
AVDD_CC1	Core Cluster PLL1 Supply	V7	—	—	13
AVDD_CC2	Core Cluster PLL2 Supply	W22	—	—	13
AVDD_PLAT	Platform PLL Supply	V22	—	—	13
AVDD_DDR	DDR PLL Supply	W6	—	—	13
AVDD_SRDS1	SerDes PLL1 Supply	C1	—	—	13
AVDD_SRDS2	SerDes PLL2 Supply	A17	—	—	13

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
Reserve	—	AB20	—	GND	19

Note:

1. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD} in order to ensure no random chip select assertion due to possible noise, etc.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the corresponding power and ground nets internally. They may be connected as a differential pair to be used by the voltage regulators with remote sense function. For Rev1.1 silicon, the better solution is to use the far sense pins relative to the power supply location, the other pair can be left as no connected. The DC power simulation should be done during the board layout process to approve the selected solution.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
10. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
11. Do not connect.
12. These are test signals for factory use only and must be pulled low (1 KΩ–2 kΩ) to ground (GND) for normal machine operation.
13. Independent supplies derived from board $V_{DD\_CA\_CB\_PL}$ (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD} if I^2C interface is used.
15. This pin requires an external 1 KΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
17. These pins must be pulled up to 1.2 V through a 180 $\Omega \pm 1\%$ resistor for EM2_MDC and a 330 $\Omega \pm 1\%$ resistor for EM2_MDIO.
18. Pin has a weak internal pull-up.
19. These pins must be pulled to ground (GND).
20. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
21. This pin requires a 200-Ω pull-up to XV_{DD}.
22. This pin requires a 200-Ω pull-up to SV_{DD}.
23. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
24. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
25. See Section 3.6, "Connection Recommendations," for additional details on this signal.

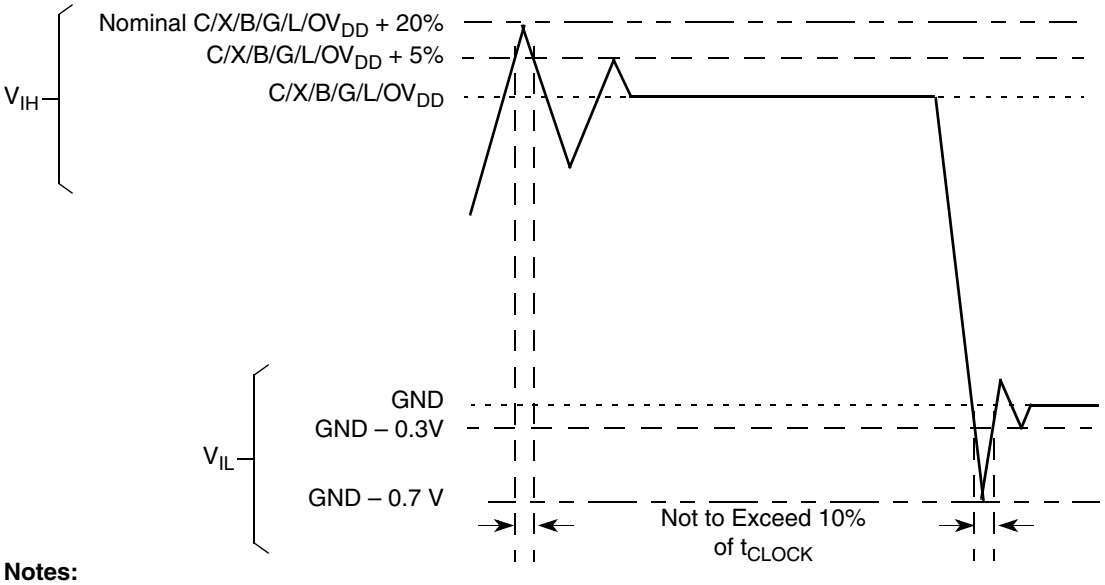
Table 3. Recommended Operating Conditions (continued)

Parameter	Symbol	Recommended Value	Unit	Note

Note:

1. POV_{DD} must be supplied 1.5 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Up Sequencing."
2. Selecting RGMII limits LV_{DD} to 2.5 V.
3. Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.
4. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
5. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Notes:

t_{CLOCK} refers to the clock period associated with the respective interface:

- For I^2C, t_{CLOCK} refers to SYSCLK.
- For DDR GV_{DD}, t_{CLOCK} refers to D*n*_MCK.
- For eSPI CV_{DD}, t_{CLOCK} refers to SPI_CLK.
- For eLBC BV_{DD}, t_{CLOCK} refers to LCLK.
- For SerDes XV_{DD}, t_{CLOCK} refers to SD_REF_CLK.
- For dTSEC LV_{DD}, t_{CLOCK} refers to EC_GTX_CLK125.
- For JTAG OV_{DD}, t_{CLOCK} refers to TCK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$

The core and platform voltages must always be provided at nominal 1.0 V. See Table 3 for the actual recommended core voltage conditions. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. CV_{DD}, BV_{DD}, OV_{DD}, and LV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied $MV_{REF}n$ signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.5/SSTL_1.35 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

Table 6. Device Power Dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	667	534	1067	467	1.0	65	8.7	—	8.2	—	—	2, 3
Thermal						105	12.0	—	11.8	—	—	5, 7
Maximum							12.3	11.1	11.9	10.6	1.4	4, 6, 7

Note:

1. Combined power of $V_{DD\_CA\_CB\_PL}$, SVDD with the DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P2040 I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.705	1.764	W	1,2,5,6
	800 MT/s data rate		0.714	1.785		
	1066 MT/s data rate		0.731	1.827		
	1200 MT/s data rate		0.739	1.848		
	1333 MT/s data rate		0.747	1.869		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1, 7
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC Per Controller	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6

2.7 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 17. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit[1]	Note
Required assertion time of $\overline{\text{PORESET}}$	1	—	ms	3
Required input assertion time of $\overline{\text{HRESET}}$	32	—	SYSCLKs	1, 2
Input setup time for POR configs with respect to negation of $\overline{\text{PORESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Note:
1. SYSCLK is the primary clock input for the device.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1, “Power-On Reset Sequence,” in the chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. Refer to Section 2.2, “Power Up Sequencing.”

Table 18. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

2.8 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 19. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (For example exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

Table 57. I²C AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 2 above is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

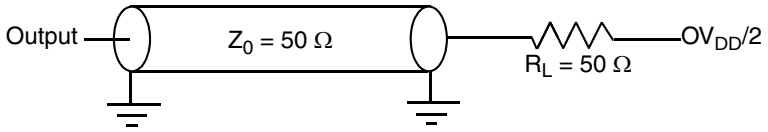


Figure 29. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

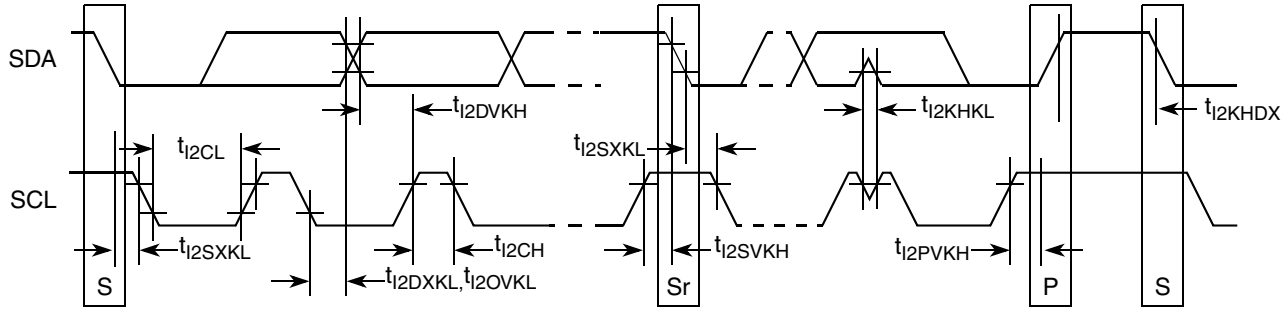


Figure 30. I²C Bus AC Timing Diagram

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 64. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Rx DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50 k	—	—	Ω	Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Rx DC Differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required Rx D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 3.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.20.5.1 Signal Definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. This figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$—each have a peak-to-peak swing of A – B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

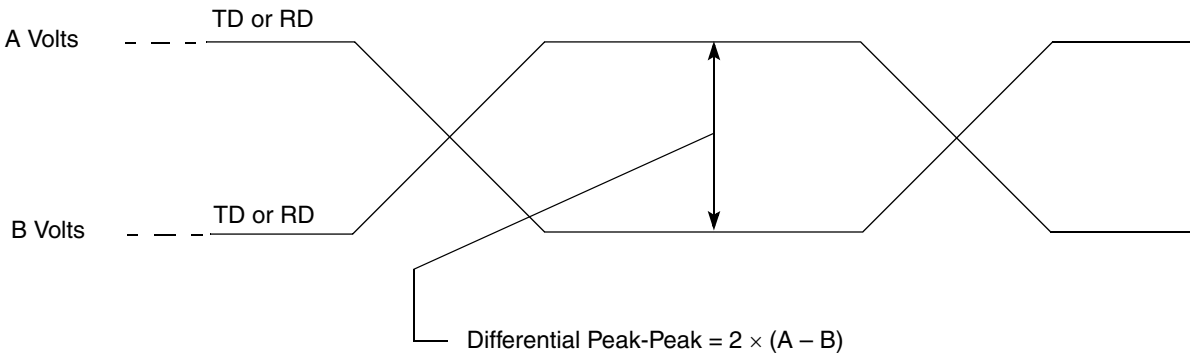


Figure 41. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.20.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.

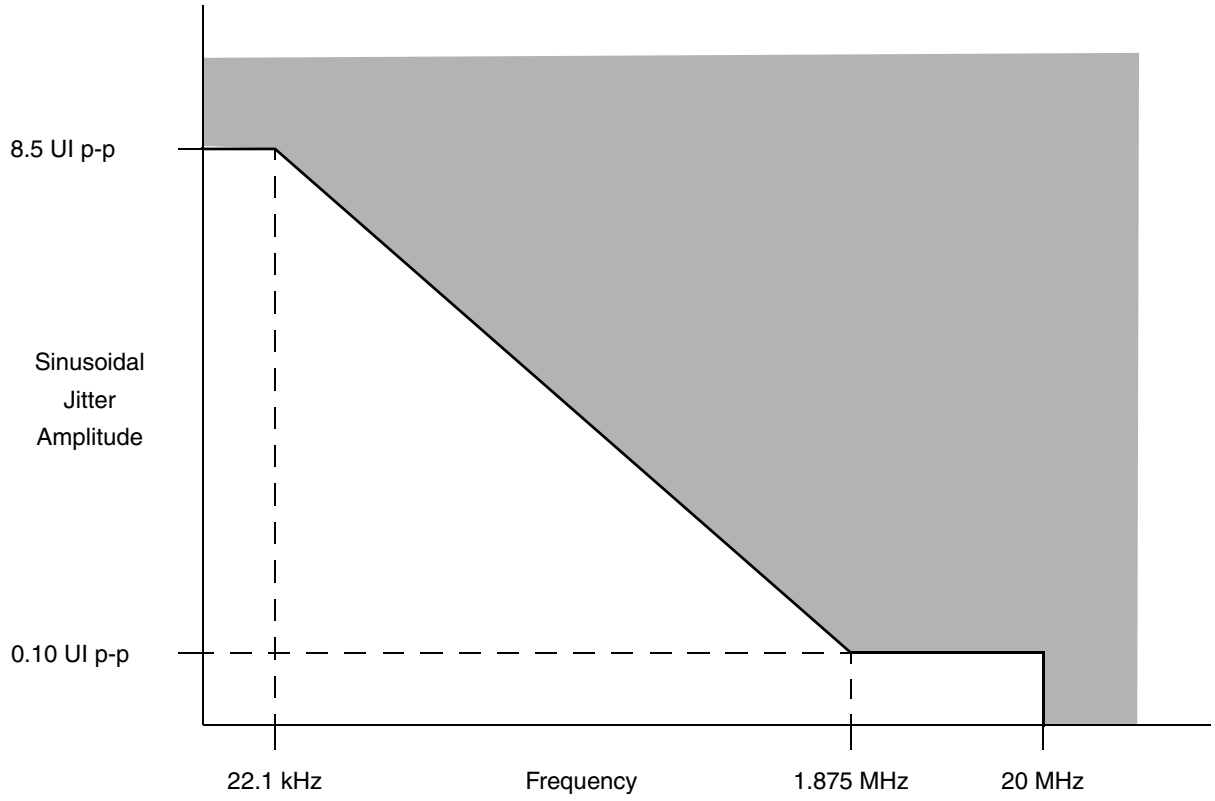


Figure 42. Single-Frequency Sinusoidal Jitter Limits

2.20.6 Aurora

This section describes the Aurora clocking requirements and AC and DC electrical characteristics.

2.20.6.1 Aurora DC Electrical Characteristics

This section describes the DC electrical characteristics for Aurora.

2.20.6.1.1 Aurora DC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 2(SD_REF_CLK2 and $\overline{\text{SD\_REF\_CLK2}}$) may be used for SerDes Aurora configurations based on the RCW configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 1.

For more information on these specifications, see Section 2.20.2, "SerDes Reference Clocks."

2.20.6.1.2 Aurora Transmitter DC Electrical Characteristics

This table provides the Aurora transmitter DC electrical characteristics (XVDD = 1.5 V or 1.8 V).

Table 74. Aurora Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p

2.20.6.1.3 Aurora Receiver DC Electrical Characteristics

This table provides the Aurora receiver DC electrical characteristics (XVDD = 1.5 V or 1.8 V).

Table 75. Aurora Receiver DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:
1. Measured at receiver

2.20.6.2 Aurora AC Timing Specifications

This section describes the AC timing specifications for Aurora.

2.20.6.2.1 Aurora AC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 2(SD_REF_CLK2 and $\overline{\text{SD\_REF\_CLK2}}$) may be used for SerDes Aurora configurations based on the RCW configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 1.

2.20.6.2.2 Aurora Transmitter AC Timing Specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 76. Aurora Transmitter AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

2.20.6.2.3 Aurora Receiver AC Timing Specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 77. Aurora Receiver AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—

3.1.6 Frequency Options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and Platform Frequency Options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 100. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	66.66	83.33	100.00	111.11	133.33
	Platform Frequency (MHz)[1]				
4:1					533
5:1				555	
6:1			600		
7:1		583			
8:1	533				

[1] Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 47. Gen 1 PCI Express Minimum Platform Frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 48. Gen 2 PCI Express Minimum Platform Frequency

See Section 18.1.3.2, “Link Width,” in the chip reference manual for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width of the single widest port used (not combined width of the number ports used) as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times 0.8512 \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

Figure 49. sRIO Minimum Platform Frequency

EC*n*_GTX_CLK125 is a 125-MHz input clock on the dTSEC ports. If the dTSEC ports are not used for RGMII, the EC*n*_GTX_CLK125 input can be tied off to GND.

If RCW field I2C = 0b0100 or 0b0101 (RCW bits 354–357), the SDHC_WP and $\overline{\text{SDHC\_CD}}$ input signals are enabled for external use. If SDHC_WP and $\overline{\text{SDHC\_CD}}$ are selected and not used, they must be externally pulled low such that SDHC_WP = 0 (write enabled) and $\overline{\text{SDHC\_CD}}$ = 0 (card detected). If RCW field I2C ≠ 0b0100 or 0b0101, thereby selecting either I2C3 or GPIO functionality, SDHC_WP and $\overline{\text{SDHC\_CD}}$ are internally driven such that SDHC_WP = write enabled and $\overline{\text{SDHC\_CD}}$ = card detected and the selected I2C3 or GPIO external pin functionality may be used.

$\overline{\text{TMP\_DETECT}}$ pin and $\overline{\text{LP\_TMP DETECT}}$ pin are active low input to the Security Monitor (refer to the “Secure Boot and Trust Architecture” chapter of the chip reference manual). If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. A 1K pulldown resistor strongly recommended. If Trust is used without tamper sensors, tie high.VDD_LP must be connected even if Low Power features aren’t used. Otherwise, the LP_Section will generate internal errors that will prevent the high power trust section from reaching Trusted/Secure state.

3.6.1 Legacy JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 55. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 55 allows the COP port to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well.

The COP interface has a standard header, shown in Figure 54, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 54 is common to all known emulators.

3.6.1.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{PORESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 55. If this is not possible, the

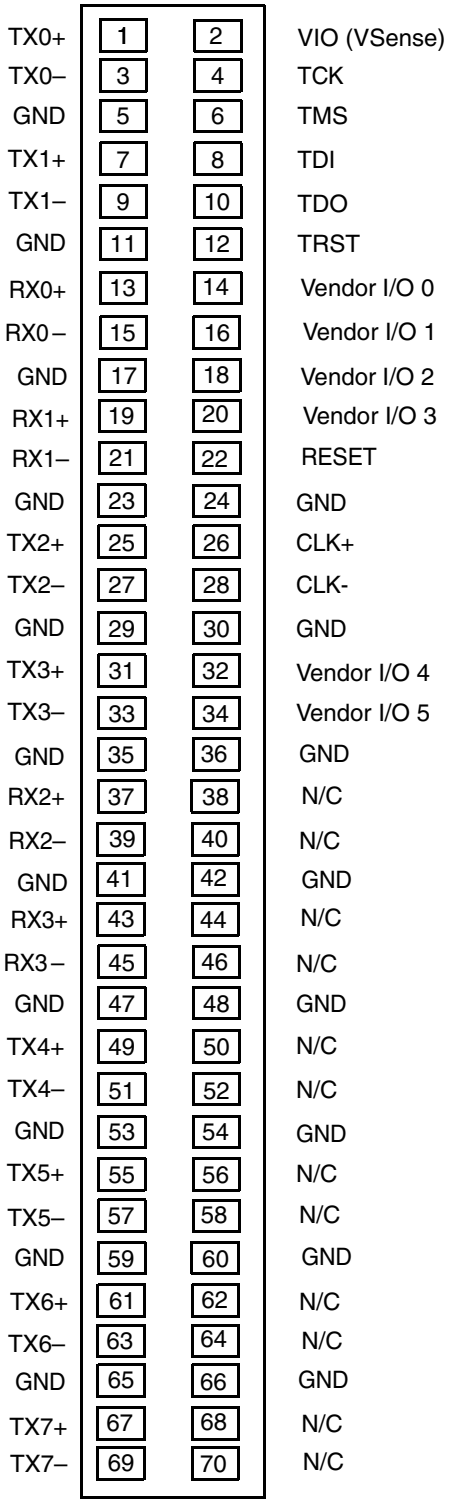


Figure 57. Aurora 70 Pin Connector Duplex Pinout

5 Security Fuse Processor

The device implements the QorIQ platform's Trust Architecture supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power Up Sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} must be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part Numbering Nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature. Not all possible combinations of part numbers implied by the part numbering scheme are supported. For a list of available part numbers, contact your Freescale Sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 107. Part Numbering Nomenclature

p	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temp. Range**	**Encryption**	**Package Type**	**CPU Freq**	**DDR Data Rate**	**Die Revision**
P = 45 nm	1–5	01 = 1 core 02 = 2 cores 04 = 4 cores	0–9	P = Prototype N = Industrial qualification	S = Std temp X = Extended temp (–40 to 105C)	E = SEC present N = SEC not present	1 = FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	F = 667 MHz H = 800 MHz K = 1000 MHz M = 1200 MHz	L = 1067 MT/s M = 1200 MT/s	A = Rev 1.0 B = Rev 1.1 C = Rev 2.0

6.2 Orderable Part Numbers Addressed by this Document

This table provides the Freescale orderable part numbers addressed by this document for the chip.