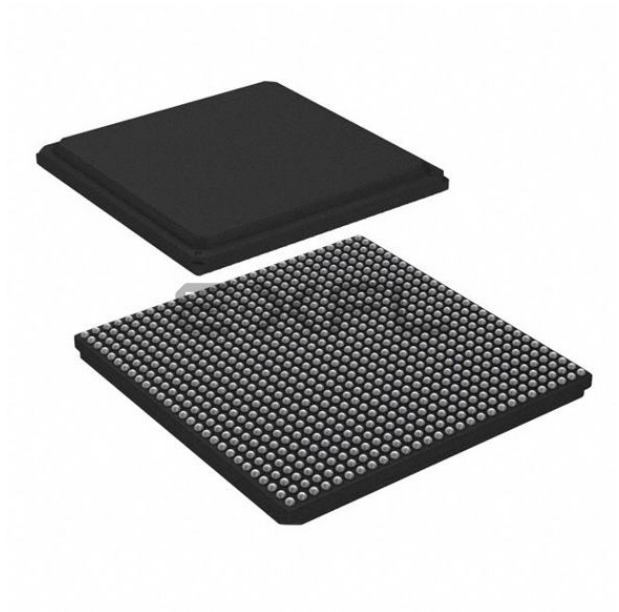

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2041nsn7pnc

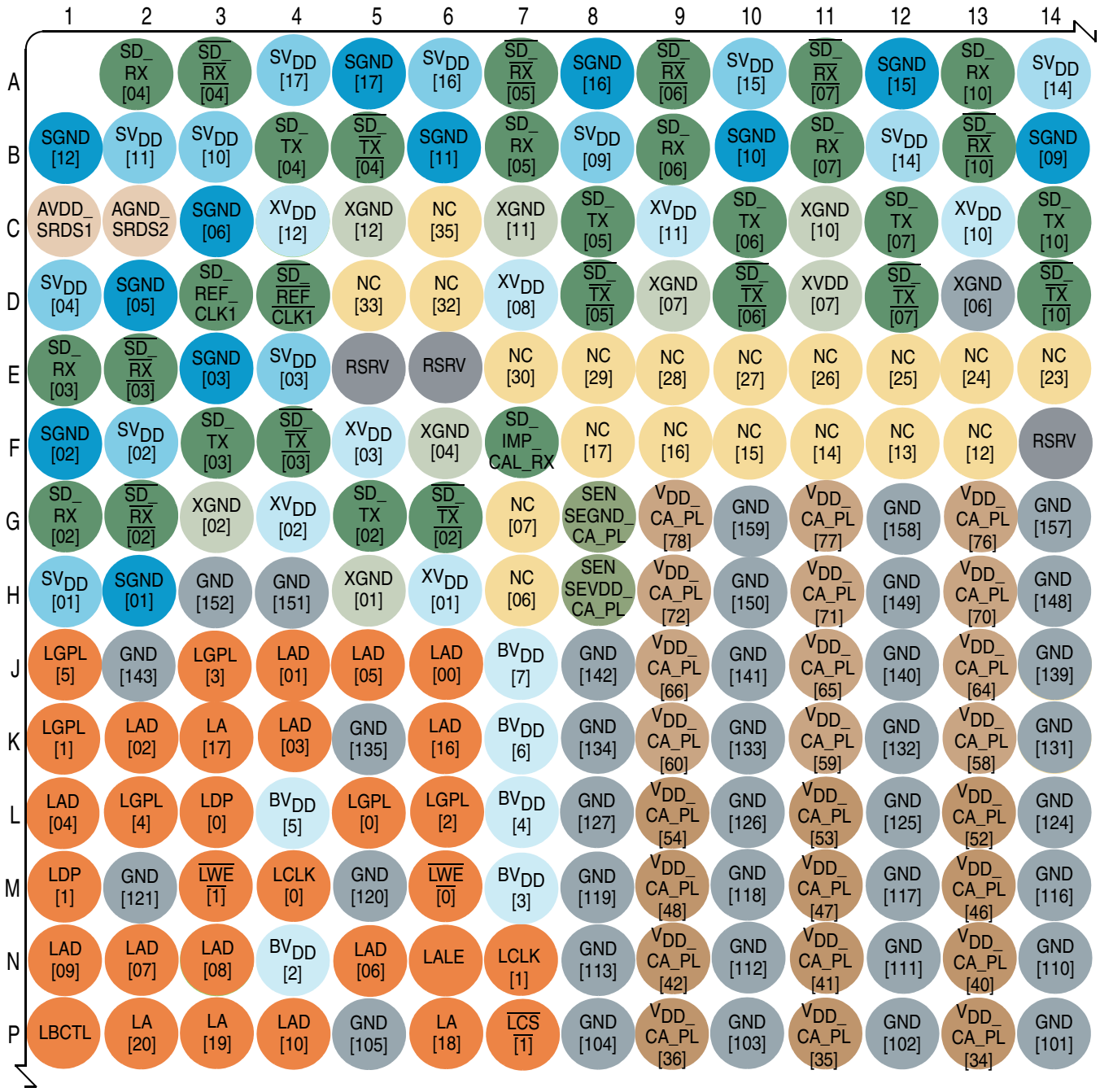


Figure 3. 780 BGA Ball Map Diagram (Detail View A)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LA19	Address	P3	I/O	BV_{DD}	31
LA20	Address	P2	I/O	BV_{DD}	31
LA21	Address	R3	I/O	BV_{DD}	31
LA22	Address	T1	I/O	BV_{DD}	31
LA23	Address	U1	I/O	BV_{DD}	3
LA24	Address	R6	I/O	BV_{DD}	3
LA25	Address	T5	I/O	BV_{DD}	31
LA26	Address	T3	I/O	BV_{DD}	3, 29
LA27	Address	T2	O	BV_{DD}	—
LA28	Address	U5	I/O	BV_{DD}	—
LA29	Address	U3	I/O	BV_{DD}	—
LA30	Address	V1	I/O	BV_{DD}	—
LA31	Address	V3	I/O	BV_{DD}	—
LDP0	Data Parity	L3	I/O	BV_{DD}	—
LDP1	Data Parity	M1	I/O	BV_{DD}	—
$\overline{\text{LCS0}}$	Chip Selects	R5	O	BV_{DD}	5
$\overline{\text{LCS1}}$	Chip Selects	P7	O	BV_{DD}	5
$\overline{\text{LCS2}}$	Chip Selects	U4	O	BV_{DD}	5
$\overline{\text{LCS3}}$	Chip Selects	R1	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write Enable	M6	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write Enable	M3	O	BV_{DD}	—
LBCTL	Buffer Control	P1	O	BV_{DD}	—
LALE	Address Latch Enable	N6	I/O	BV_{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	L5	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	K1	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	L6	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose LIne 3/ LFWP_B—FCM	J3	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	L2	I/O	BV_{DD}	36
LGPL5	UPM General Purpose Line 5 / Amux	J1	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	M4	O	BV_{DD}	—
LCLK1	Local Bus Clock	N7	O	BV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
EC1_RXD1/TSEC_1588_TRIG_IN2	Receive Data	A27	I	LV_{DD}	25
EC1_RXD0/TSEC_1588_TRIG_IN1	Receive Data	B28	I	LV_{DD}	25
EC1_RX_DV/EC_XTRNL_RX_STMP1	Receive Data Valid	A25	I	LV_{DD}	25
EC1_RX_CLK/EC_XTRNL_RX_STMP2	Receive Clock	C24	I	LV_{DD}	25
Three-Speed Ethernet Controller 2					
EC2_TXD3	Transmit Data	G28	O	LV_{DD}	—
EC2_TXD2	Transmit Data	G26	O	LV_{DD}	—
EC2_TXD1	Transmit Data	G27	O	LV_{DD}	—
EC2_TXD0	Transmit Data	G25	O	LV_{DD}	—
EC2_TX_EN	Transmit Enable	F28	O	LV_{DD}	15
EC2_GTX_CLK	Transmit Clock Out (RGMII)	E28	O	LV_{DD}	24
EC2_RXD3	Receive Data	D28	I	LV_{DD}	25
EC2_RXD2	Receive Data	E27	I	LV_{DD}	25
EC2_RXD1	Receive Data	E25	I	LV_{DD}	24, 25
EC2_RXD0	Receive Data	F26	I	LV_{DD}	24, 25
EC2_RX_DV	Receive Data Valid	D25	I	LV_{DD}	25
EC2_RX_CLK	Receive Clock	F25	I	LV_{DD}	25
UART					
UART1_SOUT/GPIO8	Transmit Data	R23	O	OV_{DD}	24
UART2_SOUT/GPIO9	Transmit Data	P26	O	OV_{DD}	24
UART1_SIN/GPIO10	Receive Data	R26	I	OV_{DD}	24
UART2_SIN/GPIO11	Receive Data	P27	I	OV_{DD}	24
$\overline{\text{UART1\_RTS}}$/UART3_SOUT/GPIO12	Ready to Send	P24	O	OV_{DD}	24
$\overline{\text{UART2\_RTS}}$/UART4_SOUT/GPIO13	Ready to Send	P25	O	OV_{DD}	24
$\overline{\text{UART1\_CTS}}$/UART3_SIN/GPIO14	Clear to Send	R25	I	OV_{DD}	24
$\overline{\text{UART2\_CTS}}$/UART4_SIN/GPIO15	Clear to Send	P23	I	OV_{DD}	24
I^2C Interface					
IIC1_SCL	Serial Clock	AC25	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial Data	AC28	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial Clock	W25	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial Data	AA25	I/O	OV_{DD}	2, 14
IIC3_SCL/GPIO16/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/SDHC_CD	Serial Clock	AB23	I/O	OV_{DD}	2, 14

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_RX04	Receive Data (positive)	A2	I	XV_{DD}	—
SD_RX03	Receive Data (positive)	E1	I	XV_{DD}	—
SD_RX02	Receive Data (positive)	G1	I	XV_{DD}	—
$\overline{\text{SD\_RX13}}$	Receive Data (negative)	A21	I	XV_{DD}	—
$\overline{\text{SD\_RX12}}$	Receive Data (negative)	A19	I	XV_{DD}	—
$\overline{\text{SD\_RX11}}$	Receive Data (negative)	A15	I	XV_{DD}	—
$\overline{\text{SD\_RX10}}$	Receive Data (negative)	B13	I	XV_{DD}	—
$\overline{\text{SD\_RX07}}$	Receive Data (negative)	A11	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive Data (negative)	A9	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive Data (negative)	A7	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive Data (negative)	A3	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive Data (negative)	E2	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive Data (negative)	G2	I	XV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	D3	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes Bank 1 PLL Reference Clock Complement	D4	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	E17	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes Bank 2 PLL Reference Clock Complement	F17	I	XV_{DD}	—
General-Purpose Input/Output					
GPIO00/$\overline{\text{SPI\_CS0}}$/SDHC_DATA4	General Purpose Input/Output	H26	I/O	CV_{DD}	—
GPIO01/$\overline{\text{SPI\_CS1}}$/SDHC_DATA5	General Purpose Input/Output	H23	I/O	CV_{DD}	—
GPIO02/$\overline{\text{SPI\_CS2}}$/SDHC_DATA6	General Purpose Input/Output	H27	I/O	CV_{DD}	—
GPIO03$\overline{\text{SPI_CS3}}$/SDHC_DATA7	General Purpose Input/Output	H24	I/O	CV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input/Output	R23	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input/Output	P26	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input/Output	R26	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input/Output	P27	I/O	OV_{DD}	—
GPIO12/$\overline{\text{UART1\_RTS}}$/UART3_SOUT	General Purpose Input/Output	P24	I/O	OV_{DD}	—
GPIO13/$\overline{\text{UART2\_RTS}}$/UART4_SOUT	General Purpose Input/Output	P25	I/O	OV_{DD}	—
GPIO14/$\overline{\text{UART1\_CTS}}$/UART3_SIN	General Purpose Input/Output	R25	I/O	OV_{DD}	—
GPIO15/$\overline{\text{UART2\_CTS}}$/UART4_SIN	General Purpose Input/Output	P23	I/O	OV_{DD}	—
GPIO16/IIC3_SCL/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/$\overline{\text{SDHC\_CD}}$	General Purpose Input/Output	AB23	I/O	OV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GPIO17/IIC3_SDA/M1SRCID0/LB_SRCID0 / DMA1_DDONE0/SDHC_WP	General Purpose Input/Output	AB26	I/O	OV_{DD}	—
GPIO18/IIC4_SCL/EVT5/M1SRCID1/ LB_SRCID1/DMA1_DREQ0	General Purpose Input/Output	AC23	I/O	OV_{DD}	—
GPIO19/IIC4_SDA/EVT6/M1SRCID2/ LB_SRCID2	General Purpose Input/Output	V24	I/O	OV_{DD}	—
GPIO21/IRQ3/DMA2_DREQ0	General Purpose Input/Output	AA26	I/O	OV_{DD}	—
GPIO22/IRQ4/DMA2_DACK0	General Purpose Input/Output	V25	I/O	OV_{DD}	—
GPIO23/IRQ5/DMA2_DDONE0	General Purpose Input/Output	AA22	I/O	OV_{DD}	—
GPIO24/IRQ6/USB1_DRVVBUS	General Purpose Input/Output	Y26	I/O	OV_{DD}	—
GPIO25/IRQ7/USB1_PWRFAULT	General Purpose Input/Output	AA23	I/O	OV_{DD}	—
GPIO26/IRQ8/USB2_DRVVBUS	General Purpose Input/Output	AC22	I/O	OV_{DD}	—
GPIO27/IRQ9/USB2_PWRFAULT	General Purpose Input/Output	AC27	I/O	OV_{DD}	—
GPIO28/IRQ10/EVT7	General Purpose Input/Output	AB24	I/O	OV_{DD}	—
GPIO29/IRQ11/EVT8	General Purpose Input/Output	AC24	I/O	OV_{DD}	—
GPIO30/EC1_TXD1/TSEC_1588_ALARM_ OUT2	General Purpose Input/Output	C25	I/O	LV_{DD}	23
GPIO31/EC1_TXD3/TSEC_1588_PULSE_ OUT2	General Purpose Input/Output	A26	I/O	LV_{DD}	23
System Control					
PORESET	Power On Reset	T22	I	OV_{DD}	—
HRESET	Hard Reset	T23	I/O	OV_{DD}	1, 2
RESET_REQ	Reset Request	U28	O	OV_{DD}	31
CKSTP_OUT	Checkstop Out	T25	O	OV_{DD}	1, 2
Debug					
EVT0	Event 0	V26	I/O	OV_{DD}	18
EVT1	Event 1	U27	I/O	OV_{DD}	—
EVT2	Event 2	U26	I/O	OV_{DD}	—
EVT3	Event 3	W24	I/O	OV_{DD}	—
EVT4	Event 4	U24	I/O	OV_{DD}	—
EVT5/IIC4_SCL/M1SRCID1/LB_SRCID1/ GPIO18/DMA1_DREQ0	Event 5	AC23	I/O	OV_{DD}	—
EVT6/IIC4_SDA/M1SRCID2/ LB_SRCID2/GPIO19	Event 6	V24	I/O	OV_{DD}	—
EVT7GPIO28/IRQ10	Event 7	AB24	I/O	OV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND166	Ground	B25	—	—	—
GND165	Ground	C23	—	—	—
GND164	Ground	D23	—	—	—
GND163	Ground	D27	—	—	—
GND162	Ground	E24	—	—	—
GND161	Ground	F22	—	—	—
GND160	Ground	F27	—	—	—
GND159	Ground	G10	—	—	—
GND158	Ground	G12	—	—	—
GND157	Ground	G14	—	—	—
GND156	Ground	G16	—	—	—
GND155	Ground	G18	—	—	—
GND154	Ground	G21	—	—	—
GND153	Ground	G22	—	—	—
GND152	Ground	H3	—	—	—
GND151	Ground	H4	—	—	—
GND150	Ground	H10	—	—	—
GND149	Ground	H12	—	—	—
GND148	Ground	H14	—	—	—
GND147	Ground	H16	—	—	—
GND146	Ground	H18	—	—	—
GND145	Ground	H21	—	—	—
GND144	Ground	H25	—	—	—
GND143	Ground	J2	—	—	—
GND142	Ground	J8	—	—	—
GND141	Ground	J10	—	—	—
GND140	Ground	J12	—	—	—
GND139	Ground	J14	—	—	—
GND138	Ground	J16	—	—	—
GND137	Ground	J18	—	—	—
GND136	Ground	J21	—	—	—
GND135	Ground	K5	—	—	—
GND134	Ground	K8	—	—	—
GND133	Ground	K10	—	—	—

Table 2. Absolute Operating Conditions[1] (continued)

Parameter	Symbol	Max Value	Unit	Note

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. $(C,X,B,G,L,O)V_{IN}$ may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 7.
8. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
9. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
10. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Note
Core Group A (cores 0–1) and platform supply voltage (Silicon Rev 1.0)	$V_{DD\_CA\_PL}$	1.0 ± 50 mV	V	4, 5
Core Group B (cores 2–3) supply voltage (Silicon Rev 1.0)	V_{DD_CB}	1.0 ± 50 mV	V	4, 5
Core Group A (cores 0–1), Core Group B (cores 2–3) and platform supply voltage (Silicon Rev 1.1)	$V_{DD\_CA\_CB\_PL}$	1.0 ± 50 mV	V	4, 5
PLL supply voltage (core, platform, DDR)	AV_{DD}	1.0 ± 50 mV	V	—
PLL supply voltage (SerDes)	AV_{DD_SRDS}	1.0 ± 50 mV	V	—
Fuse programming override supply	POV_{DD}	1.5 ± 75 mV	V	2
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	3.3 ± 165 mV	V	—
eSPI, eSDHC, GPIO	CV_{DD}	3.3 ± 165 mV 2.5 ± 125 mV 1.8 ± 90 mV	V	—
DDR DRAM I/O voltage DDR3 DDR3L	GV_{DD}	 1.5 ± 75 mV 1.35 ± 67 mV	V	—

While VDD is ramping, current may be supplied from VDD through the chip to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

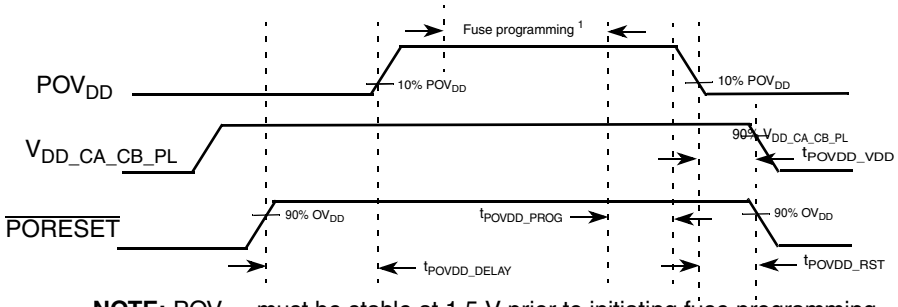
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to $V_{DD\_CA\_CB\_PL}$ ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before $V_{DD\_CA\_CB\_PL}$ is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{PORESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{PORESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply Power Default Setting."

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the $V_{DD\_CA\_CB\_PL}$ supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power Up Sequencing," it is required that POV_{DD} = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5.

$V_{DD\_CA\_CB\_PL}$ and USB_V_{DD}_1P0 must be ramped down simultaneously. USB_V_{DD}_1P8_DECAP should starts ramping down only after USB_V_{DD}_3P3 is below 1.65 V.

2.4 Power Characteristics

This table shows the power dissipations of the $V_{DD\_CA\_CB\_PL}$ supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 6. Device Power Dissipation

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	1200	600	1200	500	1.0	65	10.3	—	9.8	—	—	2, 3
Thermal						105	14.2	—	13.8	—	—	5, 7
Maximum							14.8	13.5	14.0	12.8	1.4	4, 6, 7
Typical	1000	533	1067	467	1.0	65	9.2	—	8.6	—	—	2, 3
Thermal						105	12.5	—	12.1	—	—	5, 7
Maximum							13.0	11.7	12.3	11.0	1.4	4, 6, 7
Typical	800	534	1067	467	1.0	65	9.0	—	8.4	—	—	2, 3
Thermal						105	12.2	—	12.0	—	—	5, 7
Maximum							12.6	11.4	12.1	10.9	1.4	4, 6, 7

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the device PLLs, at allowable voltage levels.

Table 8. Device AV_{DD} Power Dissipation

AV_{DD}s	Typical	Maximum	Unit	Note
AV_{DD_DDR}	5	15	mW	1
AV_{DD_CC1}				
AV_{DD_CC2}				
AV_{DD_PLAT}				
AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}				
USB_V_{DD_1P0}	—	10	mW	3

Note:

1. $V_{DD\_CA\_CB\_PL}$, T_A = 80°C, T_J = 105°C
2. SV_{DD} = 1.0 V, T_A = 80°C, T_J = 105°C
3. USB_V_{DD_1P0} = 1.0V, T_A = 80°C, T_J = 105°C

This table shows the estimated power dissipation on the POV_{DD} supply for the chip at allowable voltage levels.

Table 9. POV_{DD} Power Dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the device, at allowable voltage levels.

Table 10. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Notes
V_{DD_LP} (Device on, 105C)	1.5	mW	1
V_{DD_LP} (Device off, 70C)	195	uW	2
V_{DD_LP} (Device off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When the device is off, V_{DD_LP} may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC, which switches V_{DD_LP} to battery when the SoC is powered down. See the Trust Architecture chapter in the device reference manual for more information.

2.5 Thermal

Table 11. Package Thermal Characteristics [6]

Rating	Board	Symbol	Value	Unit	Note
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	21	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	15	°C/W	1, 3

2.10 eSPI

This section describes the DC and AC electrical specifications for the eSPI interface.

2.10.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 3.3 V.

Table 30. eSPI DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 2.5 V.

Table 31. eSPI DC Electrical Characteristics (CV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 32. eSPI DC Electrical Characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1

Table 50. eSDHC Interface DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output low voltage	V_{OL}	I_{OL} = 100μA at CV_{DD} min	—	0.125 × CV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at CV_{DD} min	CV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA at CV_{DD} min	—	0.3	V	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.15.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in Figure 23 and Figure 24.

Table 51. eSDHC AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency: SD/SDIO full-speed/high-speed mode MMC full-speed/high-speed mode	f_{SHSCK}	 0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—full-speed/high-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—full-speed/high-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	—	ns	4
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3,4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	-3	3	ns	4

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–50 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
3. To satisfy setup timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

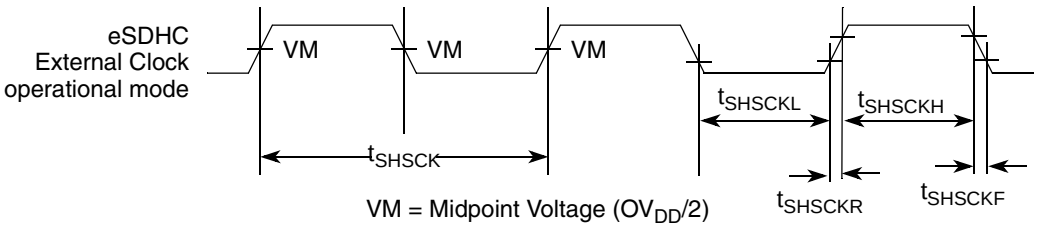


Figure 23. eSDHC Clock Input Timing Diagram

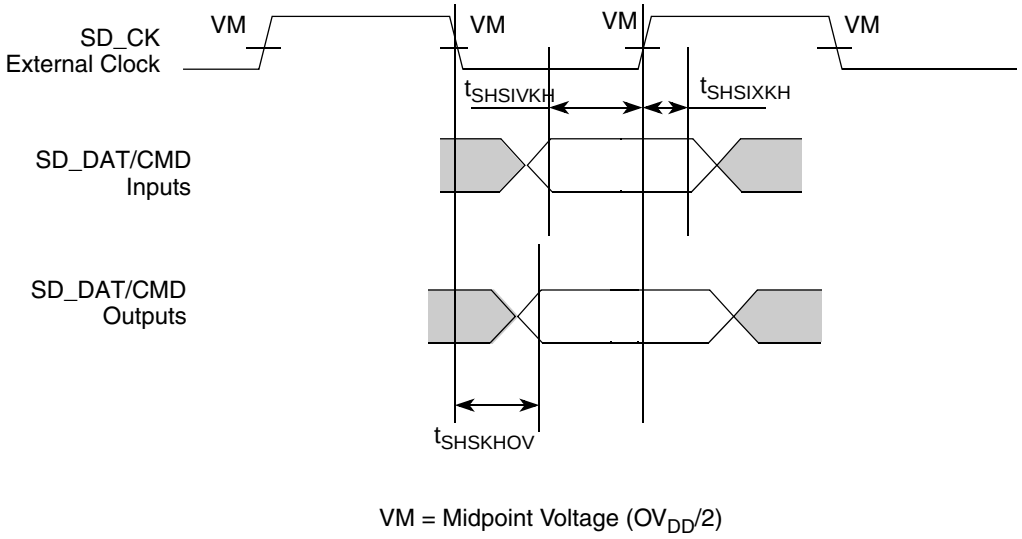


Figure 24. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.16 Multicore Programmable Interrupt Controller (MPIC) Specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC DC specifications

This table provides the DC electrical characteristics for the MPIC interface.

Table 52. MPIC DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Table 62. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 63. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	—	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.4.4 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

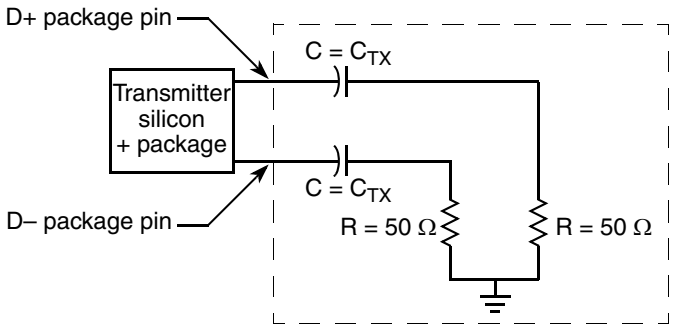


Figure 46. SGMII AC Test/Measurement Load

2.20.8.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 92. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Note:
1. Measured at receiver
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 System Clocking

This section describes the PLL configuration of the device.

This device includes six PLLs, as follows:

- There are two selectable core cluster PLLs that generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL; core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3,

3.1.6 Frequency Options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and Platform Frequency Options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 100. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	66.66	83.33	100.00	111.11	133.33
	Platform Frequency (MHz)[1]				
4:1					533
5:1				555	
6:1			600		
7:1		583			
8:1	533				

[1] Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 47. Gen 1 PCI Express Minimum Platform Frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 48. Gen 2 PCI Express Minimum Platform Frequency

See Section 18.1.3.2, “Link Width,” in the chip reference manual for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width of the single widest port used (not combined width of the number ports used) as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times 0.8512 \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

Figure 49. sRIO Minimum Platform Frequency

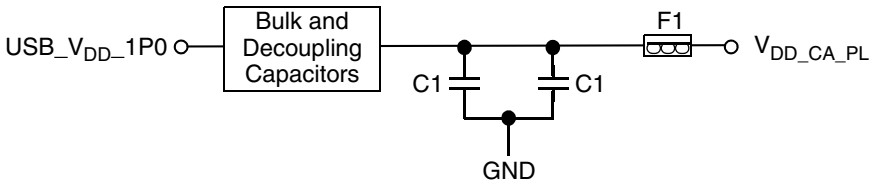


Figure 53. USB_V_{DD}_1P0 Power Supply Filter Circuit

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip's system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

3.5 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a 1-µF ceramic chip capacitor on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND pins of the device.

The Ethernet controllers 1 and/or 2 input pins may be disabled by setting their respective RCW configuration field EC1 (bits 360–361) and EC2 (bits 363–364) to 0b11 = No parallel mode Ethernet. When disabled, these inputs do not need to be externally pulled to an appropriate signal level.

3.6.2 Aurora Configuration Signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in Figure 56 and Figure 57. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Freescale recommends that the Aurora 22 pin duplex connector be designed into the system as shown in Figure 58 or the 70 pin duplex connector be designed into the system as shown in Figure 59.

If the Aurora interface is not used, Freescale recommends the legacy COP header be designed into the system as described in Section 3.6.1.1, "Termination of Unused Signals."

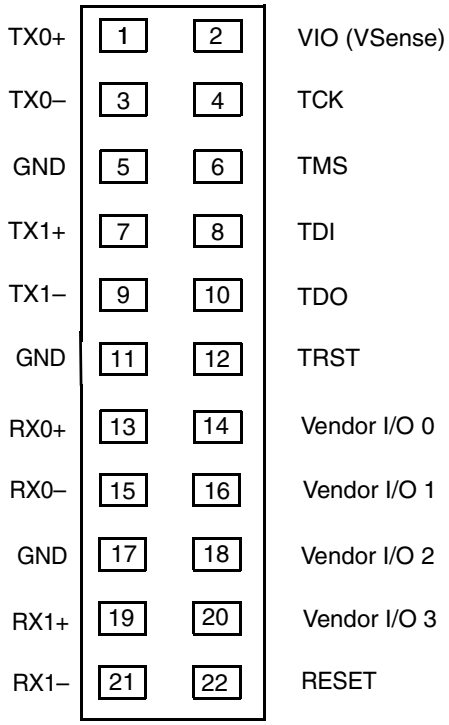
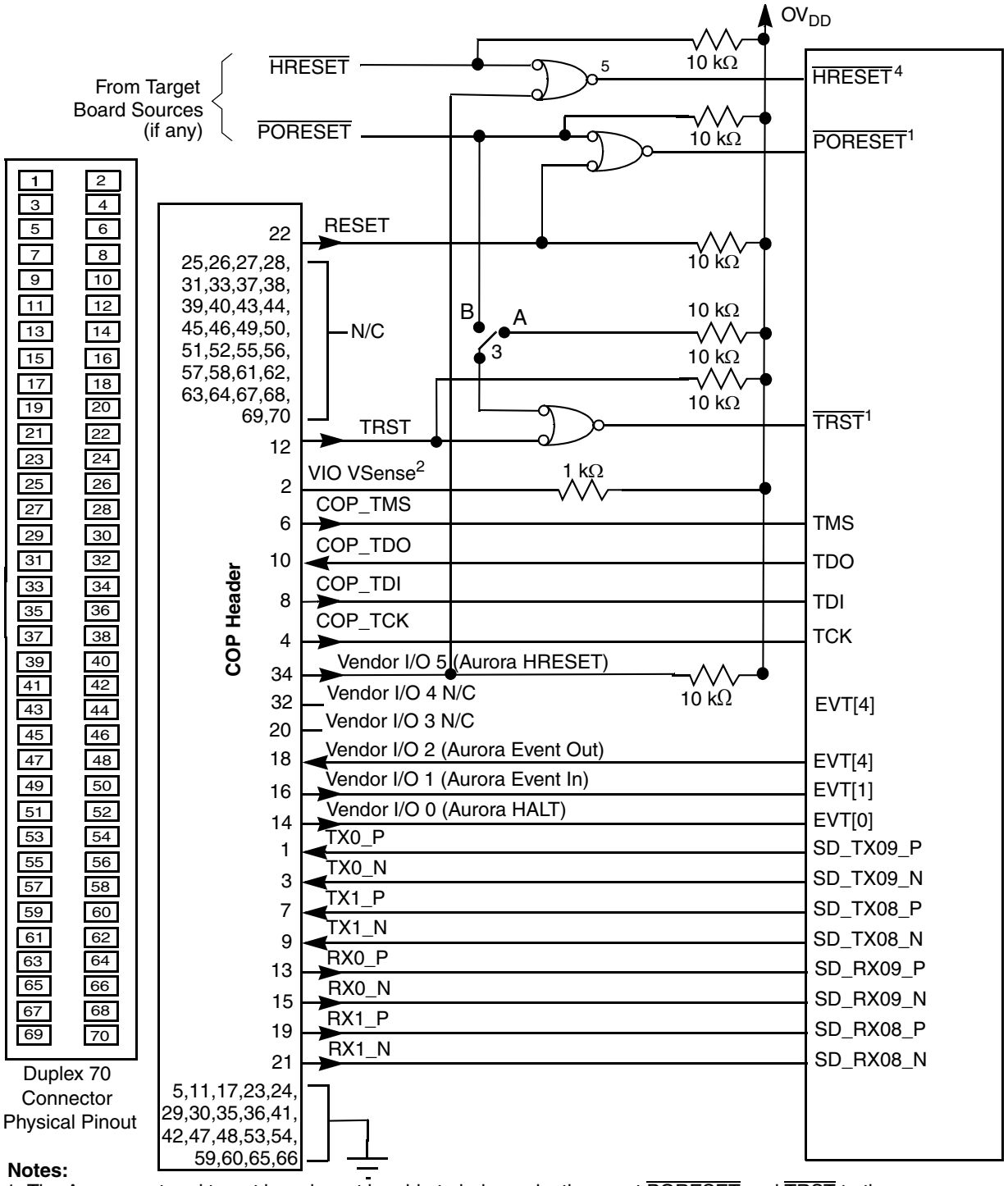


Figure 56. Aurora 22 Pin Connector Duplex Pinout



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.
5. This is an open-drain gate.

Figure 59. Aurora 70 Pin Connector Duplex Interface Connection

Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
P2040NSE1FLB P2040NSE7FLC	P	2	04 = 4 core	1	N = Industrial qualification	S = Std temp	E = SEC present	1= FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	F = 667 MHz	L = 1067 MT/s	B C
P2040NSN1FLB P2040NSN7FLC							N = SEC not present				
P2040NSE1HLB P2040NSE7HLC							E = SEC present		H = 800 MHz		
P2040NSN1HLB P2040NSN7HLC							N = SEC not present				
P2040NSE1KLB P2040NSE7KLC							E = SEC Present		K = 1000 MHz		
P2040NSN1KLB P2040NSN7KLC							N = SEC not present				
P2040NSE1MMB P2040NSE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NSN1MMB P2040NSN7MMC							N = SEC not present				
P2040NXE1FLB P2040NXE7FLC						X = Extended temp	E = SEC Present		F = 667 MHz	L = 1067 MT/s	
P2040NXN1FLB P2040NXN7FLC							N = SEC not present				
P2040NXE1MMB P2040NXE7MMC							E = SEC Present		M = 1200 MHz	M = 1200 MT/s	
P2040NXN1MMB P2040NXN7MMC							N = SEC not present				