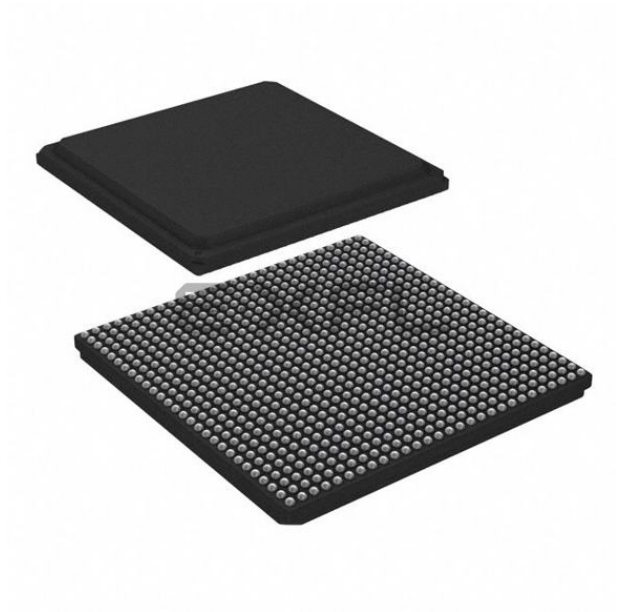

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Security; SEC 4.2
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator, Secure Fusebox
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2041nxe1pnb

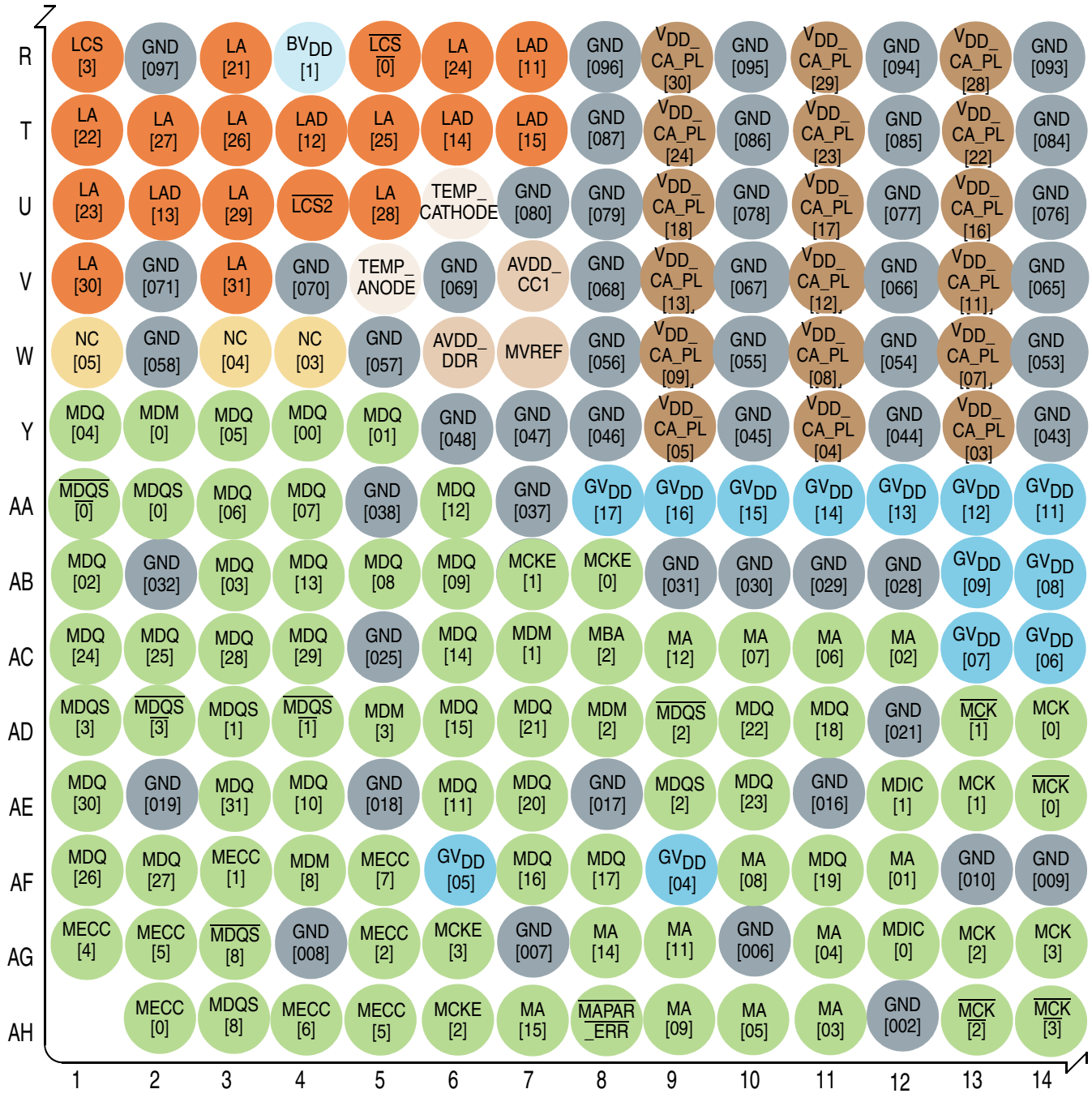


Figure 5. 780 BGA Ball Map Diagram (Detail View C)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ29	Data	AC4	I/O	GV_{DD}	—
MDQ30	Data	AE1	I/O	GV_{DD}	—
MDQ31	Data	AE3	I/O	GV_{DD}	—
MDQ32	Data	AE16	I/O	GV_{DD}	—
MDQ33	Data	AD16	I/O	GV_{DD}	—
MDQ34	Data	AE19	I/O	GV_{DD}	—
MDQ35	Data	AD19	I/O	GV_{DD}	—
MDQ36	Data	AF15	I/O	GV_{DD}	—
MDQ37	Data	AF16	I/O	GV_{DD}	—
MDQ38	Data	AF18	I/O	GV_{DD}	—
MDQ39	Data	AF19	I/O	GV_{DD}	—
MDQ40	Data	AH23	I/O	GV_{DD}	—
MDQ41	Data	AG23	I/O	GV_{DD}	—
MDQ42	Data	AH27	I/O	GV_{DD}	—
MDQ43	Data	AG27	I/O	GV_{DD}	—
MDQ44	Data	AG21	I/O	GV_{DD}	—
MDQ45	Data	AH22	I/O	GV_{DD}	—
MDQ46	Data	AH26	I/O	GV_{DD}	—
MDQ47	Data	AG26	I/O	GV_{DD}	—
MDQ48	Data	AF21	I/O	GV_{DD}	—
MDQ49	Data	AD21	I/O	GV_{DD}	—
MDQ50	Data	AF24	I/O	GV_{DD}	—
MDQ51	Data	AD24	I/O	GV_{DD}	—
MDQ52	Data	AE20	I/O	GV_{DD}	—
MDQ53	Data	AD20	I/O	GV_{DD}	—
MDQ54	Data	AD23	I/O	GV_{DD}	—
MDQ55	Data	AE25	I/O	GV_{DD}	—
MDQ56	Data	AF26	I/O	GV_{DD}	—
MDQ57	Data	AF27	I/O	GV_{DD}	—
MDQ58	Data	AD25	I/O	GV_{DD}	—
MDQ59	Data	AD26	I/O	GV_{DD}	—
MDQ60	Data	AG28	I/O	GV_{DD}	—
MDQ61	Data	AF25	I/O	GV_{DD}	—
MDQ62	Data	AD27	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND166	Ground	B25	—	—	—
GND165	Ground	C23	—	—	—
GND164	Ground	D23	—	—	—
GND163	Ground	D27	—	—	—
GND162	Ground	E24	—	—	—
GND161	Ground	F22	—	—	—
GND160	Ground	F27	—	—	—
GND159	Ground	G10	—	—	—
GND158	Ground	G12	—	—	—
GND157	Ground	G14	—	—	—
GND156	Ground	G16	—	—	—
GND155	Ground	G18	—	—	—
GND154	Ground	G21	—	—	—
GND153	Ground	G22	—	—	—
GND152	Ground	H3	—	—	—
GND151	Ground	H4	—	—	—
GND150	Ground	H10	—	—	—
GND149	Ground	H12	—	—	—
GND148	Ground	H14	—	—	—
GND147	Ground	H16	—	—	—
GND146	Ground	H18	—	—	—
GND145	Ground	H21	—	—	—
GND144	Ground	H25	—	—	—
GND143	Ground	J2	—	—	—
GND142	Ground	J8	—	—	—
GND141	Ground	J10	—	—	—
GND140	Ground	J12	—	—	—
GND139	Ground	J14	—	—	—
GND138	Ground	J16	—	—	—
GND137	Ground	J18	—	—	—
GND136	Ground	J21	—	—	—
GND135	Ground	K5	—	—	—
GND134	Ground	K8	—	—	—
GND133	Ground	K10	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND030	Ground	AB10	—	—	—
GND029	Ground	AB11	—	—	—
GND028	Ground	AB12	—	—	—
GND027	Ground	AB15	—	—	—
GND026	Ground	AB22	—	—	—
GND025	Ground	AC5	—	—	—
GND024	Ground	AC17	—	—	—
GND023	Ground	AC20	—	—	—
GND022	Ground	AC26	—	—	—
GND021	Ground	AD12	—	—	—
GND020	Ground	AD15	—	—	—
GND019	Ground	AE2	—	—	—
GND018	Ground	AE5	—	—	—
GND017	Ground	AE8	—	—	—
GND016	Ground	AE11	—	—	—
GND015	Ground	AE15	—	—	—
GND014	Ground	AE18	—	—	—
GND013	Ground	AE21	—	—	—
GND012	Ground	AE24	—	—	—
GND011	Ground	AE27	—	—	—
GND010	Ground	AF13	—	—	—
GND009	Ground	AF14	—	—	—
GND008	Ground	AG4	—	—	—
GND007	Ground	AG7	—	—	—
GND006	Ground	AG10	—	—	—
GND005	Ground	AG19	—	—	—
GND004	Ground	AG22	—	—	—
GND003	Ground	AG25	—	—	—
GND002	Ground	AH12	—	—	—
GND001	Ground	AH15	—	—	—
XGND12	SerDes Transceiver GND	C5	—	—	—
XGND11	SerDes Transceiver GND	C7	—	—	—
XGND10	SerDes Transceiver GND	C11	—	—	—
XGND09	SerDes Transceiver GND	C15	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_CA_PL50	Core Group A and Platform Supply	L17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL49	Core Group A and Platform Supply	L19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL48	Core Group A and Platform Supply	M9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL47	Core Group A and Platform Supply	M11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL46	Core Group A and Platform Supply	M13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL45	Core Group A and Platform Supply	M15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL44	Core Group A and Platform Supply	M17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL43	Core Group A and Platform Supply	M19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL42	Core Group A and Platform Supply	N9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL41	Core Group A and Platform Supply	N11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL40	Core Group A and Platform Supply	N13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL39	Core Group A and Platform Supply	N15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL38	Core Group A and Platform Supply	N17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL37	Core Group A and Platform Supply	N19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL36	Core Group A and Platform Supply	P9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL35	Core Group A and Platform Supply	P11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL34	Core Group A and Platform Supply	P13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL33	Core Group A and Platform Supply	P15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL32	Core Group A and Platform Supply	P17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL31	Core Group A and Platform Supply	P19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL30	Core Group A and Platform Supply	R9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL29	Core Group A and Platform Supply	R11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL28	Core Group A and Platform Supply	R13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL27	Core Group A and Platform Supply	R15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL26	Core Group A and Platform Supply	R17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL25	Core Group A and Platform Supply	R19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL24	Core Group A and Platform Supply	T9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL23	Core Group A and Platform Supply	T11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL22	Core Group A and Platform Supply	T13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL21	Core Group A and Platform Supply	T15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL20	Core Group A and Platform Supply	T17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL19	Core Group A and Platform Supply	T19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL18	Core Group A and Platform Supply	U9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL17	Core Group A and Platform Supply	U11	—	$V_{DD\_CA\_PL}$	37

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
Reserve	—	AB20	—	GND	19

Note:

1. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD} in order to ensure no random chip select assertion due to possible noise, etc.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the corresponding power and ground nets internally. They may be connected as a differential pair to be used by the voltage regulators with remote sense function. For Rev1.1 silicon, the better solution is to use the far sense pins relative to the power supply location, the other pair can be left as no connected. The DC power simulation should be done during the board layout process to approve the selected solution.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
10. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
11. Do not connect.
12. These are test signals for factory use only and must be pulled low (1 KΩ–2 kΩ) to ground (GND) for normal machine operation.
13. Independent supplies derived from board $V_{DD\_CA\_CB\_PL}$ (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD} if I^2C interface is used.
15. This pin requires an external 1 KΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
17. These pins must be pulled up to 1.2 V through a 180 $\Omega \pm 1\%$ resistor for EM2_MDC and a 330 $\Omega \pm 1\%$ resistor for EM2_MDIO.
18. Pin has a weak internal pull-up.
19. These pins must be pulled to ground (GND).
20. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
21. This pin requires a 200-Ω pull-up to XV_{DD}.
22. This pin requires a 200-Ω pull-up to SV_{DD}.
23. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
24. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
25. See Section 3.6, "Connection Recommendations," for additional details on this signal.

Table 2. Absolute Operating Conditions[1] (continued)

Parameter		Symbol	Max Value	Unit	Note
eSPI, eSHDC, GPIO		CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
DDR3 and DDR3L DRAM I/O voltage		GV_{DD}	–0.3 to 1.65	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
SerDes core logic supply and receivers		SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	—
Ethernet I/O, Ethernet management interface 1 (EMI1), 1588, GPIO		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3
USB PHY transceiver supply voltage		$USB\_V_{DD}\_3P3$	–0.3 to 3.63	V	—
USB PHY PLL supply voltage		$USB\_V_{DD}\_1P0$	–0.3 to 1.1	V	—
Low Power Security Monitor Supply		V_{DD_LP}	–0.3 to 1.1	V	—
Input voltage[7]	DDR3 and DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 7
	DDR3 and DDR3L DRAM reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2+ 0.3)	V	2, 7
	Ethernet signals, GPIO	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 7
	eSPI, eSHDC, GPIO	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 7
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	5, 7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6, 7
	SerDes signals	XV_{IN}	–0.4 to (XV_{DD} + 0.3)	V	7
	USB PHY transceiver signals	$USB\_V_{IN}\_3P3$	–0.3 to ($USB\_V_{DD}\_3P3$ + 0.3)	V	7
Storage junction temperature range		T_{stg}	–55 to 150	°C	—

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

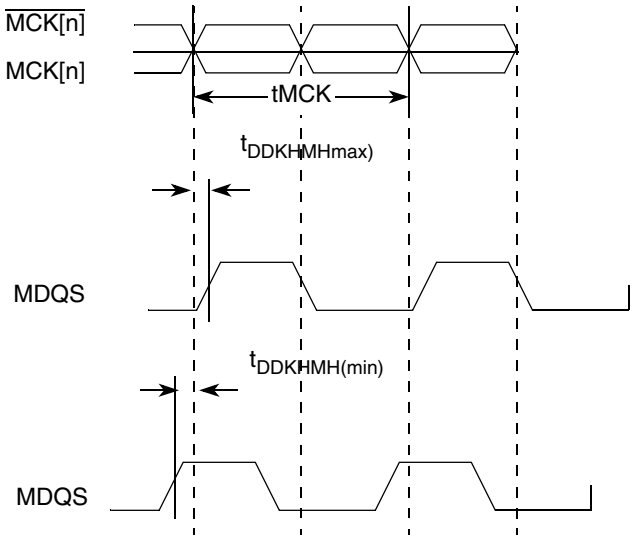


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

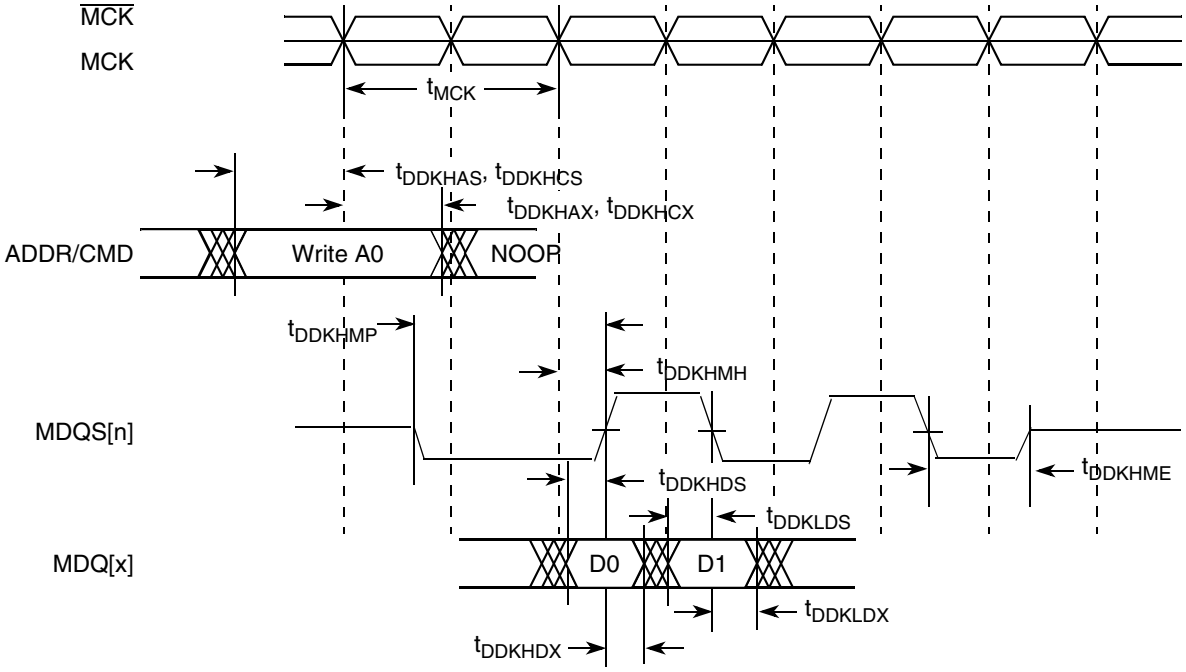


Figure 11. DDR3 and DDR3L Output Timing Diagram

Table 32. eSPI DC Electrical Characteristics (CV_{DD} = 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.10.2 eSPI AC Timing Specifications

This table provides the eSPI input and output AC timing specifications.

Table 33. eSPI AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	2 + ($t_{PLATFORM\_CLK}$*SPMODE[HO_ADJ])	— —	ns	2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV} t_{NIKHOV}	—	5.68+($t_{PLATFORM\_CLK}$*SPMODE[HO_ADJ])	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	7	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. The greater of the two output timings for t_{NIKHOX} and t_{NIKHOV} are used when SPCOM[RxDelay] of the eSPI command register is set. For example, the t_{NIKHOX} is 4.0 and t_{NIKHOV} is 7.0 if SPCOM[RxDelay] is set to be 1.

This figure provides the AC test load for the eSPI.

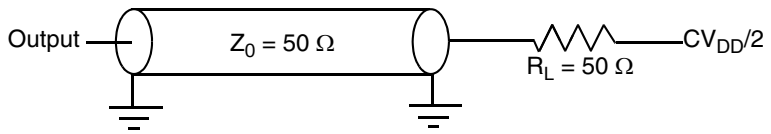


Figure 14. eSPI AC Test Load

Table 40. Ethernet Management Interface AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the frame manager clock period.

This figure shows the Ethernet management interface timing diagram

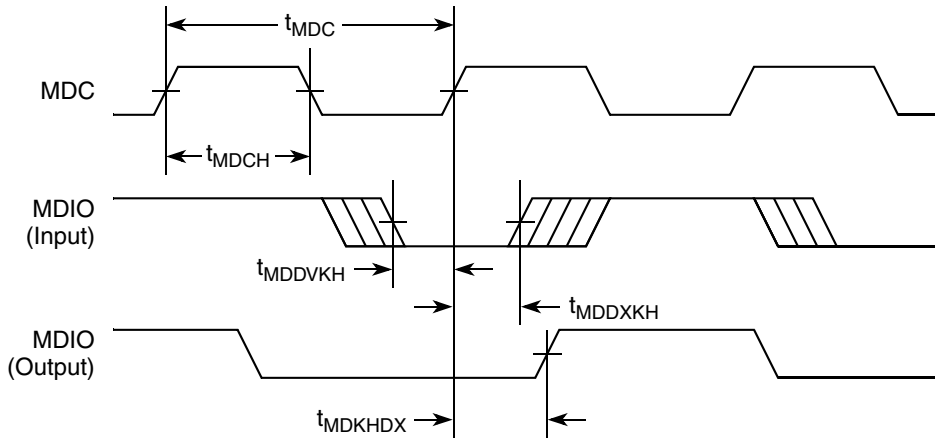


Figure 17. Ethernet Management Interface Timing Diagram

2.12.4 eTSEC IEEE Std 1588 DC Specifications

This table shows the eTSEC IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 3.3 V supply.

Table 41. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—

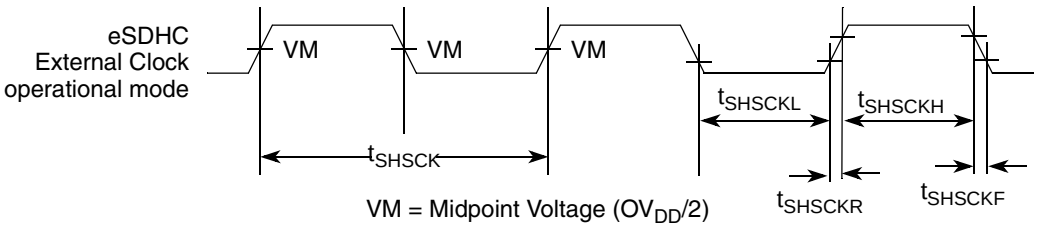


Figure 23. eSDHC Clock Input Timing Diagram

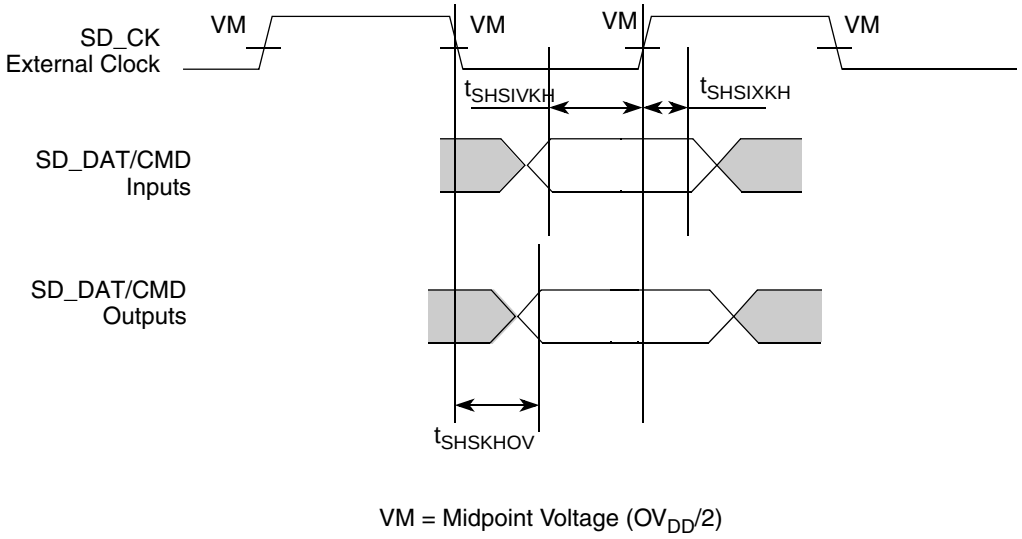


Figure 24. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.16 Multicore Programmable Interrupt Controller (MPIC) Specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC DC specifications

This table provides the DC electrical characteristics for the MPIC interface.

Table 52. MPIC DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). This figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

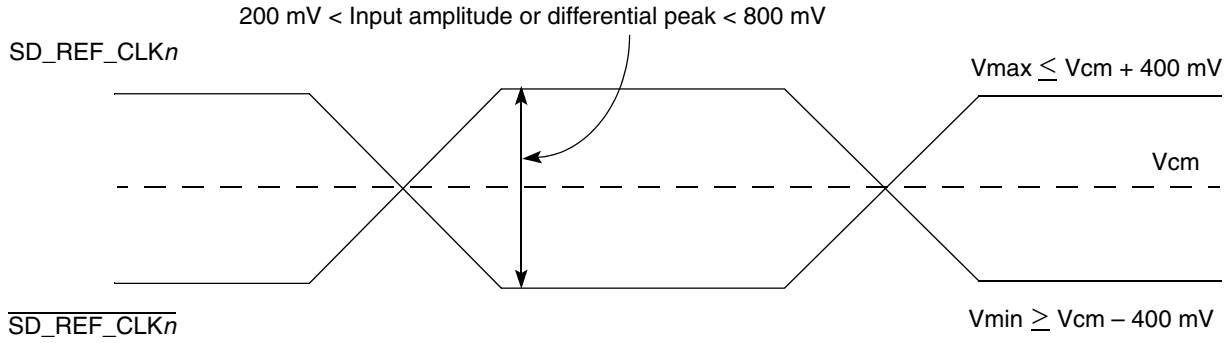


Figure 35. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SD_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}n}$ either left unconnected or tied to ground.
  — The SD_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}n}$) through the same source impedance as the clock input (SD_REF_CLK*n*) in use.

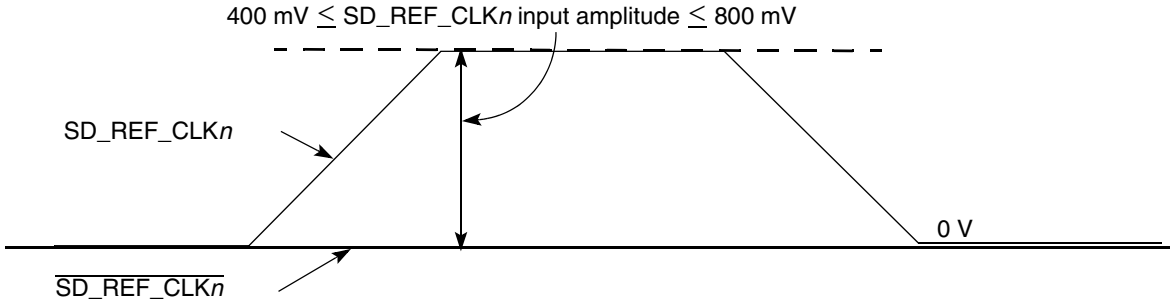


Figure 36. Single-Ended Reference Clock Input DC Requirements

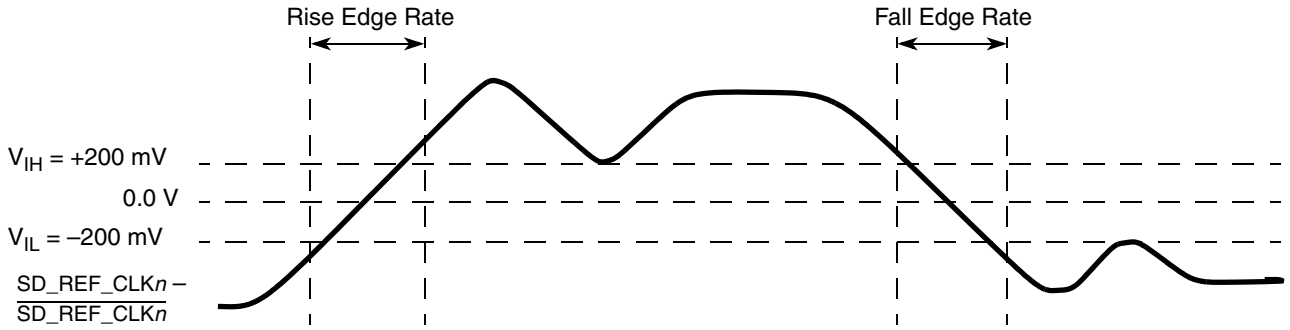


Figure 37. Differential Measurement Points for Rise and Fall Time

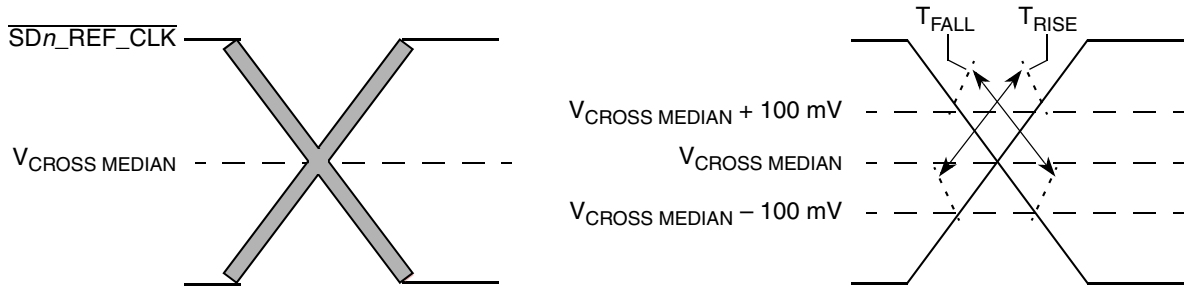


Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 Spread Spectrum Clock

SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

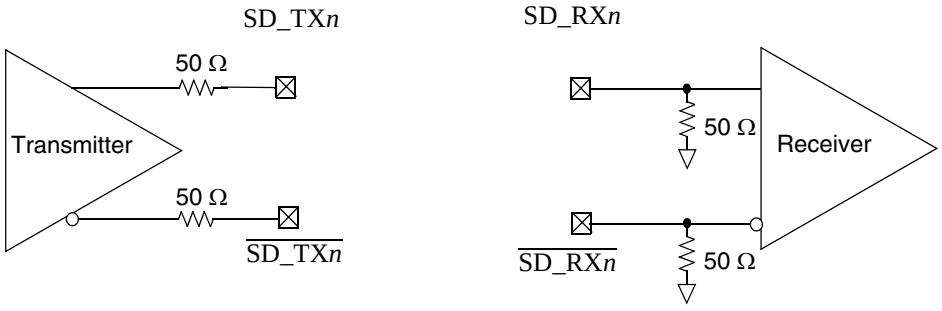


Figure 39. SerDes Transmitter and Receiver Reference Circuits

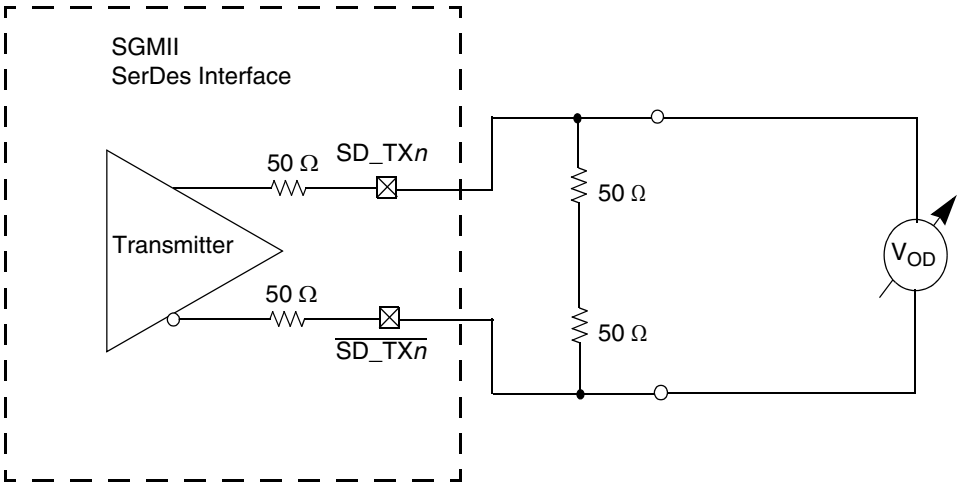


Figure 45. SGMII Transmitter DC Measurement Circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 88. SGMII 2.5x Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Output voltage	V_O	–0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—

Note:
1. Absolute output voltage limit

2.20.8.1.2 SGMII DC Receiver Electrical Characteristics

This table lists the SGMII DC receiver electrical characteristics for 1.25 GBaud. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 89. SGMII DC Receiver Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Typ	Max	Unit	Note
DC Input voltage range		—		N/A		—	1
Input differential voltage	REIDL_CTL = 001xx	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	REIDL_CTL = 100xx		175	—			
Loss of signal threshold	REIDL_CTL = 001xx	V_{LOS}	30	—	100	mV	3, 4
	REIDL_CTL = 100xx		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Table 89. SGMII DC Receiver Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 2.20.4.4, "PCI Express DC Physical Layer Receiver Specifications," and Section 2.20.4.5.2, "PCI Express AC Physical Layer Receiver Specifications," for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1–3)GCR(lane)1[REIDL_CTL] bit field.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 90. SGMII 2.5x Receiver DC Timing Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:
1. Measured at the receiver.

2.20.8.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.20.8.2.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 91. SGMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	1
Unit interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	—
Unit interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
AC coupling capacitor	C_{TX}	10		200	nF	2

Note:
1. See Figure 42 for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.20.8.2.2 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$) respectively, as depicted in this figure.

Table 98. Asynchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:SYSCLK Ratio	Set MEM_PLL_CFG = 01 for SYSCLK Freq[1]
0_0101	5:1	>96.7 MHz
0_0110	6:1	>80.6 MHz
0_1000	8:1	>120.9 MHz
0_1001	9:1	>107.4 MHz
0_1010	10:1	>96.7 MHz
0_1100	12:1	>80.6 MHz
0_1101	13:1	>74.4 MHz
1_0000	16:1	>60.4 MHz
1_0010	18:1	>53.7 MHz
All Others	Reserved	—

Note:

1. Set RCW field MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock (SYSCLK) frequency is greater than the given cutoff; otherwise, set to 0b00 for a frequency that is less than or equal to the cutoff.

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 99. Synchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:Platform CLK Ratio	Set MEM_PLL_CFG=01 for Platform CLK Freq[1]
0_0001	1:1	>600 MHz
All Others	Reserved	—

Note:

1. Set MEM_PLL_CFG=0b01 if the applied DDR PLL reference clock (Platform clock) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

3.1.6 Frequency Options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and Platform Frequency Options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 100. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	66.66	83.33	100.00	111.11	133.33
	Platform Frequency (MHz)[1]				
4:1					533
5:1				555	
6:1			600		
7:1		583			
8:1	533				

[1] Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 47. Gen 1 PCI Express Minimum Platform Frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 48. Gen 2 PCI Express Minimum Platform Frequency

See Section 18.1.3.2, “Link Width,” in the chip reference manual for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width of the single widest port used (not combined width of the number ports used) as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times 0.8512 \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

Figure 49. sRIO Minimum Platform Frequency

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW clocking configuration fields FM_CLK_SEL.

Table 104. Frame Manager Clock Select

Binary Value of FM_CLK_SEL	FM Frequency
0b0	Platform Clock Frequency /2
0b1	Core Cluster 2 Frequency /2[1]

Notes:

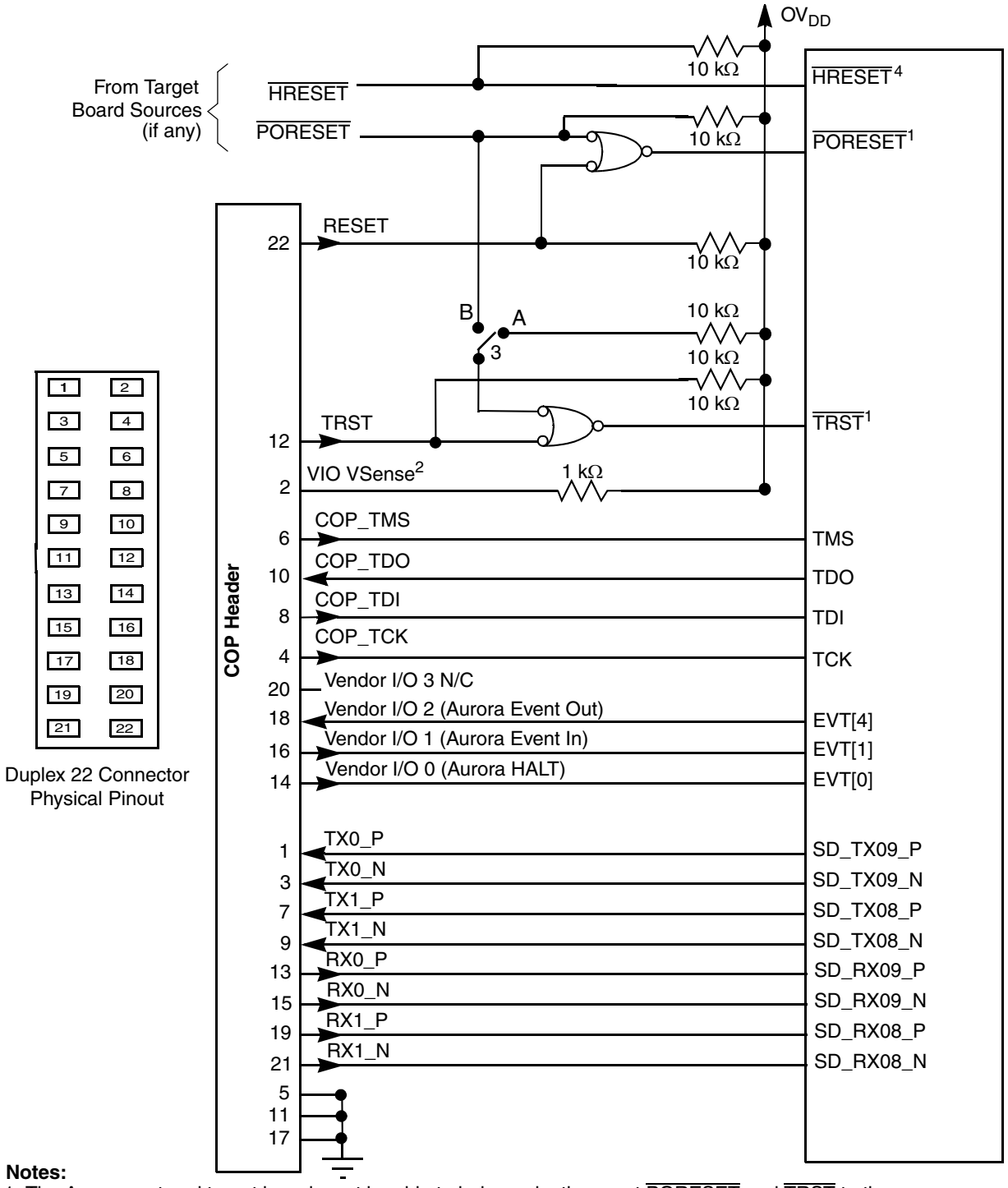
1 For asynchronous mode, max frequency, see Table 93.

3.2 Supply Power Default Setting

The device is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in Table 105, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device. $\overline{\text{HRESET}}$ is not used by the Aurora 22 pin connector.

Figure 58. Aurora 22 Pin Connector Duplex Interface Connection

and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 61. The heat sink must be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

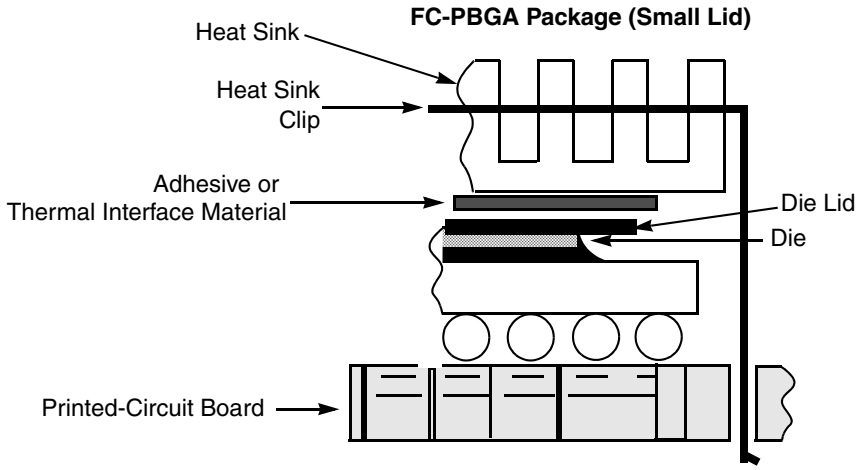


Figure 61. Package Exploded Cross-Sectional View—FC-PBGA (w/ Lid) Package

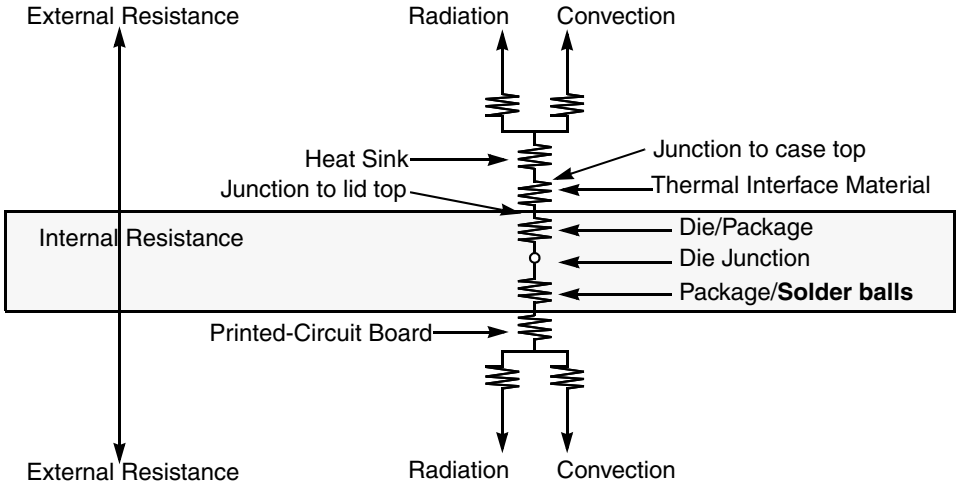
The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

Figure 62 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 62. Package with Heat Sink Mounted to a Printed-Circuit Board