Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Security; SEC 4.2
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator, Secure Fusebox
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2041nxe7mmc

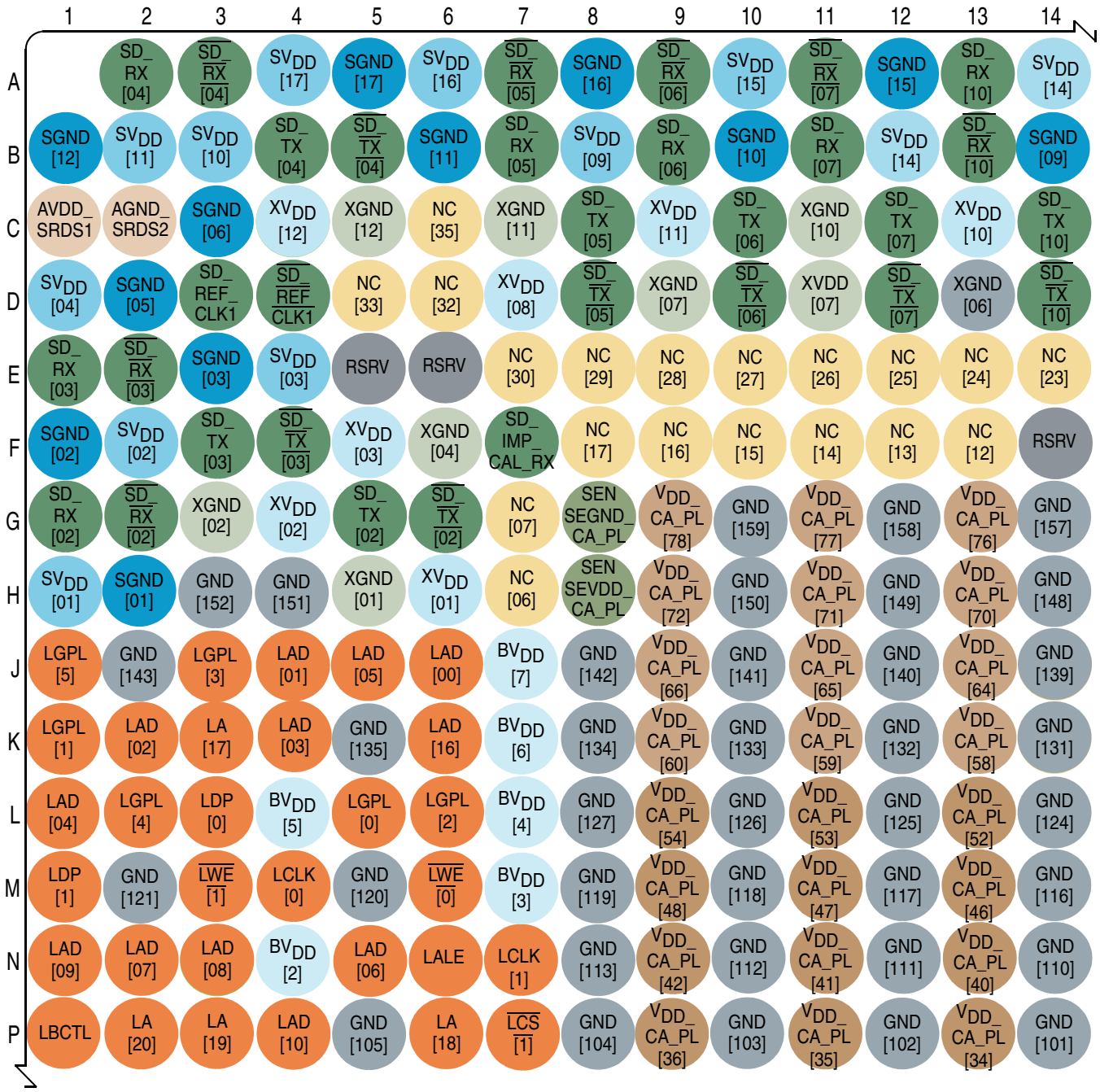


Figure 3. 780 BGA Ball Map Diagram (Detail View A)

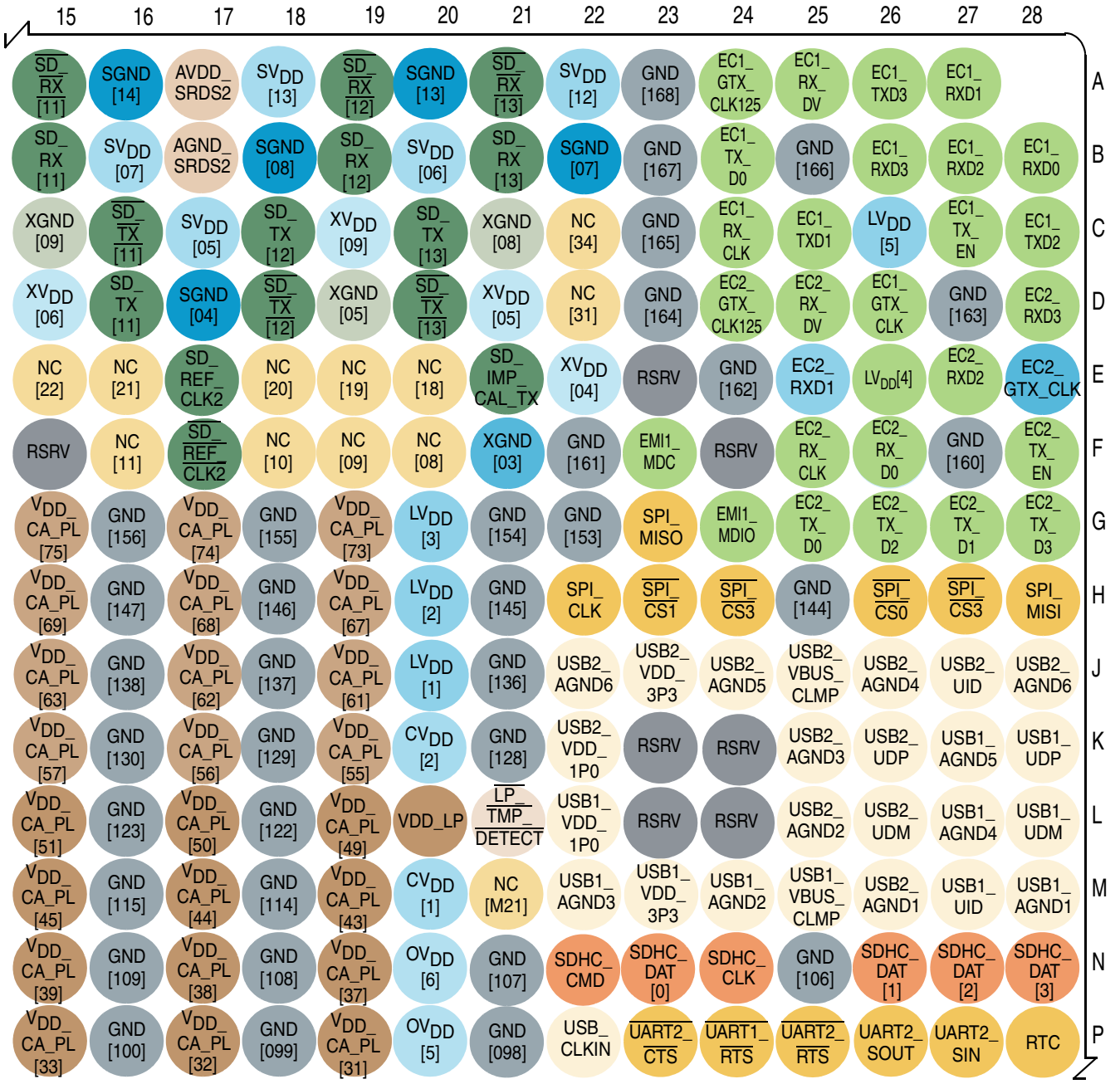


Figure 4. 780 BGA Ball Map Diagram (Detail View B)

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IRQ05/GPIO23/DMA2_DDONE0	External Interrupts	AA22	I	OV_{DD}	24
IRQ06/GPIO24/USB1_DRVVBUS	External Interrupts	Y26	I	OV_{DD}	24
IRQ07/GPIO25/USB1_PWRFAULT	External Interrupts	AA23	I	OV_{DD}	24
IRQ08/GPIO26/USB2_DRVVBUS	External Interrupts	AC22	I	OV_{DD}	24
IRQ09/GPIO27/USB2_PWRFAULT	External Interrupts	AC27	I	OV_{DD}	24
IRQ10/GPIO28/EVT7	External Interrupts	AB24	I	OV_{DD}	24
IRQ11/GPIO29/EVT8	External Interrupts	AC24	I	OV_{DD}	24
IRQ_OUT/EVT9	Interrupt Output	Y24	O	OV_{DD}	1, 2, 24
Trust					
TMP_DETECT	Tamper Detect	T24	I	OV_{DD}	25
LP_TMP_DETECT	Low Power Tamper Detect	L21	I	V_{DD_LP}	25
eSDHC					
SDHC_CMD	Command/Response	N22	I/O	CV_{DD}	—
SDHC_DAT0	Data	N23	I/O	CV_{DD}	—
SDHC_DAT1	Data	N26	I/O	CV_{DD}	—
SDHC_DAT2	Data	N27	I/O	CV_{DD}	—
SDHC_DAT3	Data	N28	I/O	CV_{DD}	—
SDHC_DAT4/SPI_CS0/GPIO00	Data	H26	I/O	CV_{DD}	24, 28
SDHC_DAT5/SPI_CS1/GPIO01	Data	H23	I/O	CV_{DD}	24, 28
SDHC_DAT6/SPI_CS2/GPIO02	Data	H27	I/O	CV_{DD}	24, 28
SDHC_DAT7/SPI_CS3/GPIO03	Data	H24	I/O	CV_{DD}	24, 28
SDHC_CLK	Host to Card Clock	N24	O	OV_{DD}	—
SDHC_CD/IIC3_SCL/GPIO16/ M1DVAL/LB_DVAL/DMA1_DACK0	Card Detection	AB23	I/O	OV_{DD}	24, 28
SDHC_WP/IIC3_SDA/GPIO17/ M1SRCID0/LB_SRCID0/DMA1_DDONE0	Card Write Protection	AB26	I	OV_{DD}	24, 28
eSPI					
SPI_MOSI	Master Out Slave In	H28	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	G23	I	CV_{DD}	—
SPI_CLK	eSPI Clock	H22	O	CV_{DD}	—
SPI_CS0/SDHC_DAT4/GPIO00	eSPI Chip Select	H26	O	CV_{DD}	24
SPI_CS1/SDHC_DAT5/GPIO01	eSPI Chip Select	H23	O	CV_{DD}	24
SPI_CS2/SDHC_DAT6/GPIO02	eSPI Chip Select	H27	O	CV_{DD}	24
SPI_CS3/SDHC_DAT7/GPIO03	eSPI Chip Select	H24	O	CV_{DD}	24

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0 / DMA1_DDONE0/SDHC_WP	Serial Data	AB26	I/O	OV_{DD}	2, 14
IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/ GPIO18/DMA1_DREQ0	Serial Clock	AC23	I/O	OV_{DD}	2, 14
IIC4_SDA/EVT6/M1SRCID2/ LB_SRCID2/GPIO19	Serial Data	V24	I/O	OV_{DD}	2, 14
SerDes (x10) PCI Express, Serial RapidIO, Aurora, 10GE, 1GE					
SD_TX13	Transmit Data (positive)	C20	O	XV_{DD}	—
SD_TX12	Transmit Data (positive)	C18	O	XV_{DD}	—
SD_TX11	Transmit Data (positive)	D16	O	XV_{DD}	—
SD_TX10	Transmit Data (positive)	C14	O	XV_{DD}	—
SD_TX07	Transmit Data (positive)	C12	O	XV_{DD}	—
SD_TX06	Transmit Data (positive)	C10	O	XV_{DD}	—
SD_TX05	Transmit Data (positive)	C8	O	XV_{DD}	—
SD_TX04	Transmit Data (positive)	B4	O	XV_{DD}	—
SD_TX03	Transmit Data (positive)	F3	O	XV_{DD}	—
SD_TX02	Transmit Data (positive)	G5	O	XV_{DD}	—
SD_TX13	Transmit Data (negative)	D20	O	XV_{DD}	—
SD_TX12	Transmit Data (negative)	D18	O	XV_{DD}	—
SD_TX11	Transmit Data (negative)	C16	O	XV_{DD}	—
SD_TX10	Transmit Data (negative)	D14	O	XV_{DD}	—
SD_TX07	Transmit Data (negative)	D12	O	XV_{DD}	—
SD_TX06	Transmit Data (negative)	D10	O	XV_{DD}	—
SD_TX05	Transmit Data (negative)	D8	O	XV_{DD}	—
SD_TX04	Transmit Data (negative)	B5	O	XV_{DD}	—
SD_TX03	Transmit Data (negative)	F4	O	XV_{DD}	—
SD_TX02	Transmit Data (negative)	G6	O	XV_{DD}	—
SD_RX13	Receive Data (positive)	B21	I	XV_{DD}	—
SD_RX12	Receive Data (positive)	B19	I	XV_{DD}	—
SD_RX11	Receive Data (positive)	B15	I	XV_{DD}	—
SD_RX10	Receive Data (positive)	A13	I	XV_{DD}	—
SD_RX07	Receive Data (positive)	B11	I	XV_{DD}	—
SD_RX06	Receive Data (positive)	B9	I	XV_{DD}	—
SD_RX05	Receive Data (positive)	B7	I	XV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND166	Ground	B25	—	—	—
GND165	Ground	C23	—	—	—
GND164	Ground	D23	—	—	—
GND163	Ground	D27	—	—	—
GND162	Ground	E24	—	—	—
GND161	Ground	F22	—	—	—
GND160	Ground	F27	—	—	—
GND159	Ground	G10	—	—	—
GND158	Ground	G12	—	—	—
GND157	Ground	G14	—	—	—
GND156	Ground	G16	—	—	—
GND155	Ground	G18	—	—	—
GND154	Ground	G21	—	—	—
GND153	Ground	G22	—	—	—
GND152	Ground	H3	—	—	—
GND151	Ground	H4	—	—	—
GND150	Ground	H10	—	—	—
GND149	Ground	H12	—	—	—
GND148	Ground	H14	—	—	—
GND147	Ground	H16	—	—	—
GND146	Ground	H18	—	—	—
GND145	Ground	H21	—	—	—
GND144	Ground	H25	—	—	—
GND143	Ground	J2	—	—	—
GND142	Ground	J8	—	—	—
GND141	Ground	J10	—	—	—
GND140	Ground	J12	—	—	—
GND139	Ground	J14	—	—	—
GND138	Ground	J16	—	—	—
GND137	Ground	J18	—	—	—
GND136	Ground	J21	—	—	—
GND135	Ground	K5	—	—	—
GND134	Ground	K8	—	—	—
GND133	Ground	K10	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD_CA_PL	Core Group A and Platform Vdd Sense	H8	—	—	8
SENSEVDD_CB	Core Group B Vdd Sense	AB16	—	—	8
USB1_VDD_3P3	USB1 PHY Transceiver 3.3 V Supply	M23	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3 V Supply	J23	—	—	—
USB1_VDD_1P0	USB1 PHY PLL 1.0 V Supply	L22	—	—	—
USB2_VDD_1P0	USB2 PHY PLL 1.0 V Supply	K22	—	—	—
Analog Signals					
MVREF	SSTL_1.5/1.35 Reference Voltage	W7	I	$GV_{DD}/2$	—
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	E21	I	200Ω (±1%) to XV_{DD}	21
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	F7	I	200Ω (±1%) to SV_{DD}	22
TEMP_ANODE	Temperature Diode Anode	V5	—	internal diode	9
TEMP_CATHODE	Temperature Diode Cathode	U6	—	internal diode	9
USB2_IBIAS_REXT	USB PHY2 Reference Bias Current Generation	K23	—	GND	32
USB1_IBIAS_REXT	USB PHY1 Reference Bias Current Generation	L23	—	GND	32
USB2_VDD_1P8_DECAP	USB2 PHY 1.8 V Output to External Decap	K24	—	GND	33
USB1_VDD_1P8_DECAP	USB1 PHY 1.8 V Output to External Decap	L24	—	GND	33
No Connection Pins					
NC03	No Connection	W4	—	—	11
NC04	No Connection	W3	—	—	11
NC05	No Connection	W1	—	—	11
NC06	No Connection	H7	—	—	11
NC07	No Connection	G7	—	—	11
NC08	No Connection	F20	—	—	11
NC09	No Connection	F19	—	—	11
NC10	No Connection	F18	—	—	11
NC11	No Connection	F16	—	—	11
NC12	No Connection	F13	—	—	11

Table 2. Absolute Operating Conditions[1] (continued)

Parameter		Symbol	Max Value	Unit	Note
eSPI, eSHDC, GPIO		CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
DDR3 and DDR3L DRAM I/O voltage		GV_{DD}	–0.3 to 1.65	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
SerDes core logic supply and receivers		SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	—
Ethernet I/O, Ethernet management interface 1 (EMI1), 1588, GPIO		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3
USB PHY transceiver supply voltage		$USB\_V_{DD}\_3P3$	–0.3 to 3.63	V	—
USB PHY PLL supply voltage		$USB\_V_{DD}\_1P0$	–0.3 to 1.1	V	—
Low Power Security Monitor Supply		V_{DD_LP}	–0.3 to 1.1	V	—
Input voltage[7]	DDR3 and DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 7
	DDR3 and DDR3L DRAM reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2+ 0.3)	V	2, 7
	Ethernet signals, GPIO	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 7
	eSPI, eSHDC, GPIO	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 7
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	5, 7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6, 7
	SerDes signals	XV_{IN}	–0.4 to (XV_{DD} + 0.3)	V	7
	USB PHY transceiver signals	$USB\_V_{IN}\_3P3$	–0.3 to ($USB\_V_{DD}\_3P3$ + 0.3)	V	7
Storage junction temperature range		T_{stg}	–55 to 150	°C	—

While VDD is ramping, current may be supplied from VDD through the chip to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

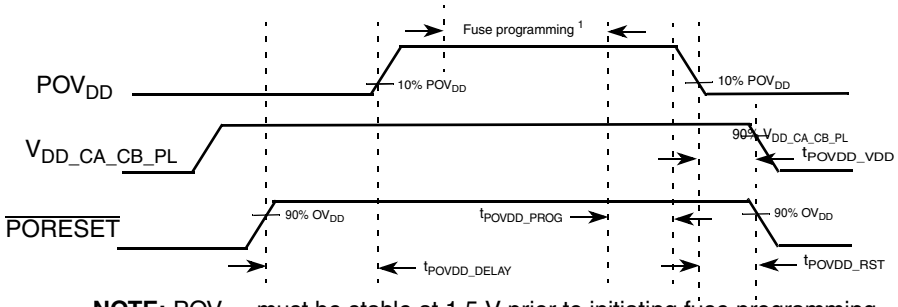
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to $V_{DD\_CA\_CB\_PL}$ ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before $V_{DD\_CA\_CB\_PL}$ is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{PORESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{PORESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

Table 6. Device Power Dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	667	534	1067	467	1.0	65	8.7	—	8.2	—	—	2, 3
Thermal						105	12.0	—	11.8	—	—	5, 7
Maximum							12.3	11.1	11.9	10.6	1.4	4, 6, 7

Note:

1. Combined power of $V_{DD\_CA\_CB\_PL}$, SVDD with the DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P2040 I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.705	1.764	W	1,2,5,6
	800 MT/s data rate		0.714	1.785		
	1066 MT/s data rate		0.731	1.827		
	1200 MT/s data rate		0.739	1.848		
	1333 MT/s data rate		0.747	1.869		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1, 7
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC Per Controller	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the device PLLs, at allowable voltage levels.

Table 8. Device AV_{DD} Power Dissipation

AV_{DD}s	Typical	Maximum	Unit	Note
AV_{DD_DDR}	5	15	mW	1
AV_{DD_CC1}				
AV_{DD_CC2}				
AV_{DD_PLAT}				
AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}				
USB_V_{DD_1P0}	—	10	mW	3

Note:

1. $V_{DD\_CA\_CB\_PL}$, T_A = 80°C, T_J = 105°C
2. SV_{DD} = 1.0 V, T_A = 80°C, T_J = 105°C
3. USB_V_{DD_1P0} = 1.0V, T_A = 80°C, T_J = 105°C

This table shows the estimated power dissipation on the POV_{DD} supply for the chip at allowable voltage levels.

Table 9. POV_{DD} Power Dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the device, at allowable voltage levels.

Table 10. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Notes
V_{DD_LP} (Device on, 105C)	1.5	mW	1
V_{DD_LP} (Device off, 70C)	195	uW	2
V_{DD_LP} (Device off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When the device is off, V_{DD_LP} may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC, which switches V_{DD_LP} to battery when the SoC is powered down. See the Trust Architecture chapter in the device reference manual for more information.

2.5 Thermal

Table 11. Package Thermal Characteristics [6]

Rating	Board	Symbol	Value	Unit	Note
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	21	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	15	°C/W	1, 3

2.7 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 17. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit[1]	Note
Required assertion time of $\overline{\text{PORESET}}$	1	—	ms	3
Required input assertion time of $\overline{\text{HRESET}}$	32	—	SYSCLKs	1, 2
Input setup time for POR configs with respect to negation of $\overline{\text{PORESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Note:
1. SYSCLK is the primary clock input for the device.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1, “Power-On Reset Sequence,” in the chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. Refer to Section 2.2, “Power Up Sequencing.”

Table 18. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

2.8 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 19. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (For example exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.9.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	1, 2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed the $MV_{REF}n$ DC level by more than ±1% of the DC value (that is, ±15mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $MV_{REF}n$ with a min value of $MV_{REF}n$ – 0.04 and a max value of $MV_{REF}n$ + 0.04. V_{TT} should track variations in the DC level of $MV_{REF}n$.
4. The voltage regulator for $MV_{REF}n$ must meet the specifications stated in Table 23.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.35 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	1, 2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.090	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.8	mA	7, 8
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.8	—	mA	7, 8

Table 56. I^2C DC Electrical Characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–40	40	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.18.2 I^2C AC Electrical Specifications

This table provides the I^2C AC timing specifications.

Table 57. I^2C AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

2.19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

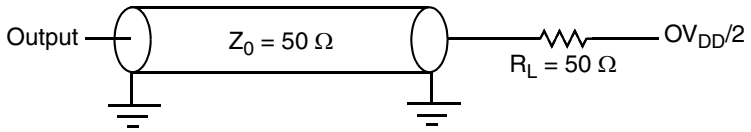


Figure 31. GPIO AC Test Load

2.20 High-Speed Serial Interfaces (HSSI)

The device features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, Aurora, and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

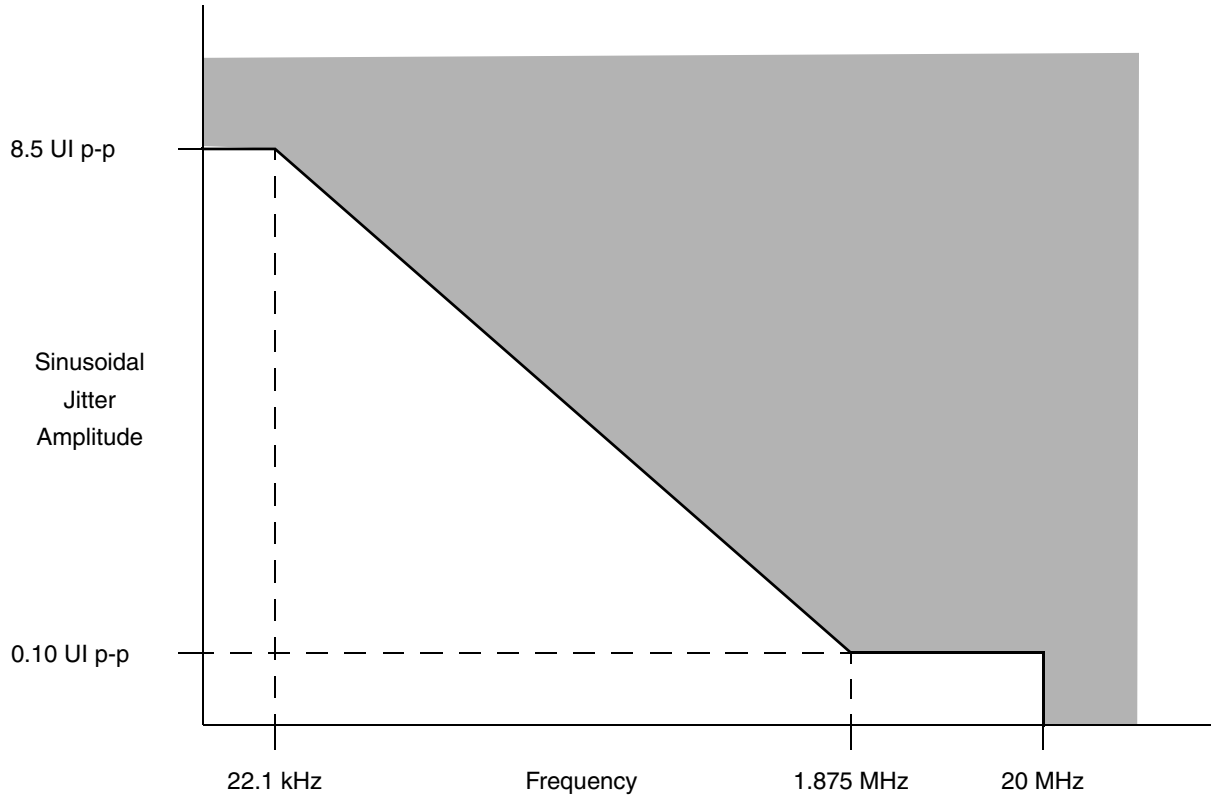


Figure 42. Single-Frequency Sinusoidal Jitter Limits

2.20.6 Aurora

This section describes the Aurora clocking requirements and AC and DC electrical characteristics.

2.20.6.1 Aurora DC Electrical Characteristics

This section describes the DC electrical characteristics for Aurora.

2.20.6.1.1 Aurora DC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 2(SD_REF_CLK2 and $\overline{\text{SD\_REF\_CLK2}}$) may be used for SerDes Aurora configurations based on the RCW configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 1.

For more information on these specifications, see Section 2.20.2, "SerDes Reference Clocks."

2.20.6.1.2 Aurora Transmitter DC Electrical Characteristics

This table provides the Aurora transmitter DC electrical characteristics (XVDD = 1.5 V or 1.8 V).

Table 74. Aurora Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p

2.20.6.1.3 Aurora Receiver DC Electrical Characteristics

This table provides the Aurora receiver DC electrical characteristics (XVDD = 1.5 V or 1.8 V).

Table 75. Aurora Receiver DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:
1. Measured at receiver

2.20.6.2 Aurora AC Timing Specifications

This section describes the AC timing specifications for Aurora.

2.20.6.2.1 Aurora AC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 2(SD_REF_CLK2 and $\overline{\text{SD\_REF\_CLK2}}$) may be used for SerDes Aurora configurations based on the RCW configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 1.

2.20.6.2.2 Aurora Transmitter AC Timing Specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 76. Aurora Transmitter AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

2.20.6.2.3 Aurora Receiver AC Timing Specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 77. Aurora Receiver AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 2i/3G Receiver (Rx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:
1. Measured at receiver.

2.20.8 SGMII Interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the device, as shown in Figure 44, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 39.

2.20.8.0.1 SGMII Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK[1:2] and $\overline{\text{SD\_REF\_CLK}[1:2]}$ pins. SerDes banks 1–2 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, “SerDes Reference Clocks.”

2.20.8.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.1.1 SGMII Transmit DC Timing Specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) as shown in Figure 45.

Table 87. SGMII DC Transmitter Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1

Table 89. SGMII DC Receiver Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 2.20.4.4, "PCI Express DC Physical Layer Receiver Specifications," and Section 2.20.4.5.2, "PCI Express AC Physical Layer Receiver Specifications," for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1–3)GCR(lane)1[REIDL_CTL] bit field.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 90. SGMII 2.5x Receiver DC Timing Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:
1. Measured at the receiver.

2.20.8.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.20.8.2.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 91. SGMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	1
Unit interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	—
Unit interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
AC coupling capacitor	C_{TX}	10		200	nF	2

Note:
1. See Figure 42 for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.20.8.2.2 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$) respectively, as depicted in this figure.

3.1.4 e500mc Core Complex PLL Select

The clock frequency of each the e500mc core 0–3 complex is determined by the binary value of the RCW field CC*n*_PLL_SEL. These tables describe the supported ratios for each core complex 0–3, where each individual core complex can select a frequency from the table.

Table 96. e500mc Core Complex [0,1] PLL Select

Binary Value of C*n*_PLL_SEL for n=[0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0001	CC1 PLL /2
0100	CC2 PLL /1
All Others	Reserved

Table 97. e500mc Core Complex [2,3] PLL Select

Binary Value of C*n*_PLL_SEL for n=[0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0100	CC2 PLL /1
0101	CC2 PLL /2
All Others	Reserved

3.1.5 DDR Controller PLL Ratios

The single DDR memory controller complexes can be asynchronous to the platform, depending on configuration.

Table 98 describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in this table. This ratio is determined by the binary value of the RCW configuration field MEM_PLL_RAT[10:14].

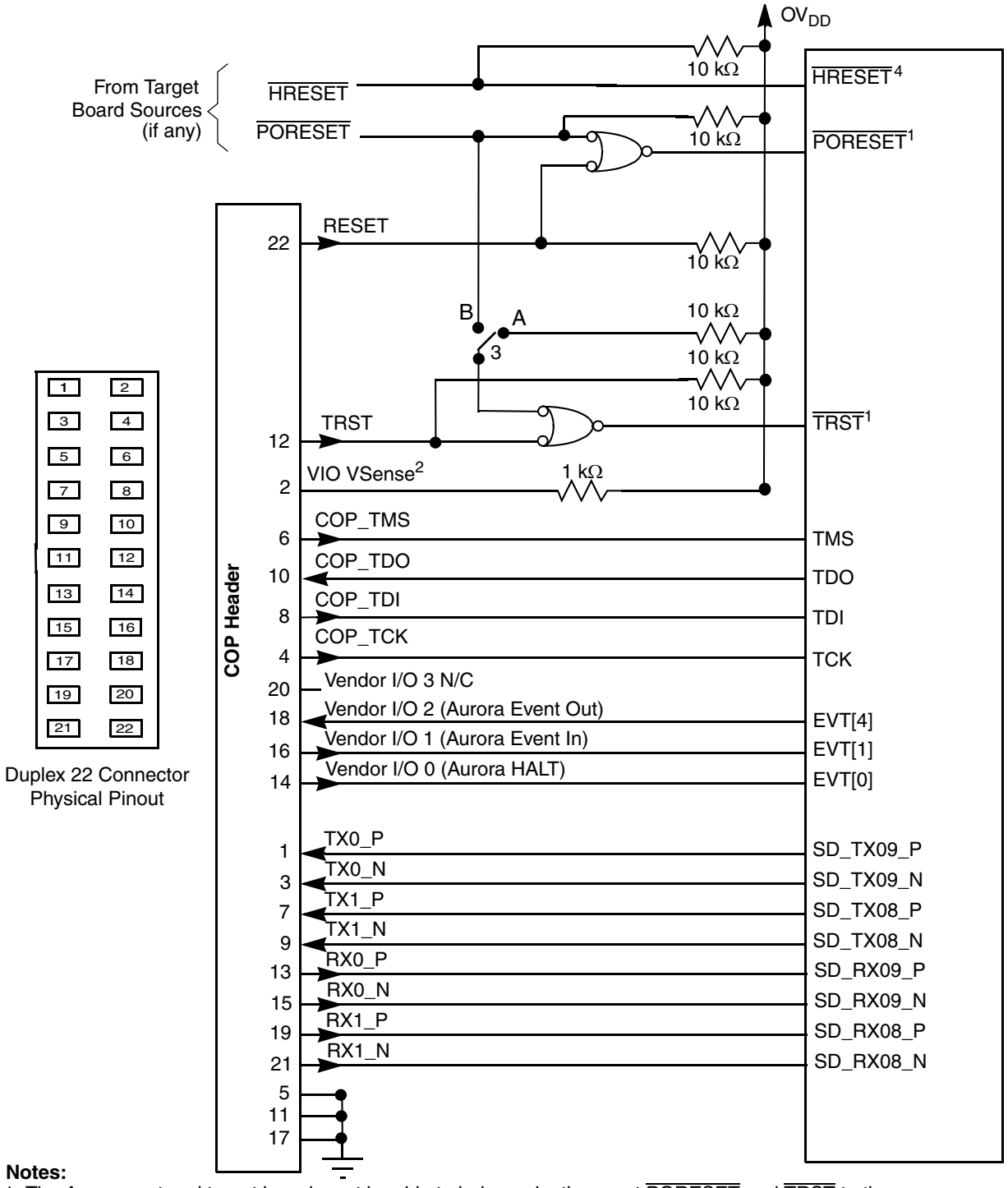
The RCW configuration field MEM_PLL_CFG[8:9] must be set to MEM_PLL_CFG[8:9] = 0b01 if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in Table 98 for asynchronous DDR clock ratios; otherwise, set MEM_PLL_CFG[8:9] = 0b00.

NOTE

The RCW Configuration field DDR_SYNC (bit 184) must be set to 0b0 for asynchronous mode.

The RCW Configuration field DDR_RATE (bit 232) must be set to b’0 for asynchronous mode

The RCW Configuration field DDR_RSV0 (bit 234) must be set to b’0 for all ratios.



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device. $\overline{\text{HRESET}}$ is not used by the Aurora 22 pin connector.

Figure 58. Aurora 22 Pin Connector Duplex Interface Connection