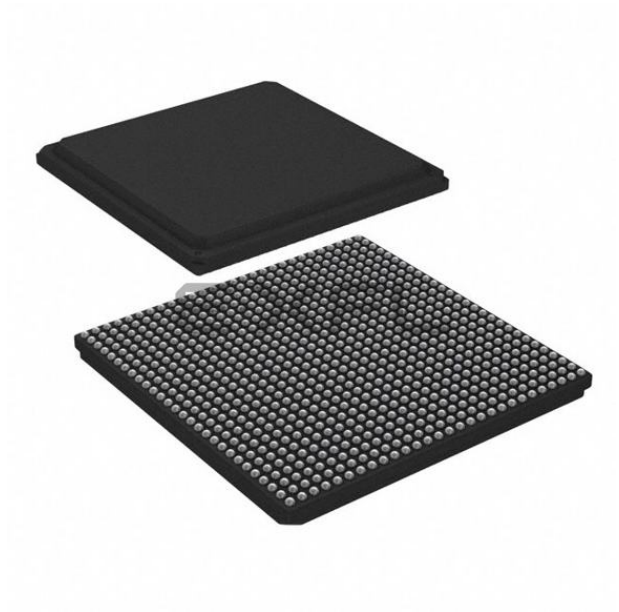


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.3GHz
Co-Processors/DSP	Security; SEC 4.2
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator, Secure Fusebox
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2041nxe7nnc

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MDQS5}}$	Data Strobe	AH24	I/O	GV_{DD}	—
$\overline{\text{MDQS6}}$	Data Strobe	AE22	I/O	GV_{DD}	—
$\overline{\text{MDQS7}}$	Data Strobe	AF28	I/O	GV_{DD}	—
$\overline{\text{MDQS8}}$	Data Strobe	AG3	I/O	GV_{DD}	—
MBA0	Bank Select	AC16	O	GV_{DD}	—
MBA1	Bank Select	AC15	O	GV_{DD}	—
MBA2	Bank Select	AC8	O	GV_{DD}	—
MA00	Address	AG16	O	GV_{DD}	—
MA01	Address	AF12	O	GV_{DD}	—
MA02	Address	AC12	O	GV_{DD}	—
MA03	Address	AH11	O	GV_{DD}	—
MA04	Address	AG11	O	GV_{DD}	—
MA05	Address	AH10	O	GV_{DD}	—
MA06	Address	AC11	O	GV_{DD}	—
MA07	Address	AC10	O	GV_{DD}	—
MA08	Address	AF10	O	GV_{DD}	—
MA09	Address	AH9	O	GV_{DD}	—
MA10	Address	AH16	O	GV_{DD}	—
MA11	Address	AG9	O	GV_{DD}	—
MA12	Address	AC9	O	GV_{DD}	—
MA13	Address	AH20	O	GV_{DD}	—
MA14	Address	AG8	O	GV_{DD}	—
MA15	Address	AH7	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	AH18	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	AH17	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	AH19	O	GV_{DD}	—
$\overline{\text{MCS0}}$	Chip Select	AC18	O	GV_{DD}	—
$\overline{\text{MCS1}}$	Chip Select	AC21	O	GV_{DD}	—
$\overline{\text{MCS2}}$	Chip Select	AG17	O	GV_{DD}	—
$\overline{\text{MCS3}}$	Chip Select	AG20	O	GV_{DD}	—
MCKE0	Clock Enable	AB8	O	GV_{DD}	—
MCKE1	Clock Enable	AB7	O	GV_{DD}	—
MCKE2	Clock Enable	AH6	O	GV_{DD}	—
MCKE3	Clock Enable	AG6	O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND166	Ground	B25	—	—	—
GND165	Ground	C23	—	—	—
GND164	Ground	D23	—	—	—
GND163	Ground	D27	—	—	—
GND162	Ground	E24	—	—	—
GND161	Ground	F22	—	—	—
GND160	Ground	F27	—	—	—
GND159	Ground	G10	—	—	—
GND158	Ground	G12	—	—	—
GND157	Ground	G14	—	—	—
GND156	Ground	G16	—	—	—
GND155	Ground	G18	—	—	—
GND154	Ground	G21	—	—	—
GND153	Ground	G22	—	—	—
GND152	Ground	H3	—	—	—
GND151	Ground	H4	—	—	—
GND150	Ground	H10	—	—	—
GND149	Ground	H12	—	—	—
GND148	Ground	H14	—	—	—
GND147	Ground	H16	—	—	—
GND146	Ground	H18	—	—	—
GND145	Ground	H21	—	—	—
GND144	Ground	H25	—	—	—
GND143	Ground	J2	—	—	—
GND142	Ground	J8	—	—	—
GND141	Ground	J10	—	—	—
GND140	Ground	J12	—	—	—
GND139	Ground	J14	—	—	—
GND138	Ground	J16	—	—	—
GND137	Ground	J18	—	—	—
GND136	Ground	J21	—	—	—
GND135	Ground	K5	—	—	—
GND134	Ground	K8	—	—	—
GND133	Ground	K10	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD_CA_PL	Core Group A and Platform Vdd Sense	H8	—	—	8
SENSEVDD_CB	Core Group B Vdd Sense	AB16	—	—	8
USB1_VDD_3P3	USB1 PHY Transceiver 3.3 V Supply	M23	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3 V Supply	J23	—	—	—
USB1_VDD_1P0	USB1 PHY PLL 1.0 V Supply	L22	—	—	—
USB2_VDD_1P0	USB2 PHY PLL 1.0 V Supply	K22	—	—	—
Analog Signals					
MVREF	SSTL_1.5/1.35 Reference Voltage	W7	I	$GV_{DD}/2$	—
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	E21	I	200Ω (±1%) to XV_{DD}	21
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	F7	I	200Ω (±1%) to SV_{DD}	22
TEMP_ANODE	Temperature Diode Anode	V5	—	internal diode	9
TEMP_CATHODE	Temperature Diode Cathode	U6	—	internal diode	9
USB2_IBIAS_REXT	USB PHY2 Reference Bias Current Generation	K23	—	GND	32
USB1_IBIAS_REXT	USB PHY1 Reference Bias Current Generation	L23	—	GND	32
USB2_VDD_1P8_DECAP	USB2 PHY 1.8 V Output to External Decap	K24	—	GND	33
USB1_VDD_1P8_DECAP	USB1 PHY 1.8 V Output to External Decap	L24	—	GND	33
No Connection Pins					
NC03	No Connection	W4	—	—	11
NC04	No Connection	W3	—	—	11
NC05	No Connection	W1	—	—	11
NC06	No Connection	H7	—	—	11
NC07	No Connection	G7	—	—	11
NC08	No Connection	F20	—	—	11
NC09	No Connection	F19	—	—	11
NC10	No Connection	F18	—	—	11
NC11	No Connection	F16	—	—	11
NC12	No Connection	F13	—	—	11

Table 6. Device Power Dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core & Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Note
							Quad Cores		Dual Cores			
Typical	667	534	1067	467	1.0	65	8.7	—	8.2	—	—	2, 3
Thermal						105	12.0	—	11.8	—	—	5, 7
Maximum							12.3	11.1	11.9	10.6	1.4	4, 6, 7

Note:

1. Combined power of $V_{DD\_CA\_CB\_PL}$, SVDD with the DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P2040 I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.705	1.764	W	1,2,5,6
	800 MT/s data rate		0.714	1.785		
	1066 MT/s data rate		0.731	1.827		
	1200 MT/s data rate		0.739	1.848		
	1333 MT/s data rate		0.747	1.869		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1, 7
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC Per Controller	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6

2.6.3 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the e500mc; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 16× the period of the platform clock. That is, minimum clock high time is 8× (platform clock), and minimum clock low time is 8× (platform clock). There is no minimum RTC frequency; RTC may be grounded if not needed.

2.6.4 dTSEC Gigabit Ethernet Reference Clock Timing

This table provides the dTSEC gigabit reference clocks DC electrical characteristics.

Table 15. EC_GTX_CLK125 DC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.

This table provides the dTSEC gigabit reference clocks AC timing specifications.

Table 16. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Note:
1. Rise and fall times for EC_GTX_CLK125 are measured from 20% to 80% (rise time) and 80% to 20% (fall time) of LV_{DD}.
2. EC_GTX_CLK125 is used to generate the GTX clock for the dTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the dTSEC GTX_CLK. See Section 2.12.2.2, "RGMII AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.6.5 Other Input Clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information on the input clock requirements of functional blocks sourced external of the device, such as SerDes, Ethernet Management, eSDHC, Local Bus, see the specific interface section.

2.9.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 24. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Max	Unit	Note
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	—	MVREF*n* – 0.150	V	—
	≤ 1200 MT/s data rate			MVREF*n* – 0.175		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	MVREF*n* + 0.150	—	V	—
	≤ 1200 MT/s data rate		MVREF*n* + 0.175			

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 25. DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Max	Unit	Note
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	—	MVREF*n* – 0.135	V	—
	≤ 1200 MT/s data rate		—	MVREF*n* – 0.160		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	MVREF*n* + 0.135	—	V	—
	≤ 1200 MT/s data rate		MVREF*n* + 0.160	—		

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 26. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}			ps	1
1200 MT/s data rate		–142	142		
1066 MT/s data rate		–170	170		
800 MT/s data rate		–200	200		
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}			ps	2
1200 MT/s data rate		–275	275		
1066 MT/s data rate		–300	300		
800 MT/s data rate		–425	425		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

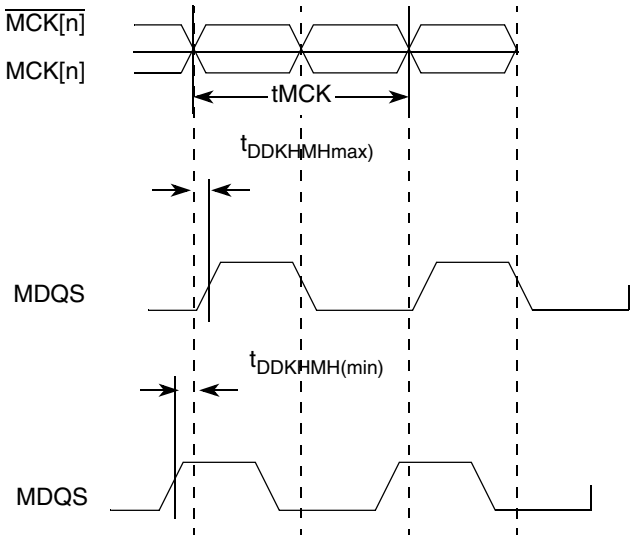


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

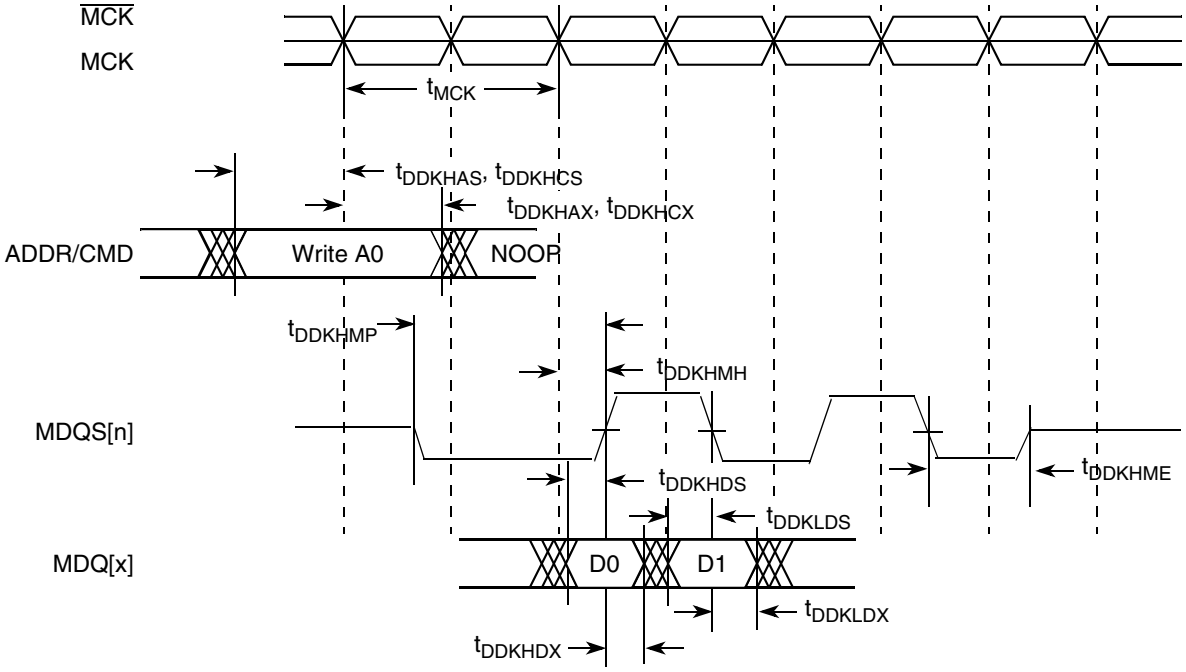


Figure 11. DDR3 and DDR3L Output Timing Diagram

Table 43. eTSEC IEEE 1588 AC Timing Specifications (continued)

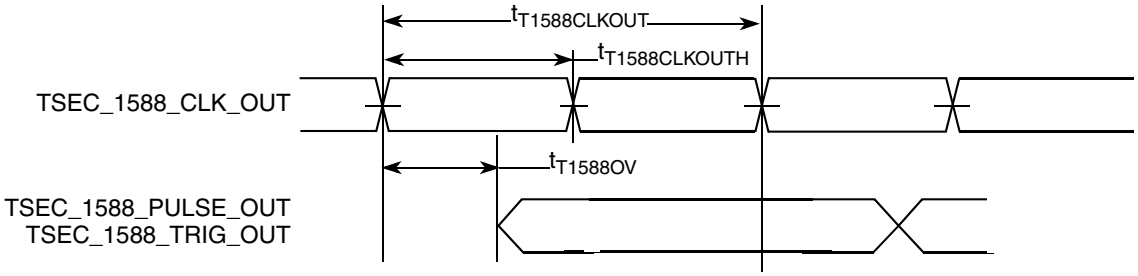
For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

Figure 18. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

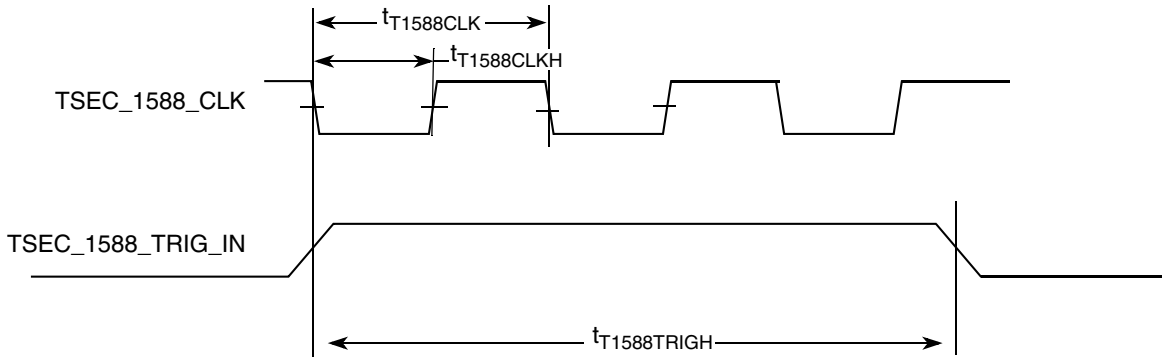


Figure 19. eTSEC IEEE 1588 Input AC Timing

only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 37 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{\overline{SD\_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{TD}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and $\overline{SD\_REF\_CLK1}$ for SerDes bank1 and SD_REF_CLK2 and $\overline{SD\_REF\_CLK2}$ for SerDes bank2.

SerDes banks 1–2 may be used for various combinations of the following IP blocks based on the RCW configuration field SRDS_PRTCL:

- SerDes bank 1: PCI Express 1/2/3, sRIO1/2, SGMII (1.25 Gbps only).
- SerDes bank 2: PCI Express3, SGMII (1.25 or 3.125 GBaud), SATA or Aurora.

The following sections describe the SerDes reference clock requirements and provide application information.

2.20.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

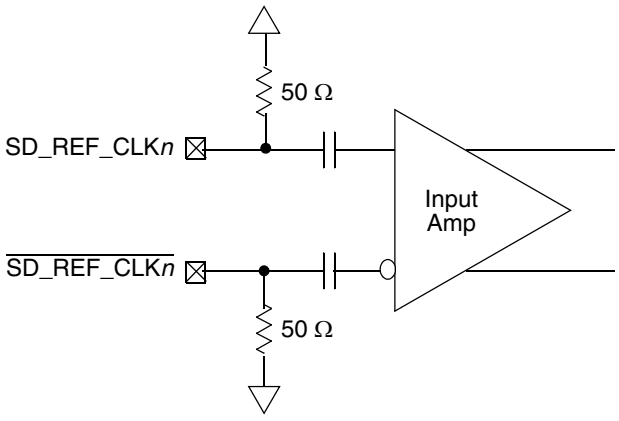


Figure 33. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in Section 2.1.2, "Recommended Operating Conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ are internally AC-coupled differential inputs as shown in Figure 33. Each differential clock input (SD_REF_CLK*n* or $\overline{\text{SD\_REF\_CLK}n}$) has on-chip 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. This figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

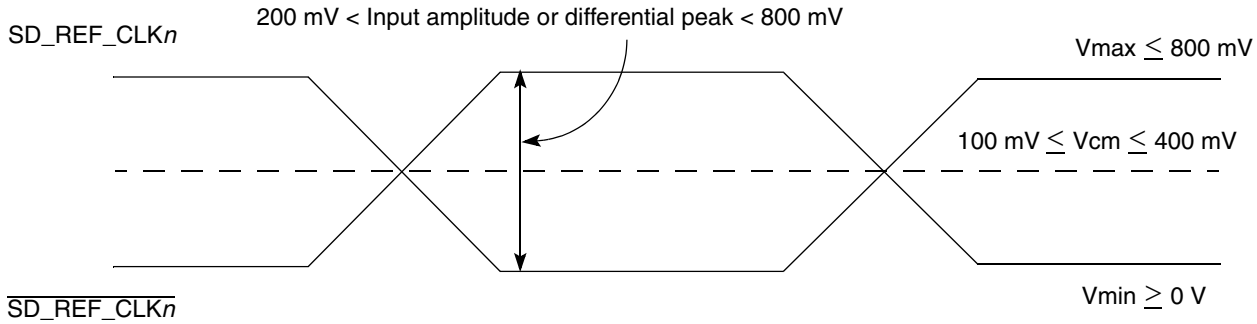


Figure 34. Differential Reference Clock Input DC Requirements (External DC-Coupled)

Table 65. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = $2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Note:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.20.4.5 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.5.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 40 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 67. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 – T_{TX-EYE} = 0.25 UI. See Notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 40 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.20.4.5.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications 2.5 GT/s and 5 GT/s.

Table 69. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input AC Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture

Note:

1. No test load is necessarily associated with this value.

2.20.4.6 Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in this figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

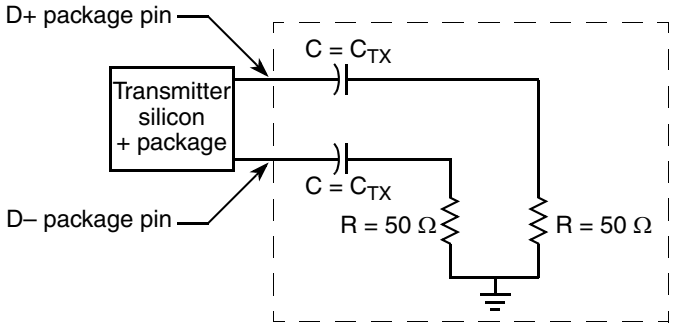


Figure 40. Test/Measurement Load

2.20.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125, and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

2.20.6.1.3 Aurora Receiver DC Electrical Characteristics

This table provides the Aurora receiver DC electrical characteristics (XVDD = 1.5 V or 1.8 V).

Table 75. Aurora Receiver DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:
1. Measured at receiver

2.20.6.2 Aurora AC Timing Specifications

This section describes the AC timing specifications for Aurora.

2.20.6.2.1 Aurora AC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 2(SD_REF_CLK2 and $\overline{\text{SD\_REF\_CLK2}}$) may be used for SerDes Aurora configurations based on the RCW configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 1.

2.20.6.2.2 Aurora Transmitter AC Timing Specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 76. Aurora Transmitter AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

2.20.6.2.3 Aurora Receiver AC Timing Specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 77. Aurora Receiver AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—

2.20.7.1.2 SATA DC Receiver (Rx) Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 80. Gen1i/1.5 G Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{SATA_RXDIFF}	240	—	600	mV p-p	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	—

Note:
1. Voltage relative to common of either signal comprising a differential pair

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 81. Gen2i/3 G Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{SATA_RXDIFF}	275	—	750	mV p-p	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Note:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

2.20.7.2 SATA AC Timing Specifications

This section discusses the SATA AC timing specifications.

2.20.7.2.1 AC Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in this table to be guaranteed by the customer's application design.

Table 82. SATA Reference Clock Input Requirements

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	+350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—

"e500mc Core Cluster to SYSCLK PLL Ratio." The frequency for each core complex 0–3 is selected using the configuration bits as described in Table 96.

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Platform to SYSCLK PLL Ratio."
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in Section 3.1.5, "DDR Controller PLL Ratios."
- Each of the three SerDes blocks has a PLL which generate a core clock from their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.6, "Frequency Options."

3.1.1 Clock Ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 93. Processor Clocking Specifications

Parameter	Maximum Processor Core Frequency								Unit	Note
	667 MHz		800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500mc core PLL frequency	667	667	667	800	667	1000	667	1200	MHz	1,4
e500mc core frequency	333	667	333	800	333	1000	333	1200	MHz	4, 8
Platform clock frequency	400	533	400	533	400	533	400	600	MHz	1
Memory bus clock frequency	400	533	400	533	400	533	400	600	MHz	1,2,5,6
Local bus clock frequency	—	67	—	67	—	67	—	75	MHz	3
PME	—	267	—	267	—	267	—	300	MHz	7
FMan	—	467	—	467	—	467	—	500	MHz	—

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500-mc core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e500mc (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3 memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the chip reference manual for more information.
4. The e500mc core can run at e500mc core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 667 MHz, this results in a minimum allowable e500mc core frequency of 333 MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. The PME runs synchronously to the platform clock, running at a frequency of platform clock/2.
8. Core frequency must be at least as fast as the platform frequency (Rev 1.1 silicon).

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW clocking configuration fields FM_CLK_SEL.

Table 104. Frame Manager Clock Select

Binary Value of FM_CLK_SEL	FM Frequency
0b0	Platform Clock Frequency /2
0b1	Core Cluster 2 Frequency /2[1]

Notes:

1 For asynchronous mode, max frequency, see Table 93.

3.2 Supply Power Default Setting

The device is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in Table 105, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

3.3 Power Supply Design

This section discusses the power supply design.

3.3.1 PLL Power Supply Filtering

Each of the PLLs described in Section 3.1, "System Clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, AV_{DD_CCn} and AV_{DD_DDR} voltages must be derived directly from the $V_{DD\_CA\_CB\_PL}$ source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 50, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 50 shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%

C1 = 10µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH

C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD}.

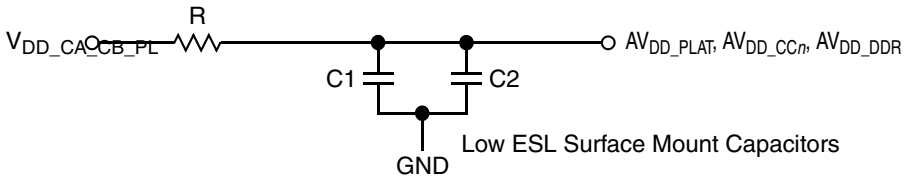


Figure 50. PLL Power Supply Filter Circuit

The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 51. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn}

3.6.4.1 USB Divider Network

This figure shows the required divider network for the VBUS interface for the device. Additional requirements for the external components are as follows:

- Both resistors require 0.1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V–5.25 V.
- The 0.6 V diode requires an I_F = 10 mA, I_R < 500 nA and $V_{F(Max)}$ = 0.8 V.

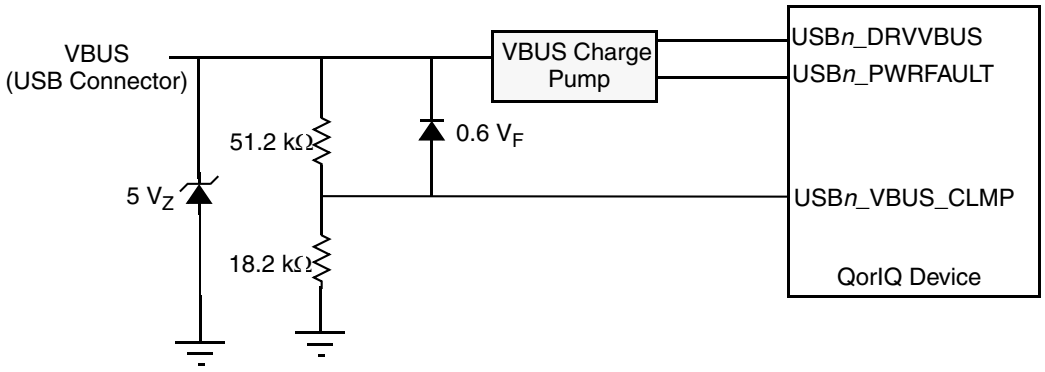


Figure 60. Divider Network at VBUS

USB1_DRVVBUS and USB1_PWRFAULT are muxed on GPIO[25] and GPIO[27] pins, respectively. USB2_DRVVBUS and USB2_PWRFAULT are muxed on GPIO[6:7] pins, respectively. Setting RCW[GPIO] selects USB functionality on the GPIO pins.

3.6.4.2 USB*n*_V_{DD}_1P8_DECAP Capacitor Options

The USB*n*_V_{DD}_1P8_DECAP pins require a capacitor connected to GND.

This table lists the recommended capacitors for the USBn_VDD_1P8_DECAP signal.

Table 106. Recommended Capacitor Parts for USB*n*_V_{DD}_1P8_DECAP

Manufacturer	Part Number	Value	ESR	Package
Kemet	T494B105(1)025A(2)	1 uF, 25 V	2 Ω	B(3528)
	T494B155(1)025A(2)	1.5 uF, 25 V	1.5 Ω	—
NIC	NMC0603X7R106KTRPF	1 uF, 10 V	Low ESR	0603
TDK Corporation	CERB2CX5R0G105M	1 uF, 4 V	200 m-Ω	0603
Vishay	TR3B105(1)035(2)1500	1 uF, 35 V	1.5 Ω	B(3528)

3.7 Recommended Thermal Model

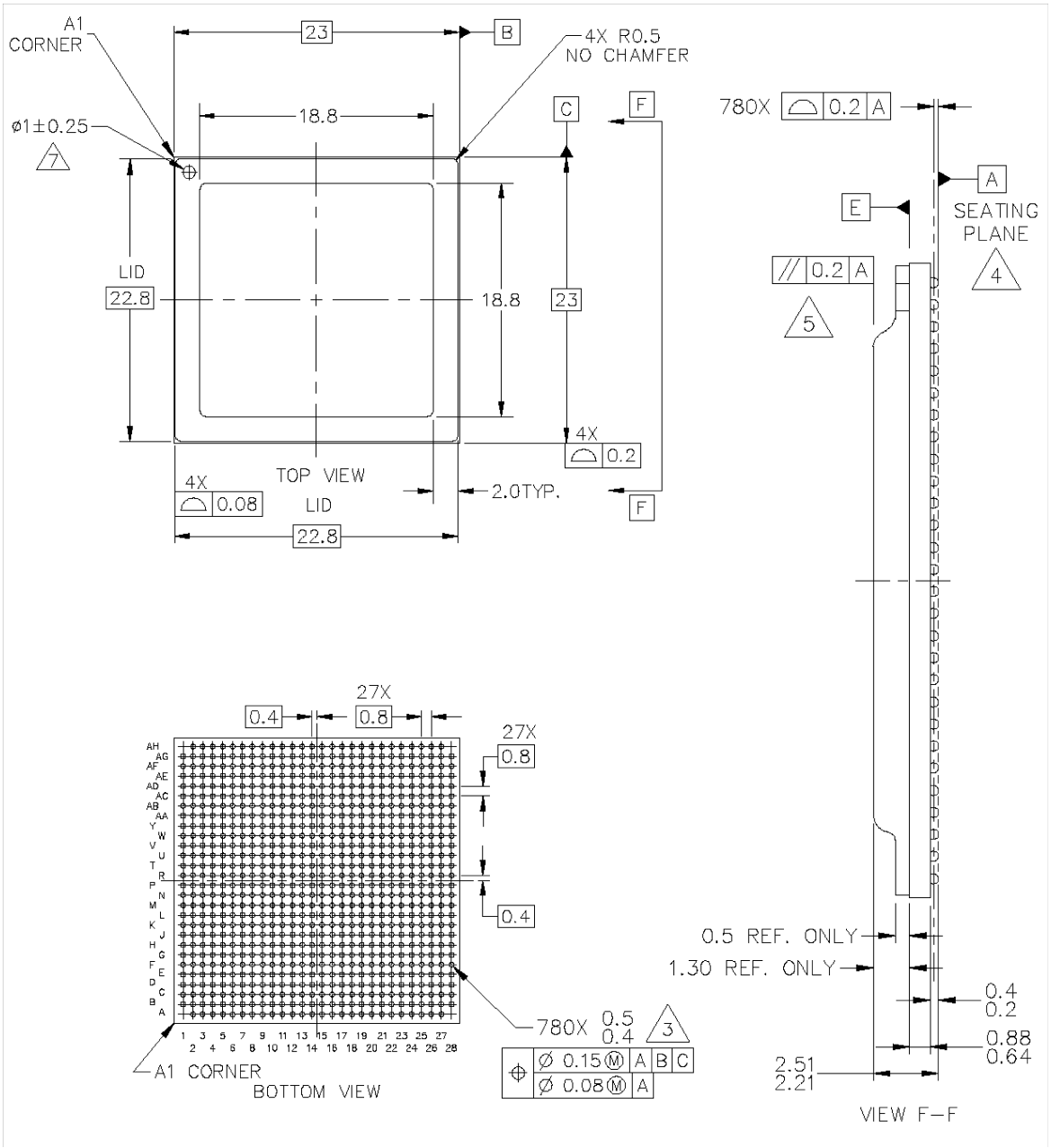
Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow,

4.2 Mechanical Dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the device.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement excludes any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
7. Pin 1 thru hole is centered within foot area.

Figure 63. Mechanical Dimensions of the FC-PBGA with Full Lid