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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	-
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p2041nxn1pnb

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0 / DMA1_DDONE0/SDHC_WP	Serial Data	AB26	I/O	OV_{DD}	2, 14
IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/ GPIO18/DMA1_DREQ0	Serial Clock	AC23	I/O	OV_{DD}	2, 14
IIC4_SDA/EVT6/M1SRCID2/ LB_SRCID2/GPIO19	Serial Data	V24	I/O	OV_{DD}	2, 14
SerDes (x10) PCI Express, Serial RapidIO, Aurora, 10GE, 1GE					
SD_TX13	Transmit Data (positive)	C20	O	XV_{DD}	—
SD_TX12	Transmit Data (positive)	C18	O	XV_{DD}	—
SD_TX11	Transmit Data (positive)	D16	O	XV_{DD}	—
SD_TX10	Transmit Data (positive)	C14	O	XV_{DD}	—
SD_TX07	Transmit Data (positive)	C12	O	XV_{DD}	—
SD_TX06	Transmit Data (positive)	C10	O	XV_{DD}	—
SD_TX05	Transmit Data (positive)	C8	O	XV_{DD}	—
SD_TX04	Transmit Data (positive)	B4	O	XV_{DD}	—
SD_TX03	Transmit Data (positive)	F3	O	XV_{DD}	—
SD_TX02	Transmit Data (positive)	G5	O	XV_{DD}	—
SD_TX13	Transmit Data (negative)	D20	O	XV_{DD}	—
SD_TX12	Transmit Data (negative)	D18	O	XV_{DD}	—
SD_TX11	Transmit Data (negative)	C16	O	XV_{DD}	—
SD_TX10	Transmit Data (negative)	D14	O	XV_{DD}	—
SD_TX07	Transmit Data (negative)	D12	O	XV_{DD}	—
SD_TX06	Transmit Data (negative)	D10	O	XV_{DD}	—
SD_TX05	Transmit Data (negative)	D8	O	XV_{DD}	—
SD_TX04	Transmit Data (negative)	B5	O	XV_{DD}	—
SD_TX03	Transmit Data (negative)	F4	O	XV_{DD}	—
SD_TX02	Transmit Data (negative)	G6	O	XV_{DD}	—
SD_RX13	Receive Data (positive)	B21	I	XV_{DD}	—
SD_RX12	Receive Data (positive)	B19	I	XV_{DD}	—
SD_RX11	Receive Data (positive)	B15	I	XV_{DD}	—
SD_RX10	Receive Data (positive)	A13	I	XV_{DD}	—
SD_RX07	Receive Data (positive)	B11	I	XV_{DD}	—
SD_RX06	Receive Data (positive)	B9	I	XV_{DD}	—
SD_RX05	Receive Data (positive)	B7	I	XV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_RX04	Receive Data (positive)	A2	I	XV_{DD}	—
SD_RX03	Receive Data (positive)	E1	I	XV_{DD}	—
SD_RX02	Receive Data (positive)	G1	I	XV_{DD}	—
$\overline{\text{SD\_RX13}}$	Receive Data (negative)	A21	I	XV_{DD}	—
$\overline{\text{SD\_RX12}}$	Receive Data (negative)	A19	I	XV_{DD}	—
$\overline{\text{SD\_RX11}}$	Receive Data (negative)	A15	I	XV_{DD}	—
$\overline{\text{SD\_RX10}}$	Receive Data (negative)	B13	I	XV_{DD}	—
$\overline{\text{SD\_RX07}}$	Receive Data (negative)	A11	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive Data (negative)	A9	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive Data (negative)	A7	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive Data (negative)	A3	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive Data (negative)	E2	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive Data (negative)	G2	I	XV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	D3	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes Bank 1 PLL Reference Clock Complement	D4	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	E17	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes Bank 2 PLL Reference Clock Complement	F17	I	XV_{DD}	—
General-Purpose Input/Output					
GPIO00/$\overline{\text{SPI\_CS0}}$/SDHC_DATA4	General Purpose Input/Output	H26	I/O	CV_{DD}	—
GPIO01/$\overline{\text{SPI\_CS1}}$/SDHC_DATA5	General Purpose Input/Output	H23	I/O	CV_{DD}	—
GPIO02/$\overline{\text{SPI\_CS2}}$/SDHC_DATA6	General Purpose Input/Output	H27	I/O	CV_{DD}	—
GPIO03$\overline{\text{SPI_CS3}}$/SDHC_DATA7	General Purpose Input/Output	H24	I/O	CV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input/Output	R23	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input/Output	P26	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input/Output	R26	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input/Output	P27	I/O	OV_{DD}	—
GPIO12/$\overline{\text{UART1\_RTS}}$/UART3_SOUT	General Purpose Input/Output	P24	I/O	OV_{DD}	—
GPIO13/$\overline{\text{UART2\_RTS}}$/UART4_SOUT	General Purpose Input/Output	P25	I/O	OV_{DD}	—
GPIO14/$\overline{\text{UART1\_CTS}}$/UART3_SIN	General Purpose Input/Output	R25	I/O	OV_{DD}	—
GPIO15/$\overline{\text{UART2\_CTS}}$/UART4_SIN	General Purpose Input/Output	P23	I/O	OV_{DD}	—
GPIO16/IIC3_SCL/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/$\overline{\text{SDHC\_CD}}$	General Purpose Input/Output	AB23	I/O	OV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
USB1_AGND01	USB1 PHY Transceiver GND	M28	—	—	—
USB2_AGND06	USB2 PHY Transceiver GND	J22	—	—	—
USB2_AGND05	USB2 PHY Transceiver GND	J24	—	—	—
USB2_AGND04	USB2 PHY Transceiver GND	J26	—	—	—
USB2_AGND03	USB2 PHY Transceiver GND	K25	—	—	—
USB2_AGND02	USB2 PHY Transceiver GND	L25	—	—	—
USB2_AGND01	USB2 PHY Transceiver GND	M26	—	—	—
OVDD06	General I/O Supply	N20	—	OV_{DD}	—
OVDD05	General I/O Supply	P20	—	OV_{DD}	—
OVDD04	General I/O Supply	R20	—	OV_{DD}	—
OVDD03	General I/O Supply	T20	—	OV_{DD}	—
OVDD02	General I/O Supply	T26	—	OV_{DD}	—
OVDD01	General I/O Supply	W26	—	OV_{DD}	—
CVDD2	eSPI and eSDHC Supply	K20	—	CV_{DD}	—
CVDD1	eSPI and eSDHC Supply	M20	—	CV_{DD}	—
GVDD17	DDR Supply	AA8	—	GV_{DD}	—
GVDD16	DDR Supply	AA9	—	GV_{DD}	—
GVDD15	DDR Supply	AA10	—	GV_{DD}	—
GVDD14	DDR Supply	AA11	—	GV_{DD}	—
GVDD13	DDR Supply	AA12	—	GV_{DD}	—
GVDD12	DDR Supply	AA13	—	GV_{DD}	—
GVDD11	DDR Supply	AA14	—	GV_{DD}	—
GVDD10	DDR Supply	AA15	—	GV_{DD}	—
GVDD09	DDR Supply	AB13	—	GV_{DD}	—
GVDD08	DDR Supply	AB14	—	GV_{DD}	—
GVDD07	DDR Supply	AC13	—	GV_{DD}	—
GVDD06	DDR Supply	AC14	—	GV_{DD}	—
GVDD05	DDR Supply	AF6	—	GV_{DD}	—
GVDD04	DDR Supply	AF9	—	GV_{DD}	—
GVDD03	DDR Supply	AF17	—	GV_{DD}	—
GVDD02	DDR Supply	AF20	—	GV_{DD}	—
GVDD01	DDR Supply	AF23	—	GV_{DD}	—
BVDD07	Local Bus Supply	J7	—	BV_{DD}	—
BVDD06	Local Bus Supply	K7	—	BV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
BVDD05	Local Bus Supply	L4	—	BV_{DD}	—
BVDD04	Local Bus Supply	L7	—	BV_{DD}	—
BVDD03	Local Bus Supply	M7	—	BV_{DD}	—
BVDD02	Local Bus Supply	N4	—	BV_{DD}	—
BVDD01	Local Bus Supply	R4	—	BV_{DD}	—
SVDD17	SerDes Core Logic Supply	A4	—	SV_{DD}	—
SVDD16	SerDes Core Logic Supply	A6	—	SV_{DD}	—
SVDD15	SerDes Core Logic Supply	A10	—	SV_{DD}	—
SVDD14	SerDes Core Logic Supply	A14	—	SV_{DD}	—
SVDD13	SerDes Core Logic Supply	A18	—	SV_{DD}	—
SVDD12	SerDes Core Logic Supply	A22	—	SV_{DD}	—
SVDD11	SerDes Core Logic Supply	B2	—	SV_{DD}	—
SVDD10	SerDes Core Logic Supply	B3	—	SV_{DD}	—
SVDD09	SerDes Core Logic Supply	B8	—	SV_{DD}	—
SVDD08	SerDes Core Logic Supply	B12	—	SV_{DD}	—
SVDD07	SerDes Core Logic Supply	B16	—	SV_{DD}	—
SVDD06	SerDes Core Logic Supply	B20	—	SV_{DD}	—
SVDD05	SerDes Core Logic Supply	C17	—	SV_{DD}	—
SVDD04	SerDes Core Logic Supply	D1	—	SV_{DD}	—
SVDD03	SerDes Core Logic Supply	E4	—	SV_{DD}	—
SVDD02	SerDes Core Logic Supply	F2	—	SV_{DD}	—
SVDD01	SerDes Core Logic Supply	H1	—	SV_{DD}	—
XVDD12	SerDes Transceiver Supply	C4	—	XV_{DD}	—
XVDD11	SerDes Transceiver Supply	C9	—	XV_{DD}	—
XVDD10	SerDes Transceiver Supply	C13	—	XV_{DD}	—
XVDD09	SerDes Transceiver Supply	C19	—	XV_{DD}	—
XVDD08	SerDes Transceiver Supply	D7	—	XV_{DD}	—
XVDD07	SerDes Transceiver Supply	D11	—	XV_{DD}	—
XVDD06	SerDes Transceiver Supply	D15	—	XV_{DD}	—
XVDD05	SerDes Transceiver Supply	D21	—	XV_{DD}	—
XVDD04	SerDes Transceiver Supply	E22	—	XV_{DD}	—
XVDD03	SerDes Transceiver Supply	F5	—	XV_{DD}	—
XVDD02	SerDes Transceiver Supply	G4	—	XV_{DD}	—
XVDD01	SerDes Transceiver Supply	H6	—	XV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LVDD05	Ethernet Controller 1 and 2 Supply	C26	—	LV_{DD}	—
LVDD04	Ethernet Controller 1 and 2 Supply	E26	—	LV_{DD}	—
LVDD03	Ethernet Controller 1 and 2 Supply	G20	—	LV_{DD}	—
LVDD02	Ethernet Controller 1 and 2 Supply	H20	—	LV_{DD}	—
LVDD01	Ethernet Controller 1 and 2 Supply	J20	—	LV_{DD}	—
POVDD	Fuse Programming Override Supply	U21	—	POV_{DD}	30
VDD_CA_PL78	Core Group A and Platform Supply	G9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL77	Core Group A and Platform Supply	G11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL76	Core Group A and Platform Supply	G13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL75	Core Group A and Platform Supply	G15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL74	Core Group A and Platform Supply	G17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL73	Core Group A and Platform Supply	G19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL72	Core Group A and Platform Supply	H9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL71	Core Group A and Platform Supply	H11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL70	Core Group A and Platform Supply	H13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL69	Core Group A and Platform Supply	H15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL68	Core Group A and Platform Supply	H17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL67	Core Group A and Platform Supply	H19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL66	Core Group A and Platform Supply	J9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL65	Core Group A and Platform Supply	J11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL64	Core Group A and Platform Supply	J13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL63	Core Group A and Platform Supply	J15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL62	Core Group A and Platform Supply	J17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL61	Core Group A and Platform Supply	J19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL60	Core Group A and Platform Supply	K9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL59	Core Group A and Platform Supply	K11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL58	Core Group A and Platform Supply	K13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL57	Core Group A and Platform Supply	K15	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL56	Core Group A and Platform Supply	K17	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL55	Core Group A and Platform Supply	K19	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL54	Core Group A and Platform Supply	L9	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL53	Core Group A and Platform Supply	L11	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL52	Core Group A and Platform Supply	L13	—	$V_{DD\_CA\_PL}$	37
VDD_CA_PL51	Core Group A and Platform Supply	L15	—	$V_{DD\_CA\_PL}$	37

Table 7. P2040 I/O Power Supply Estimated Values (continued)

IEEE 1588	—	LVdd (2.5V)	0.004	0.005	W	1,3,6
eLBC	32-bit, 100Mhz	BVdd (1.8V)	0.048	0.120	W	1,3,6
		BVdd (2.5V)	0.072	0.193		
		BVdd (3.3V)	0.120	0.277		
	16-bit, 100Mhz	BVdd (1.8V)	0.021	0.030	W	1,3,6
		BVdd (2.5V)	0.036	0.046		
		BVdd (3.3V)	0.057	0.076		
eSDHC	—	Ovdd (3.3V)	0.014	0.150	W	1,3,6
eSPI	—	CVdd (1.8V)	0.004	0.005	W	1,3,6
		CVdd (2.5V)	0.006	0.008		
		CVdd (3.3V)	0.010	0.013		
USB	—	USB_Vdd_3P3	0.012	0.015	W	1,3,6
I2C	—	OVdd (3.3V)	0.002	0.003	W	1,3,6
DUART	—	OVdd (3.3V)	0.006	0.008	W	1,3,6
GPIO	x8	OVdd (1.8V)	0.005	0.006	W	1,3,4,6
		OVdd (2.5V)	0.007	0.009		
		OVdd (3.3V)	0.009	0.011		
Others (Reset, System Clock, JTAG & Misc)	—	OVdd (3.3V)	0.003	0.015	W	1,3,4,6

Note:

1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load.
4. GPIO's are supported on 1.8 V, 2.5 V and 3.3 V rails as specified in the hardware specification.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guranteed current.
7. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configuration combination possible for the device. To get the XVDD power numbers, the user should add the combined lanes to match to the total SerDes lanes used, not simply multiply the power numbers by the number of lanes.

2.7 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 17. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit[1]	Note
Required assertion time of $\overline{\text{PORESET}}$	1	—	ms	3
Required input assertion time of $\overline{\text{HRESET}}$	32	—	SYSCLKs	1, 2
Input setup time for POR configs with respect to negation of $\overline{\text{PORESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Note:
1. SYSCLK is the primary clock input for the device.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1, “Power-On Reset Sequence,” in the chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. Refer to Section 2.2, “Power Up Sequencing.”

Table 18. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

2.8 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 19. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (For example exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

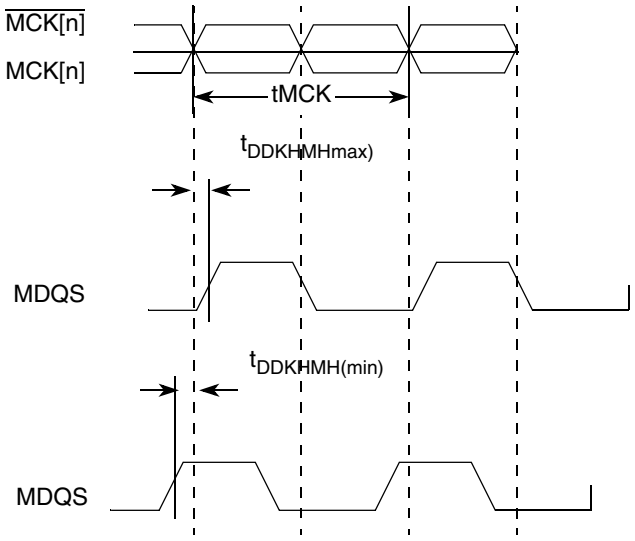

Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

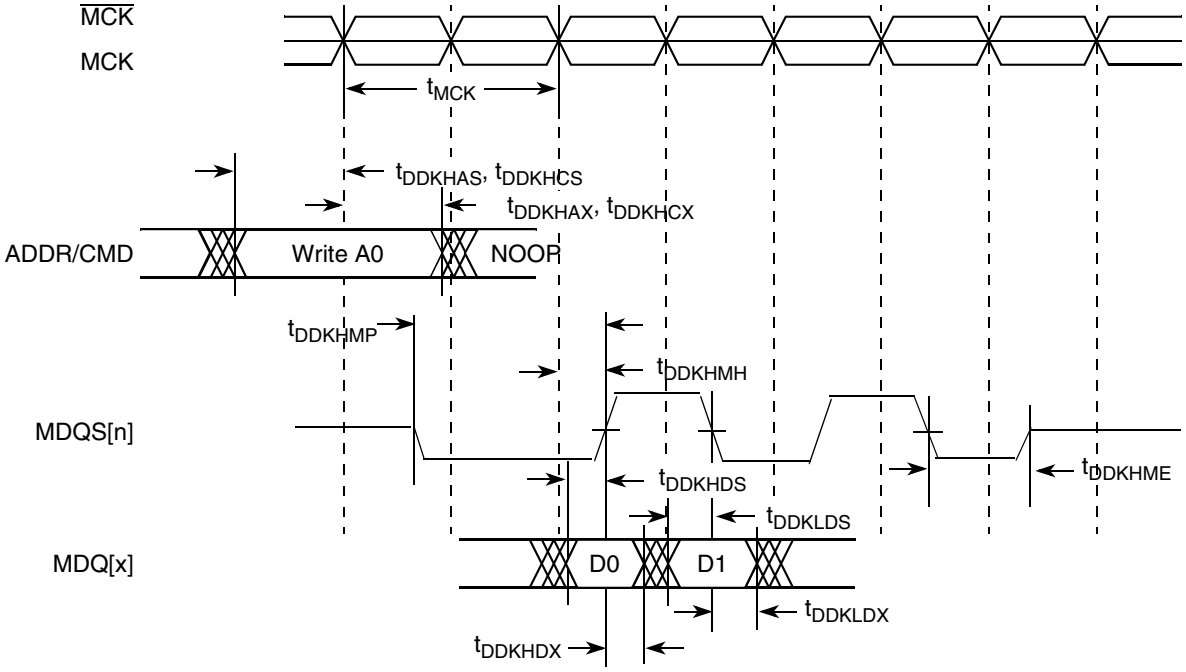

Figure 11. DDR3 and DDR3L Output Timing Diagram

2.12.2.2 RGMII AC Timing Specifications

This table shows the RGMII AC timing specifications.

Table 37. RGMII AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Note:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300ppm.

Table 41. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

This table shows the eTSEC IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 42. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.12.5 eTSEC IEEE Std 1588 AC Specifications

This table provides the eTSEC IEEE 1588 AC timing specifications.

Table 43. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	6.4	—	$T_{RX\_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.5	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

2.14 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 46. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 47. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 1.8 V.

Table 48. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.14.2 Enhanced Local Bus AC Timing Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

This figure shows the eLBC AC test load.

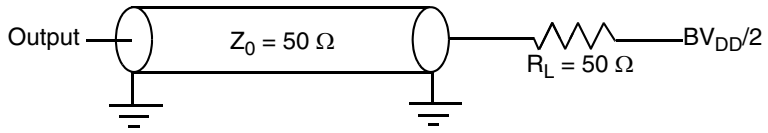

Figure 20. Enhanced Local Bus AC Test Load

2.14.2.1 Local Bus AC Timing Specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table provides the eLBC timing specifications.

Table 49. Enhanced Local Bus Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—

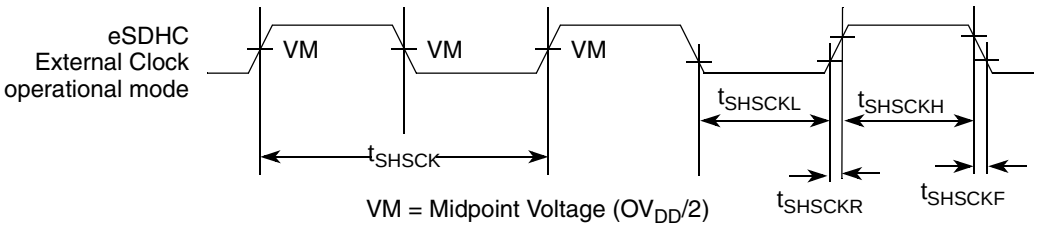

Figure 23. eSDHC Clock Input Timing Diagram

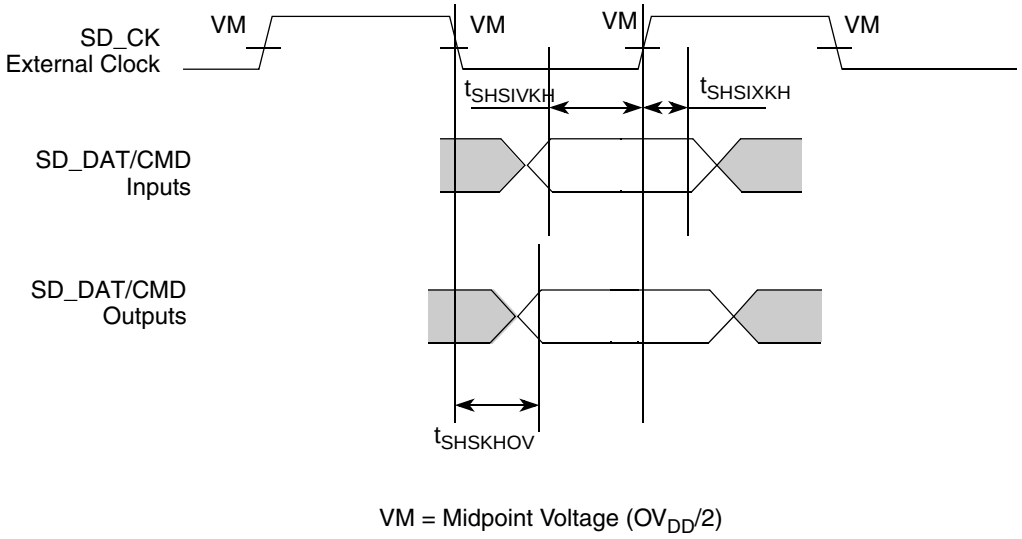

Figure 24. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.16 Multicore Programmable Interrupt Controller (MPIC) Specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC DC specifications

This table provides the DC electrical characteristics for the MPIC interface.

Table 52. MPIC DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

This figure provides the JTAG clock input timing diagram.

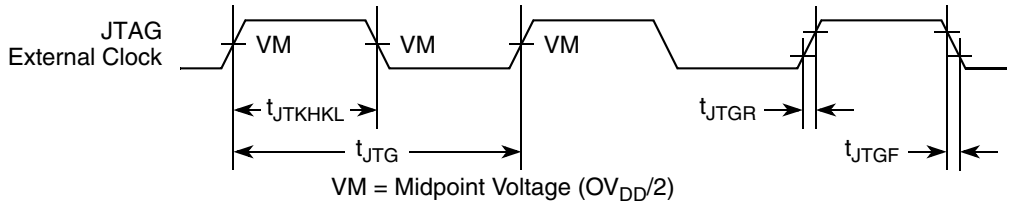

Figure 26. JTAG Clock Input Timing Diagram

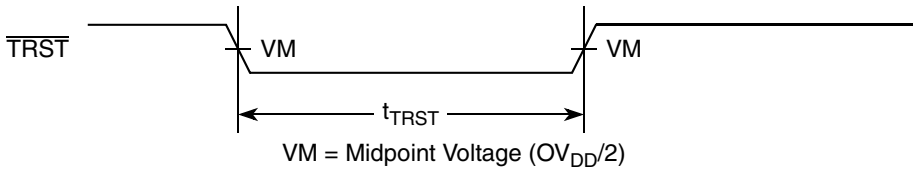

Figure 27. $\overline{\text{TRST}}$ Timing Diagram

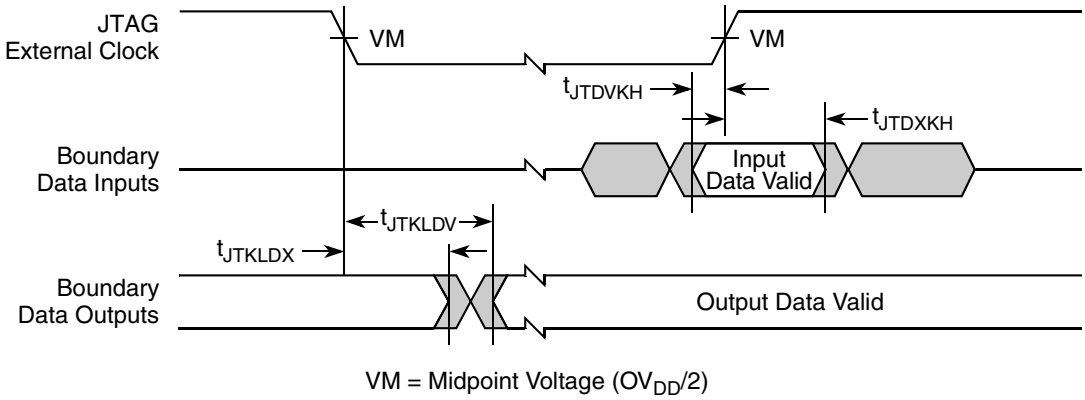

Figure 28. Boundary-Scan Timing Diagram

2.18 I²C

This section describes the DC and AC electrical characteristics for the I^2C interface.

2.18.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 56. I^2C DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2

- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.20.5.3 Serial RapidIO Clocking Requirements for SD_REF_CLK*n* and SD_REF_CLK*n*

SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for various SerDes Serial RapidIO configurations based on the RCW configuration field SRDS_PRTCL. Serial RapidIO is not supported on SerDes banks 2.

For more information on these specifications, see Section 2.20.2, "SerDes Reference Clocks."

2.20.5.4 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.20.5.4.1 DC Serial RapidIO Timing Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud and XX ps at 5 GBaud.

This table defines the transmitter DC specifications for Serial RapidIO operating at XV_{DD} = 1.5 V or 1.8 V.

Table 70. Serial RapidIO Transmitter DC Timing Specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output voltage	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.20.5.4.2 DC Serial RapidIO Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

Table 87. SGMII DC Transmitter Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output differential voltage[2, 3, 4] (XV_{DD-Typ} at 1.5 V and 1.8 V)	$\|V_{OD}\|$	320	500.0	725.0	mV	B(1-2)TECR(lane)0[AMP_RED] =0b000000
		293.8	459.0	665.6		B(1-2)TECR(lane)0[AMP_RED] =0b000010
		266.9	417.0	604.7		B(1-2)TECR(lane)0[AMP_RED] =0b000101
		240.6	376.0	545.2		B(1-2)TECR(lane)0[AMP_RED] =0b001000
		213.1	333.0	482.9		B(1-2)TECR(lane)0[AMP_RED] =0b001100
		186.9	292.0	423.4		B(1-2)TECR(lane)0[AMP_RED] =0b001111
		160.0	250.0	362.5		B(1-2)TECR(lane)0[AMP_RED] =0b010011
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Note:

1. This does not align to DC-coupled SGMII.
2. V_{OD}| = |V_{SD_TXn} – $V_{\overline{SD\_TXn}}$|. |V_{OD}| is also referred to as output differential peak voltage. $V_{TX-DIFFp-p}$ = 2*|V_{OD}|.
3. Example amplitude reduction setting for SGMII on SerDes bank 1 lane E: B1TECRE0[AMP_RED] = 0b000010 for an output differential voltage of 459 mV typical.
4. The |V_{OD}| value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.5 V or 1.8 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD_TX*n* and $\overline{\text{SD\_TX}n}$.

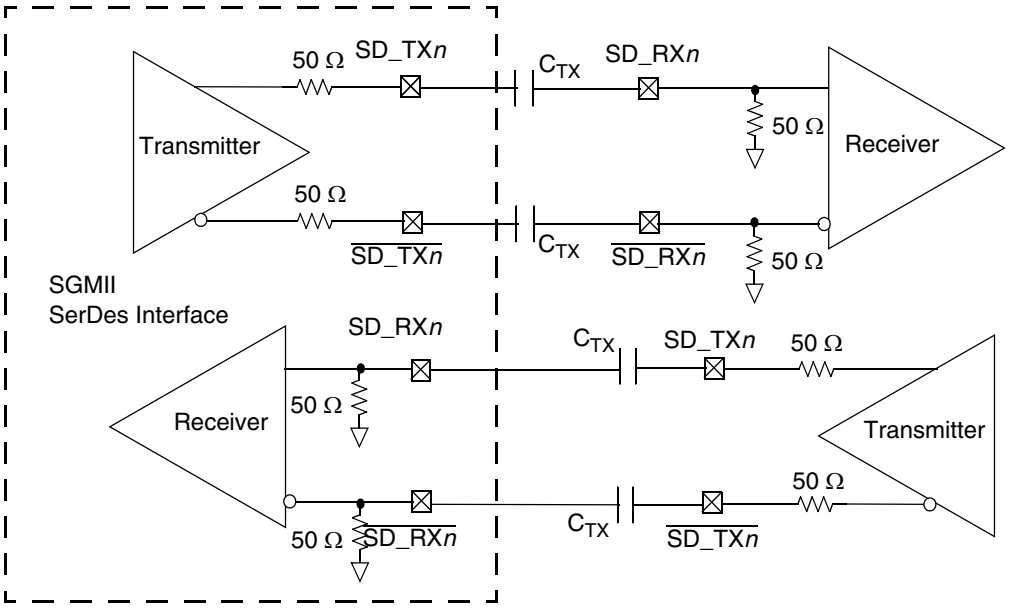

Figure 44. 4-Wire AC-Coupled SGMII Serial Link Connection Example

Table 89. SGMII DC Receiver Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 2.20.4.4, "PCI Express DC Physical Layer Receiver Specifications," and Section 2.20.4.5.2, "PCI Express AC Physical Layer Receiver Specifications," for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1–3)GCR(lane)1[REIDL_CTL] bit field.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 90. SGMII 2.5x Receiver DC Timing Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:
1. Measured at the receiver.

2.20.8.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.20.8.2.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 91. SGMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	1
Unit interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	—
Unit interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
AC coupling capacitor	C_{TX}	10		200	nF	2

Note:
1. See Figure 42 for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.20.8.2.2 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$) respectively, as depicted in this figure.

3.1.4 e500mc Core Complex PLL Select

The clock frequency of each the e500mc core 0–3 complex is determined by the binary value of the RCW field CC*n*_PLL_SEL. These tables describe the supported ratios for each core complex 0–3, where each individual core complex can select a frequency from the table.

Table 96. e500mc Core Complex [0,1] PLL Select

Binary Value of C*n*_PLL_SEL for n=[0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0001	CC1 PLL /2
0100	CC2 PLL /1
All Others	Reserved

Table 97. e500mc Core Complex [2,3] PLL Select

Binary Value of C*n*_PLL_SEL for n=[0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0100	CC2 PLL /1
0101	CC2 PLL /2
All Others	Reserved

3.1.5 DDR Controller PLL Ratios

The single DDR memory controller complexes can be asynchronous to the platform, depending on configuration.

Table 98 describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in this table. This ratio is determined by the binary value of the RCW configuration field MEM_PLL_RAT[10:14].

The RCW configuration field MEM_PLL_CFG[8:9] must be set to MEM_PLL_CFG[8:9] = 0b01 if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in Table 98 for asynchronous DDR clock ratios; otherwise, set MEM_PLL_CFG[8:9] = 0b00.

NOTE

The RCW Configuration field DDR_SYNC (bit 184) must be set to 0b0 for asynchronous mode.

The RCW Configuration field DDR_RATE (bit 232) must be set to b’0 for asynchronous mode

The RCW Configuration field DDR_RSV0 (bit 234) must be set to b’0 for all ratios.

Table 98. Asynchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:SYSCLK Ratio	Set MEM_PLL_CFG = 01 for SYSCLK Freq[1]
0_0101	5:1	>96.7 MHz
0_0110	6:1	>80.6 MHz
0_1000	8:1	>120.9 MHz
0_1001	9:1	>107.4 MHz
0_1010	10:1	>96.7 MHz
0_1100	12:1	>80.6 MHz
0_1101	13:1	>74.4 MHz
1_0000	16:1	>60.4 MHz
1_0010	18:1	>53.7 MHz
All Others	Reserved	—

Note:

1. Set RCW field MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock (SYSCLK) frequency is greater than the given cutoff; otherwise, set to 0b00 for a frequency that is less than or equal to the cutoff.

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 99. Synchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:Platform CLK Ratio	Set MEM_PLL_CFG=01 for Platform CLK Freq[1]
0_0001	1:1	>600 MHz
All Others	Reserved	—

Note:

1. Set MEM_PLL_CFG=0b01 if the applied DDR PLL reference clock (Platform clock) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

5 Security Fuse Processor

The device implements the QorIQ platform's Trust Architecture supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power Up Sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} must be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part Numbering Nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature. Not all possible combinations of part numbers implied by the part numbering scheme are supported. For a list of available part numbers, contact your Freescale Sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 107. Part Numbering Nomenclature

p	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temp. Range**	**Encryption**	**Package Type**	**CPU Freq**	**DDR Data Rate**	**Die Revision**
P = 45 nm	1–5	01 = 1 core 02 = 2 cores 04 = 4 cores	0–9	P = Prototype N = Industrial qualification	S = Std temp X = Extended temp (–40 to 105C)	E = SEC present N = SEC not present	1 = FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	F = 667 MHz H = 800 MHz K = 1000 MHz M = 1200 MHz	L = 1067 MT/s M = 1200 MT/s	A = Rev 1.0 B = Rev 1.1 C = Rev 2.0

6.2 Orderable Part Numbers Addressed by this Document

This table provides the Freescale orderable part numbers addressed by this document for the chip.