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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FCPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p2041nxn7mmc

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Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ63	Data	AD28	I/O	GV_{DD}	—
MECC0	Error Correcting Code	AH2	I/O	GV_{DD}	—
MECC1	Error Correcting Code	AF3	I/O	GV_{DD}	—
MECC2	Error Correcting Code	AG5	I/O	GV_{DD}	—
MECC3	Error Correcting Code	AH5	I/O	GV_{DD}	—
MECC4	Error Correcting Code	AG1	I/O	GV_{DD}	—
MECC5	Error Correcting Code	AG2	I/O	GV_{DD}	—
MECC6	Error Correcting Code	AH4	I/O	GV_{DD}	—
MECC7	Error Correcting Code	AF5	I/O	GV_{DD}	—
$\overline{\text{MAPAR\_ERR}}$	Address Parity Error	AH8	I	GV_{DD}	4
MAPAR_OUT	Address Parity Out	AG15	O	GV_{DD}	—
MDM0	Data Mask	Y2	O	GV_{DD}	—
MDM1	Data Mask	AC7	O	GV_{DD}	—
MDM2	Data Mask	AD8	O	GV_{DD}	—
MDM3	Data Mask	AD5	O	GV_{DD}	—
MDM4	Data Mask	AE17	O	GV_{DD}	—
MDM5	Data Mask	AH25	O	GV_{DD}	—
MDM6	Data Mask	AF22	O	GV_{DD}	—
MDM7	Data Mask	AE26	O	GV_{DD}	—
MDM8	Data Mask	AF4	O	GV_{DD}	—
MDQS0	Data Strobe	AA2	I/O	GV_{DD}	—
MDQS1	Data Strobe	AD3	I/O	GV_{DD}	—
MDQS2	Data Strobe	AE9	I/O	GV_{DD}	—
MDQS3	Data Strobe	AD1	I/O	GV_{DD}	—
MDQS4	Data Strobe	AD18	I/O	GV_{DD}	—
MDQS5	Data Strobe	AG24	I/O	GV_{DD}	—
MDQS6	Data Strobe	AE23	I/O	GV_{DD}	—
MDQS7	Data Strobe	AE28	I/O	GV_{DD}	—
MDQS8	Data Strobe	AH3	I/O	GV_{DD}	—
$\overline{\text{MDQS0}}$	Data Strobe	AA1	I/O	GV_{DD}	—
$\overline{\text{MDQS1}}$	Data Strobe	AD4	I/O	GV_{DD}	—
$\overline{\text{MDQS2}}$	Data Strobe	AD9	I/O	GV_{DD}	—
$\overline{\text{MDQS3}}$	Data Strobe	AD2	I/O	GV_{DD}	—
$\overline{\text{MDQS4}}$	Data Strobe	AD17	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND030	Ground	AB10	—	—	—
GND029	Ground	AB11	—	—	—
GND028	Ground	AB12	—	—	—
GND027	Ground	AB15	—	—	—
GND026	Ground	AB22	—	—	—
GND025	Ground	AC5	—	—	—
GND024	Ground	AC17	—	—	—
GND023	Ground	AC20	—	—	—
GND022	Ground	AC26	—	—	—
GND021	Ground	AD12	—	—	—
GND020	Ground	AD15	—	—	—
GND019	Ground	AE2	—	—	—
GND018	Ground	AE5	—	—	—
GND017	Ground	AE8	—	—	—
GND016	Ground	AE11	—	—	—
GND015	Ground	AE15	—	—	—
GND014	Ground	AE18	—	—	—
GND013	Ground	AE21	—	—	—
GND012	Ground	AE24	—	—	—
GND011	Ground	AE27	—	—	—
GND010	Ground	AF13	—	—	—
GND009	Ground	AF14	—	—	—
GND008	Ground	AG4	—	—	—
GND007	Ground	AG7	—	—	—
GND006	Ground	AG10	—	—	—
GND005	Ground	AG19	—	—	—
GND004	Ground	AG22	—	—	—
GND003	Ground	AG25	—	—	—
GND002	Ground	AH12	—	—	—
GND001	Ground	AH15	—	—	—
XGND12	SerDes Transceiver GND	C5	—	—	—
XGND11	SerDes Transceiver GND	C7	—	—	—
XGND10	SerDes Transceiver GND	C11	—	—	—
XGND09	SerDes Transceiver GND	C15	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD_CA_PL	Core Group A and Platform Vdd Sense	H8	—	—	8
SENSEVDD_CB	Core Group B Vdd Sense	AB16	—	—	8
USB1_VDD_3P3	USB1 PHY Transceiver 3.3 V Supply	M23	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3 V Supply	J23	—	—	—
USB1_VDD_1P0	USB1 PHY PLL 1.0 V Supply	L22	—	—	—
USB2_VDD_1P0	USB2 PHY PLL 1.0 V Supply	K22	—	—	—
Analog Signals					
MVREF	SSTL_1.5/1.35 Reference Voltage	W7	I	$GV_{DD}/2$	—
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	E21	I	200Ω (±1%) to XV_{DD}	21
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	F7	I	200Ω (±1%) to SV_{DD}	22
TEMP_ANODE	Temperature Diode Anode	V5	—	internal diode	9
TEMP_CATHODE	Temperature Diode Cathode	U6	—	internal diode	9
USB2_IBIAS_REXT	USB PHY2 Reference Bias Current Generation	K23	—	GND	32
USB1_IBIAS_REXT	USB PHY1 Reference Bias Current Generation	L23	—	GND	32
USB2_VDD_1P8_DECAP	USB2 PHY 1.8 V Output to External Decap	K24	—	GND	33
USB1_VDD_1P8_DECAP	USB1 PHY 1.8 V Output to External Decap	L24	—	GND	33
No Connection Pins					
NC03	No Connection	W4	—	—	11
NC04	No Connection	W3	—	—	11
NC05	No Connection	W1	—	—	11
NC06	No Connection	H7	—	—	11
NC07	No Connection	G7	—	—	11
NC08	No Connection	F20	—	—	11
NC09	No Connection	F19	—	—	11
NC10	No Connection	F18	—	—	11
NC11	No Connection	F16	—	—	11
NC12	No Connection	F13	—	—	11

Table 2. Absolute Operating Conditions[1] (continued)

Parameter	Symbol	Max Value	Unit	Note

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. $(C,X,B,G,L,O)V_{IN}$ may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 7.
8. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
9. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
10. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Note
Core Group A (cores 0–1) and platform supply voltage (Silicon Rev 1.0)	$V_{DD\_CA\_PL}$	1.0 ± 50 mV	V	4, 5
Core Group B (cores 2–3) supply voltage (Silicon Rev 1.0)	V_{DD_CB}	1.0 ± 50 mV	V	4, 5
Core Group A (cores 0–1), Core Group B (cores 2–3) and platform supply voltage (Silicon Rev 1.1)	$V_{DD\_CA\_CB\_PL}$	1.0 ± 50 mV	V	4, 5
PLL supply voltage (core, platform, DDR)	AV_{DD}	1.0 ± 50 mV	V	—
PLL supply voltage (SerDes)	AV_{DD_SRDS}	1.0 ± 50 mV	V	—
Fuse programming override supply	POV_{DD}	1.5 ± 75 mV	V	2
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	3.3 ± 165 mV	V	—
eSPI, eSDHC, GPIO	CV_{DD}	3.3 ± 165 mV 2.5 ± 125 mV 1.8 ± 90 mV	V	—
DDR DRAM I/O voltage DDR3 DDR3L	GV_{DD}	 1.5 ± 75 mV 1.35 ± 67 mV	V	—

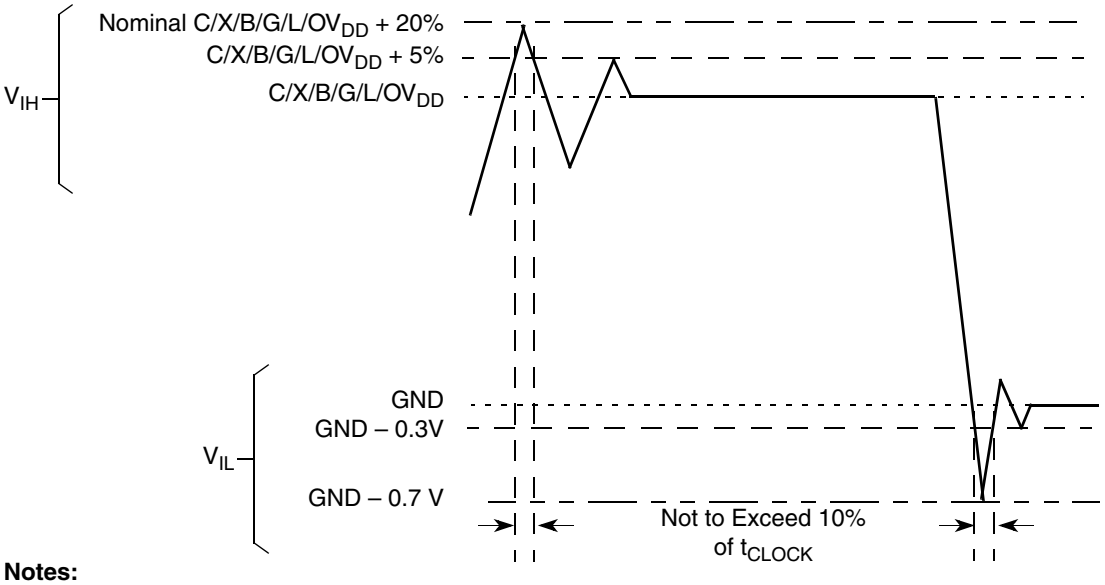
Table 3. Recommended Operating Conditions (continued)

Parameter	Symbol	Recommended Value	Unit	Note

Note:

1. POV_{DD} must be supplied 1.5 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Up Sequencing."
2. Selecting RGMII limits LV_{DD} to 2.5 V.
3. Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.
4. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
5. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Notes:

t_{CLOCK} refers to the clock period associated with the respective interface:

- For I^2C, t_{CLOCK} refers to SYSCLK.
- For DDR GV_{DD}, t_{CLOCK} refers to D*n*_MCK.
- For eSPI CV_{DD}, t_{CLOCK} refers to SPI_CLK.
- For eLBC BV_{DD}, t_{CLOCK} refers to LCLK.
- For SerDes XV_{DD}, t_{CLOCK} refers to SD_REF_CLK.
- For dTSEC LV_{DD}, t_{CLOCK} refers to EC_GTX_CLK125.
- For JTAG OV_{DD}, t_{CLOCK} refers to TCK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$

The core and platform voltages must always be provided at nominal 1.0 V. See Table 3 for the actual recommended core voltage conditions. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. CV_{DD}, BV_{DD}, OV_{DD}, and LV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied $MV_{REF}n$ signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.5/SSTL_1.35 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

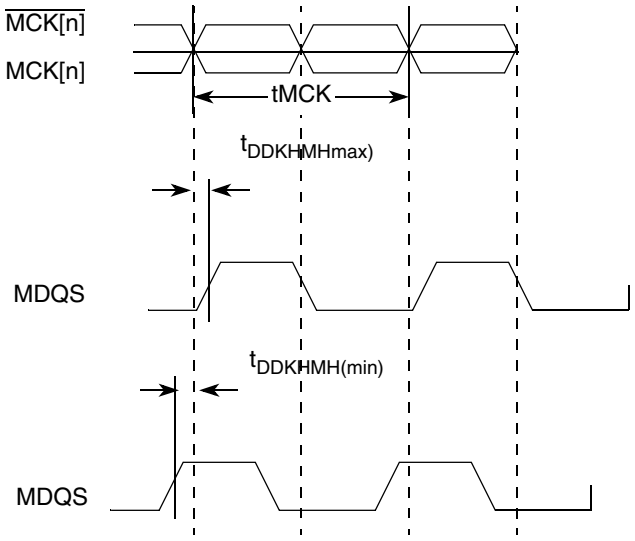


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

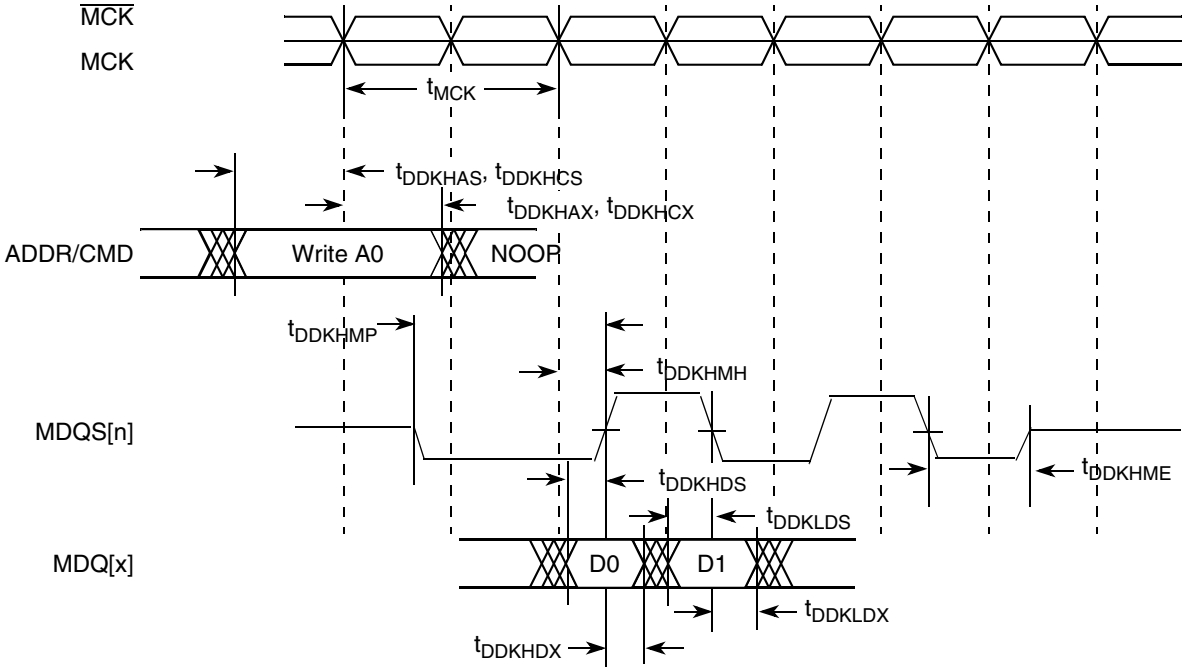


Figure 11. DDR3 and DDR3L Output Timing Diagram

This figure provides the AC test load for the DDR3 and DDR3L controller bus.

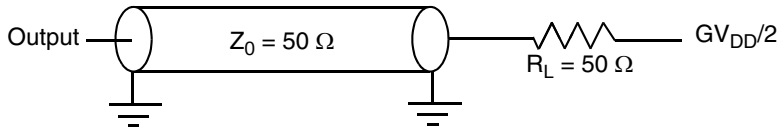


Figure 12. DDR3 and DDR3L Controller Bus AC Test Load

2.9.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 and DDR3L SDRAM controller interface. This figure shows the differential timing specification.

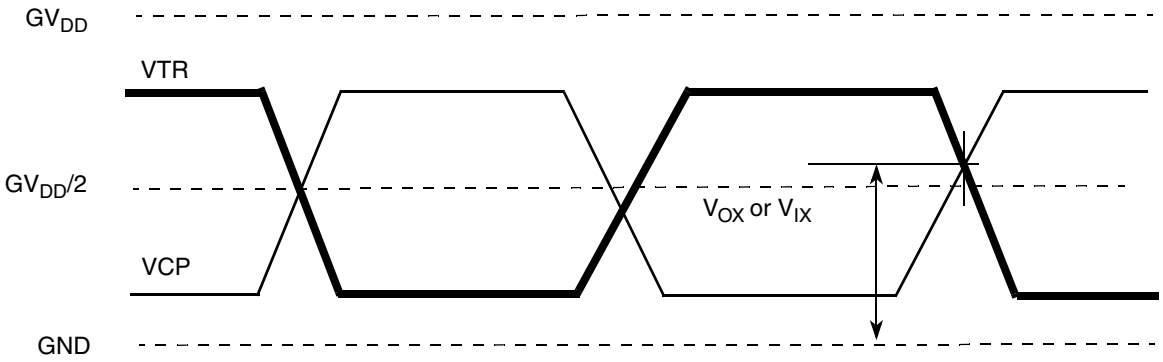


Figure 13. DDR3 and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

This table provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 28. DDR3 SDRAM Differential Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.150$	$0.5 \times GV_{DD} + 0.150$	V	—
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.115$	$0.5 \times GV_{DD} + 0.115$	V	—

Note:
1. I/O drivers are calibrated before making measurements.

This table provides the DDR3L differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 29. DDR3L SDRAM Differential Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit	Note
Input AC differential cross-point voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.135$	$0.5 \times GV_{DD} + 0.135$	V	—
Output AC differential cross-point voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.105$	$0.5 \times GV_{DD} + 0.105$	V	—

Note:
1. I/O drivers are calibrated before making measurements.

Table 41. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

This table shows the eTSEC IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 42. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.12.5 eTSEC IEEE Std 1588 AC Specifications

This table provides the eTSEC IEEE 1588 AC timing specifications.

Table 43. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	6.4	—	$T_{RX\_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.5	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Table 43. eTSEC IEEE 1588 AC Timing Specifications (continued)

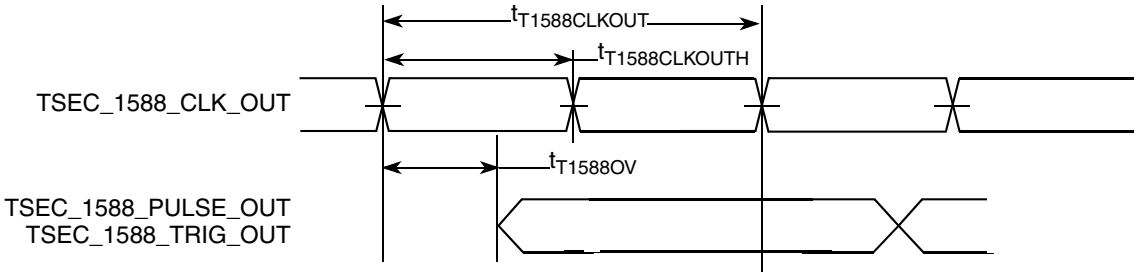
For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

Figure 18. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

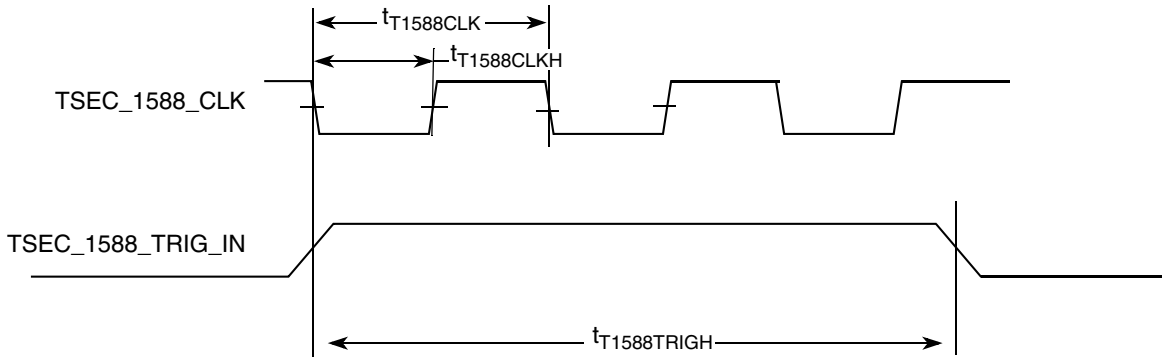


Figure 19. eTSEC IEEE 1588 Input AC Timing

This figure shows the AC timing diagram of the local bus interface.

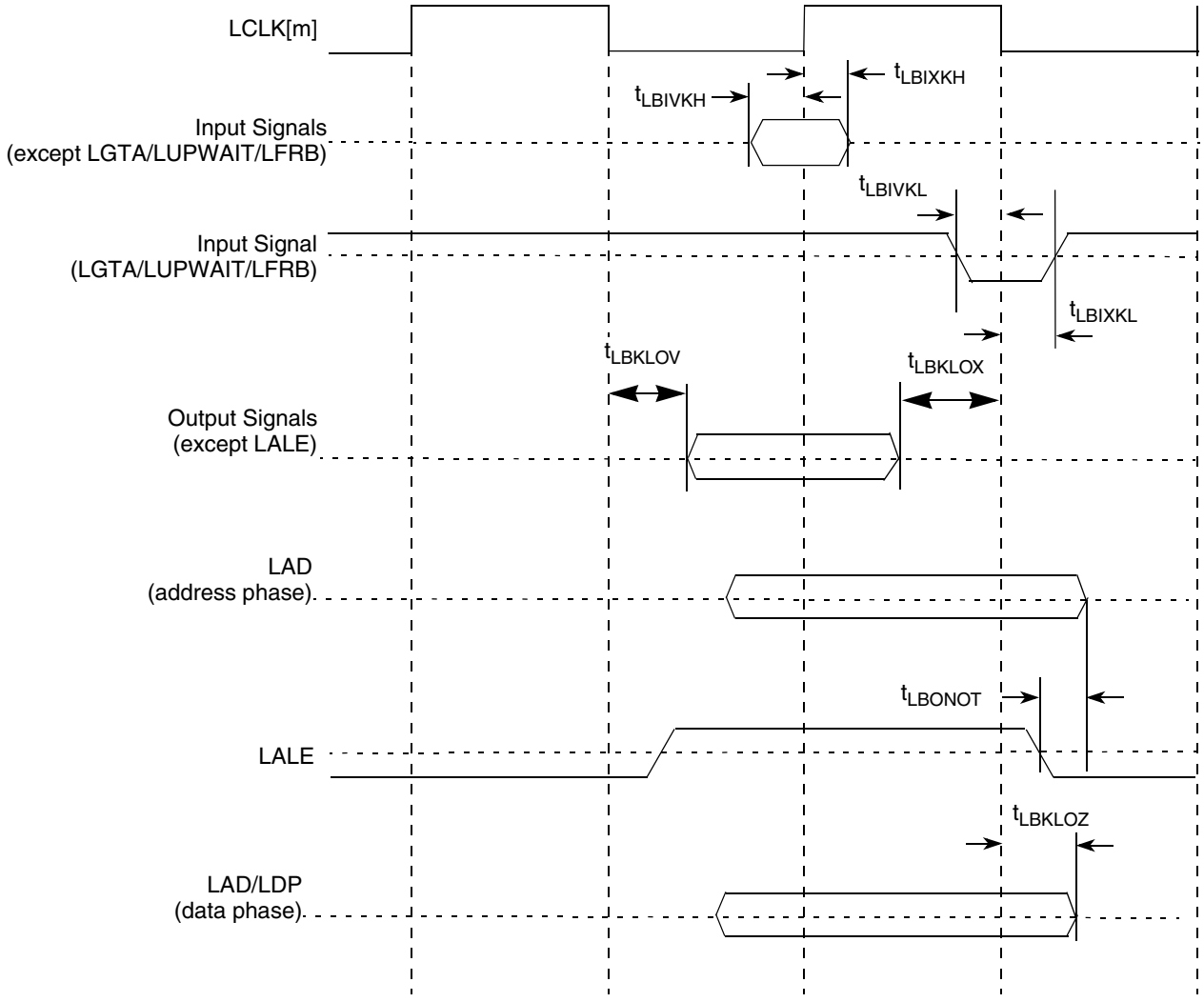


Figure 21. Enhanced Local Bus Signals

Figure 22 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

This figure provides the JTAG clock input timing diagram.

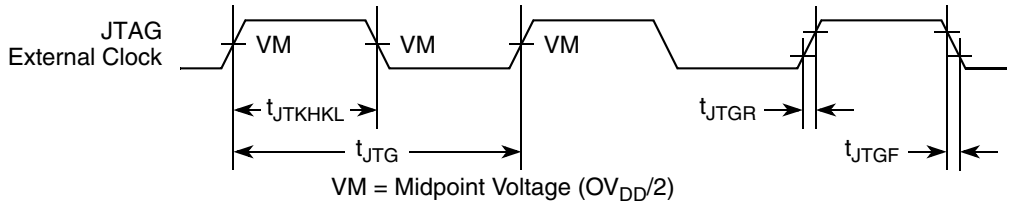


Figure 26. JTAG Clock Input Timing Diagram

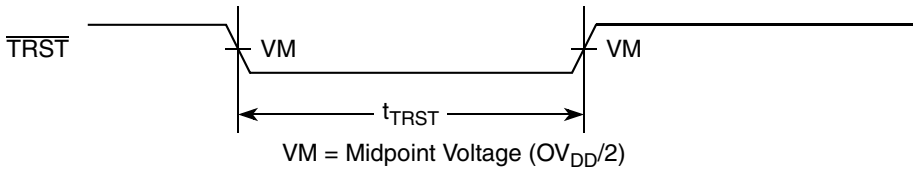


Figure 27. $\overline{\text{TRST}}$ Timing Diagram

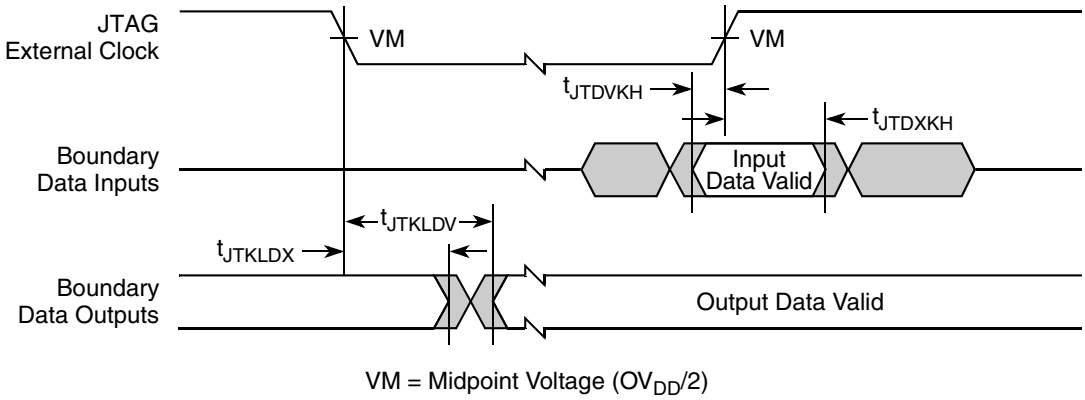


Figure 28. Boundary-Scan Timing Diagram

2.18 I²C

This section describes the DC and AC electrical characteristics for the I^2C interface.

2.18.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 56. I^2C DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2

2.19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

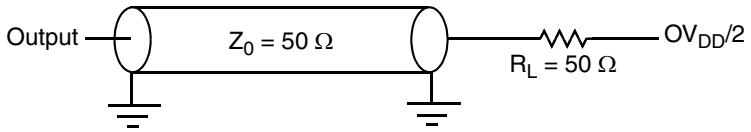


Figure 31. GPIO AC Test Load

2.20 High-Speed Serial Interfaces (HSSI)

The device features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, Aurora, and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 37 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{\overline{SD\_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{TD}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and $\overline{SD\_REF\_CLK1}$ for SerDes bank1 and SD_REF_CLK2 and $\overline{SD\_REF\_CLK2}$ for SerDes bank2.

SerDes banks 1–2 may be used for various combinations of the following IP blocks based on the RCW configuration field SRDS_PRTCL:

- SerDes bank 1: PCI Express 1/2/3, sRIO1/2, SGMII (1.25 Gbps only).
- SerDes bank 2: PCI Express3, SGMII (1.25 or 3.125 GBaud), SATA or Aurora.

The following sections describe the SerDes reference clock requirements and provide application information.

2.20.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

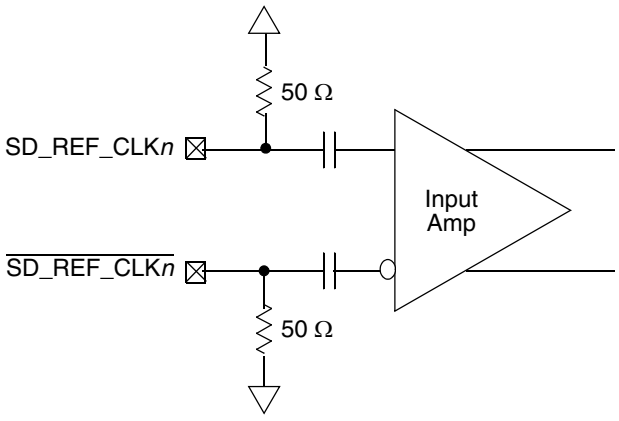


Figure 33. Receiver of SerDes Reference Clocks

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). This figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

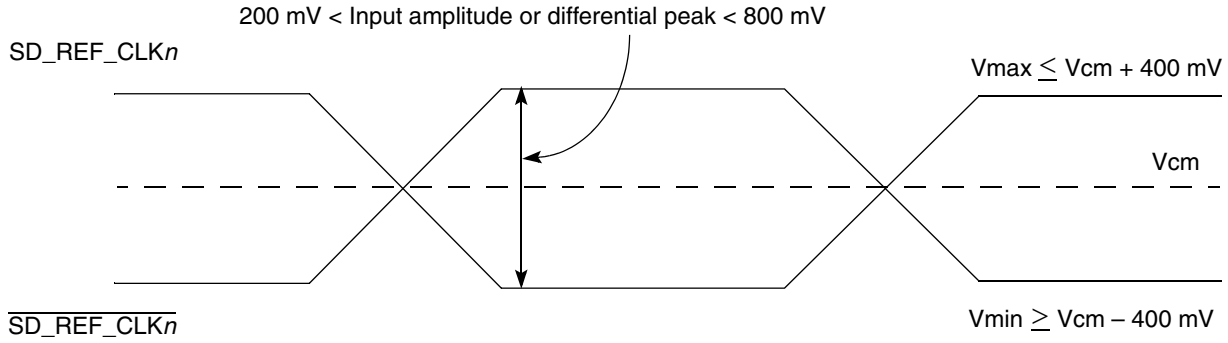


Figure 35. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SD_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}n}$ either left unconnected or tied to ground.
  — The SD_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}n}$) through the same source impedance as the clock input (SD_REF_CLK*n*) in use.

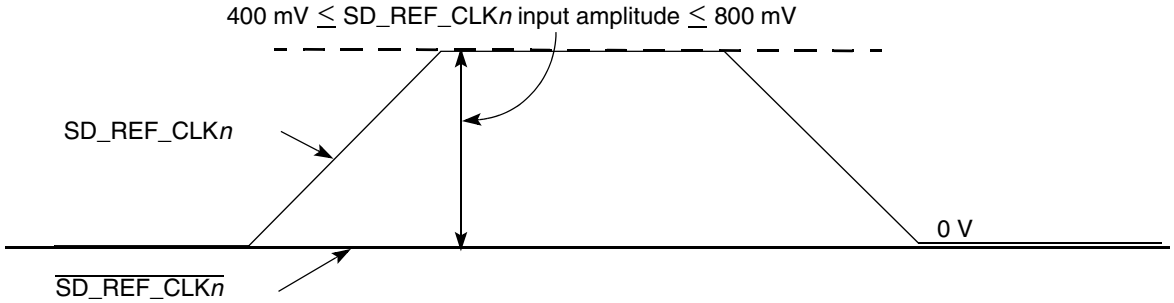


Figure 36. Single-Ended Reference Clock Input DC Requirements

Table 83. Gen1i/1.5 G Transmitter (Tx) AC Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 84. Gen 2i/3 G Transmitter (Tx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.3	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:
1. Measured at Tx output pins peak-to-peak phase variation, random data pattern

2.20.7.4 AC Differential Receiver Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 85. Gen 1i/1.5G Receiver (Rx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.35	UI p-p	1

Note:
1. Measured at receiver.

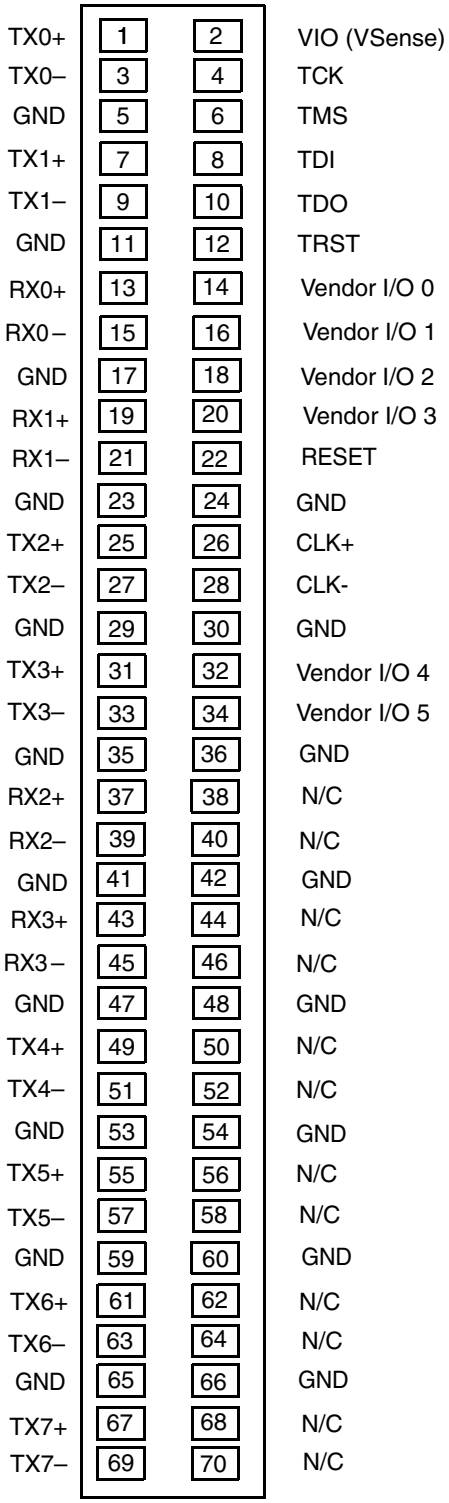
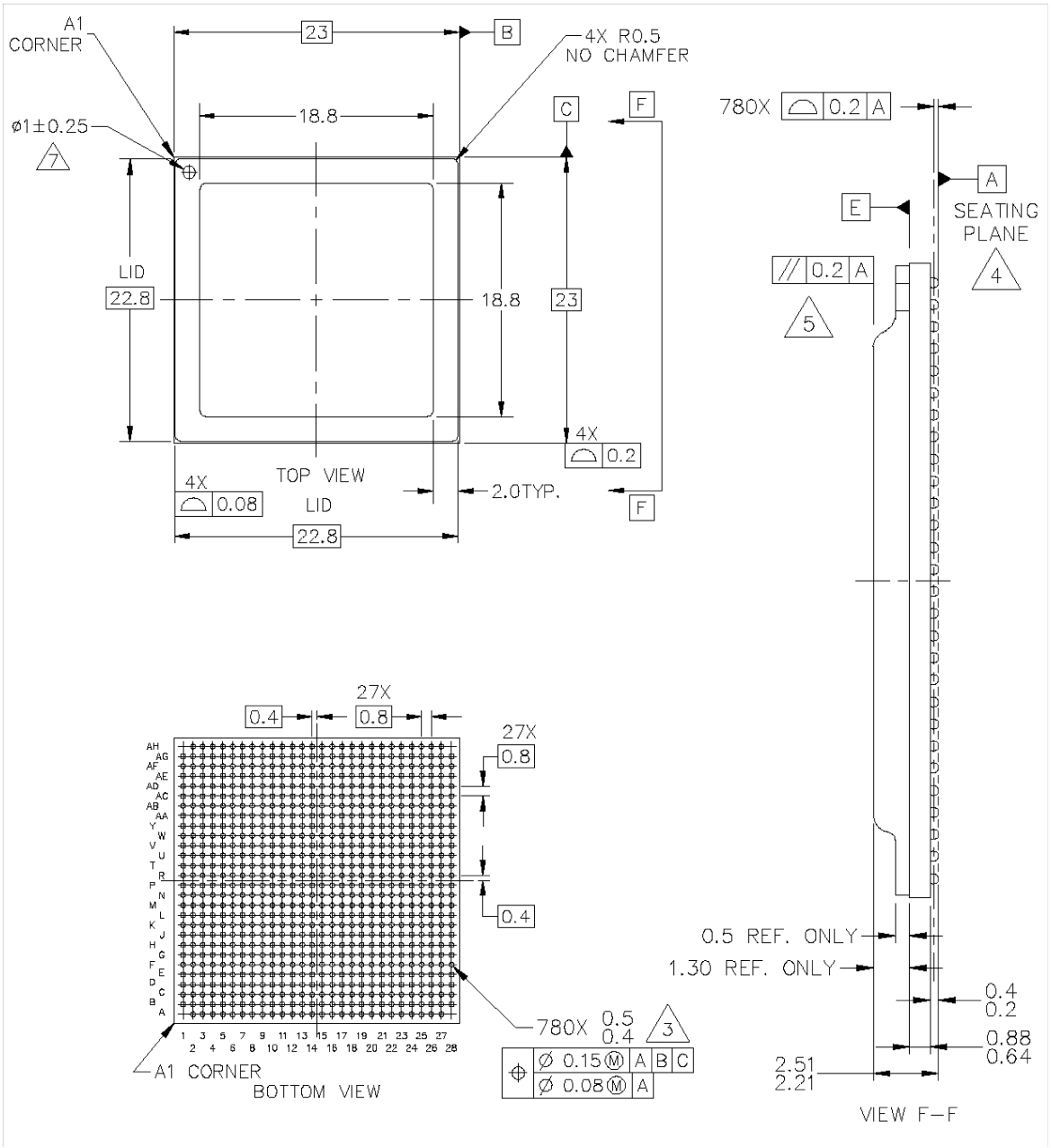


Figure 57. Aurora 70 Pin Connector Duplex Pinout

4.2 Mechanical Dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the device.



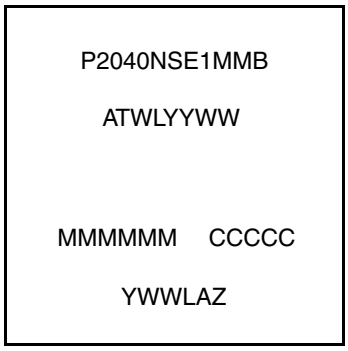
Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement excludes any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
7. Pin 1 thru hole is centered within foot area.

Figure 63. Mechanical Dimensions of the FC-PBGA with Full Lid

6.2.1 Part Marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Notes:

P2040NSE1MMB is the orderable part number. See Table 107 for details.

ATWLYYWW is the test traceability code.
MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

Figure 64. Part Marking for FC-PBGA Device

7 Revision History

This table provides a revision history for this document.

Table 108. Revision History

Rev. Number	Date	Description
2	02/2013	• In Table 7, “P2040 I/O Power Supply Estimated Values,” updated the USB power supply with USB_Vdd_3P3 and updated the typical value with “0.003” in the Others (Reset, System Clock, JTAG & Misc.) row. • In Table 8, “Device AVDD Power Dissipation,” removed V_{DD_LP} from table. • Added Table 10, “VDD_LP Power Dissipation.” • In Table 53, “MPIC Input AC Timing Specifications,” added Trust inputs AC timing and footnote 2. • In Table 93, “Processor Clocking Specifications,” updated footnote 8 with Rev 1.1 silicon. • In Table 107, “Part Numbering Nomenclature,” added “C” in the Die Revision collumn. • In Section 6.2, “Orderable Part Numbers Addressed by this Document,” added the device part numbers for Rev 2.0 silicon.

Table 108. Revision History (continued)

Rev. Number	Date	Description
1	09/2012	• In Table 1, “Pin List by Bus”, added note for pin V_{DD_LP} • Updated Table 8, “Device AVDD Power Dissipation”. • In Table 12, “SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V)”, updated the input current max value and added input capacitance max value. • In Table 51, “eSDHC AC Timing Specifications”, updated input setup times from 5 ns to 2.5 ns. • In Section 3.1.6.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces”, updated the note that the “PCI Express link width” refers to “a single port”. • In Section 4.1, “Package Parameters for the FC-PBGA”, updated the solder ball composition and module height. • In Section 4.2, “Mechanical Dimensions of the FC-PBGA”, updated the figure for the mechanical dimensions. • In Section 3.6, “Connection Recommendations”, removed the sentence “If no aspect of Trust Architecture is to be used, all Trust Architecture pins can be tied to GND.”
0	06/2012	Initial public release