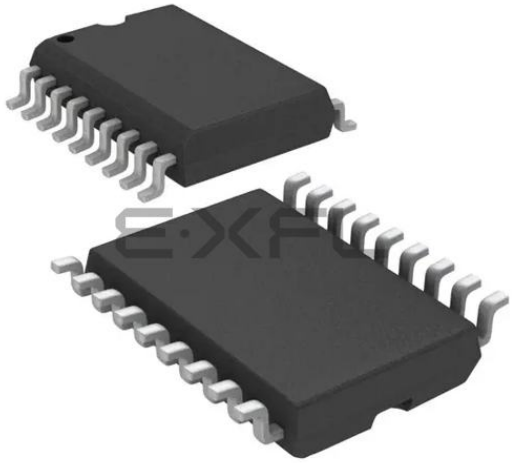

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f1330-e-so

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TABLE 1-2: PIC18F1230/1330 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP, SOIC	SSOP	QFN			
MCLR/VPP/RA5/FLTA	4	4	1			Master Clear (input), programming voltage (input) or Fault detect input.
MCLR				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				I	Analog	Programming voltage input.
RA5				I	ST	Digital input.
FLTA(1)				I	ST	Fault detect input for PWM.
RA7/OSC1/CLKI/ T1OSI/FLTA	16	18	21			Oscillator crystal, external clock input, Timer1 oscillator input or Fault detect input.
RA7				I/O	ST	Digital I/O.
OSC1				I	Analog	Oscillator crystal input or external clock source input.
CLKI				I	—	External clock source input.
T1OSI(2)				I	Analog	Timer1 oscillator input.
FLTA(1)				I	ST	Fault detect input for PWM.
RA6/OSC2/CLKO/ T1OSO/T1CKI/AN3	15	17	20			Oscillator crystal, clock output, Timer1 oscillator output or analog input.
RA6				I/O	ST	Digital I/O.
OSC2				O	—	Oscillator crystal output or external clock source input.
CLKO				O	—	External clock source output.
T1OSO(2)				O	—	Timer1 oscillator output.
TICKI(2)				I	ST	Timer1 clock input.
AN3				I	Analog	Analog input 3.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Placement of FLTA depends on the value of Configuration bit, FLTAMX, of CONFIG3H.

2: Placement of T1OSI and T1OSO/T1CKI depends on the value of Configuration bit, T1OSCMX, of CONFIG3H.

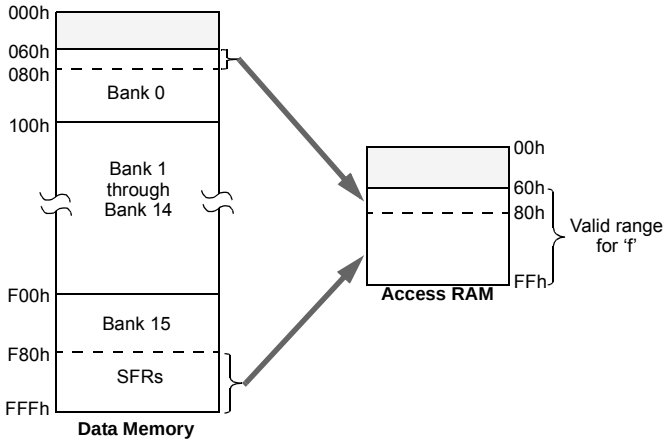
FIGURE 6-8: COMPARING ADDRESSING OPTIONS FOR BIT-ORIENTED AND BYTE-ORIENTED INSTRUCTIONS (EXTENDED INSTRUCTION SET ENABLED)

EXAMPLE INSTRUCTION: `ADDWF, f, d, a` (Opcode: `0010 01da ffff ffff`)

When 'a' = 0 and f ≥ 60h:

The instruction executes in Direct Forced mode. 'f' is interpreted as a location in the Access RAM between 060h and 0FFh. This is the same as locations 060h to 07Fh (Bank 0) and F80h to FFFh (Bank 15) of data memory.

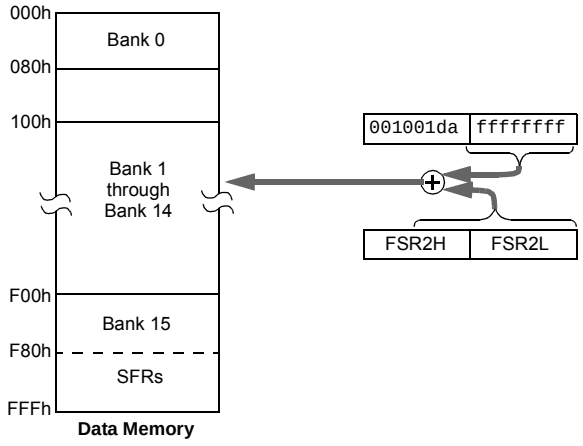
Locations below 60h are not available in this addressing mode.



When 'a' = 0 and f ≤ 5Fh:

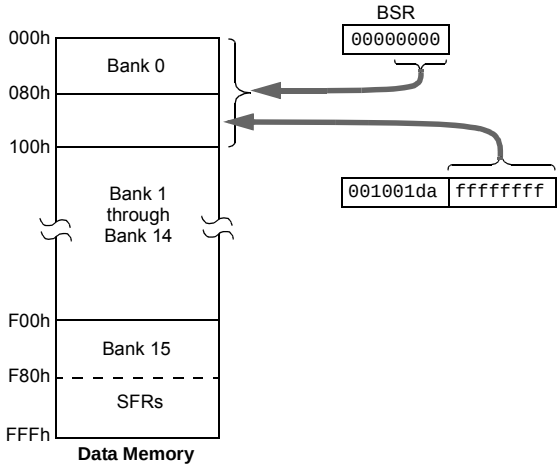
The instruction executes in Indexed Literal Offset mode. 'f' is interpreted as an offset to the address value in FSR2. The two are added together to obtain the address of the target register for the instruction. The address can be anywhere in the data memory space.

Note that in this mode, the correct syntax is now:
`ADDWF [k], d`
where 'k' is the same as 'f'.



When 'a' = 1 (all values of f):

The instruction executes in Direct mode (also known as Direct Long mode). 'f' is interpreted as a location in one of the 16 banks of the data memory space. The bank is designated by the Bank Select Register (BSR). The address can be in any implemented bank in the data memory space.



7.2.2 TABLAT – TABLE LATCH REGISTER

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch register is used to hold 8-bit data during data transfers between program memory and data RAM.

7.2.3 TBLPTR – TABLE POINTER REGISTER

The Table Pointer (TBLPTR) register addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low-order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the device ID, the user ID and the Configuration bits.

The Table Pointer register, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways based on the table operation. These operations are shown in Table 7-1. These operations on the TBLPTR only affect the low-order 21 bits.

7.2.4 TABLE POINTER BOUNDARIES

TBLPTR is used in reads, writes and erases of the Flash program memory.

When a TBLRD is executed, all 22 bits of the TBLPTR determine which byte is read from program memory into TABLAT.

When the timed write to program memory begins (via the WR bit), the 19 MSbs of the TBLPTR (TBLPTR<21:3>) determine which program memory block of 8 bytes is written to. The Table Pointer register's three LSBs (TBLPTR<2:0>) are ignored. For more detail, see **Section 7.5 "Writing to Flash Program Memory"**.

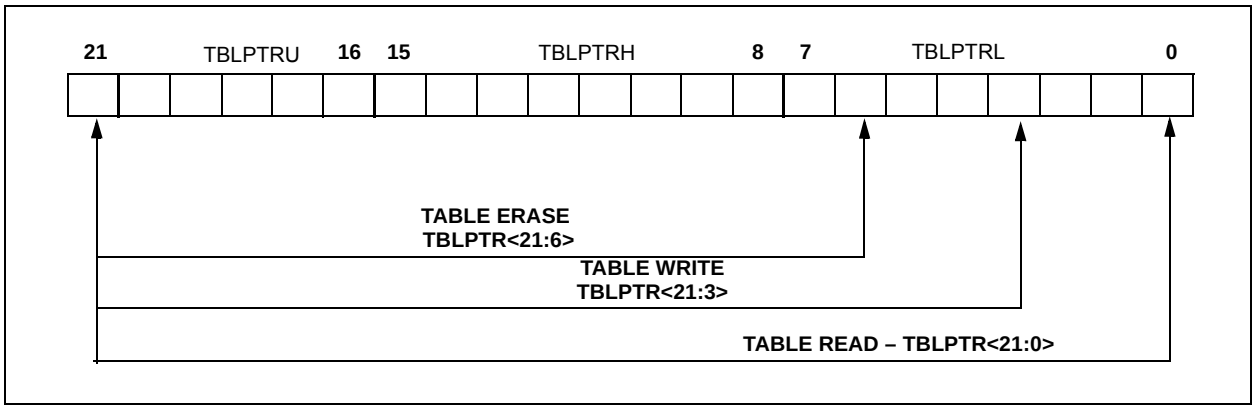
When an erase of program memory is executed, the 16 MSbs of the Table Pointer register (TBLPTR<21:6>) point to the 64-byte block that will be erased. The Least Significant bits (TBLPTR<5:0>) are ignored.

Figure 7-3 describes the relevant boundaries of TBLPTR based on Flash program memory operations.

TABLE 7-1: TABLE POINTER OPERATIONS WITH TBLRD AND TBLWT INSTRUCTIONS

Example	Operation on Table Pointer
TBLRD* TBLWT*	TBLPTR is not modified
TBLRD*+ TBLWT*+	TBLPTR is incremented after the read/write
TBLRD*- TBLWT*-	TBLPTR is decremented after the read/write
TBLRD+* TBLWT+*	TBLPTR is incremented before the read/write

FIGURE 7-3: TABLE POINTER BOUNDARIES BASED ON OPERATION



10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

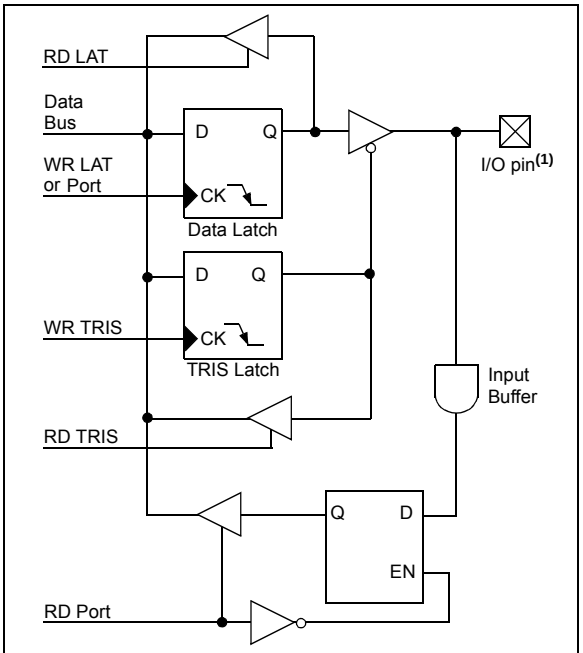
Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Output Latch register)

The Output Latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Output Latch (LATA) register is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

Pins RA6 and RA7 are multiplexed with the main oscillator pins; they are enabled as oscillator or I/O pins by the selection of the main oscillator in the Configuration register (see **Section 20.1 "Configuration Bits"** for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as '0'.

The RA0 pin is multiplexed with one of the analog inputs, one of the external interrupt inputs, one of the interrupt-on-change inputs and one of the analog comparator inputs to become RA0/AN0/INT0/KBI0/CMP0 pin.

The RA1 pin is multiplexed with one of the analog inputs, one of the external interrupt inputs and one of the interrupt-on-change inputs to become RA1/AN1/INT1/KBI1 pin.

Pins RA2 and RA3 are multiplexed with the Enhanced USART transmission and reception input (see **Section 20.1 "Configuration Bits"** for details).

The RA4 pin is multiplexed with the Timer0 module clock input, one of the analog inputs and the analog VREF+ input to become the RA4/T0CKI/AN2/VREF+ pin.

The Fault detect input for PWM $\overline{\text{FLTA}}$ is multiplexed with pins RA5 and RA7. Its placement is decided by clearing or setting the FLTAMX bit of Configuration Register 3H.

Note:	On a Power-on Reset, RA0, RA1, RA4 and RA5 are configured as analog inputs and read as '0'. RA2 and RA3 are configured as digital inputs.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

```
CLRF    PORTA   ; Initialize PORTA by
                ; clearing output
                ; data latches
CLRF    LATA    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   07h     ; Configure A/D
MOVWF   ADCON1  ; for digital inputs
MOVWF   07h     ; Configure comparators
MOVWF   CMCON   ; for digital input
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISA   ; Set RA<7:6,3:0> as inputs
                ; RA<5:4> as outputs
```

TABLE 10-1: PORTA I/O SUMMARY

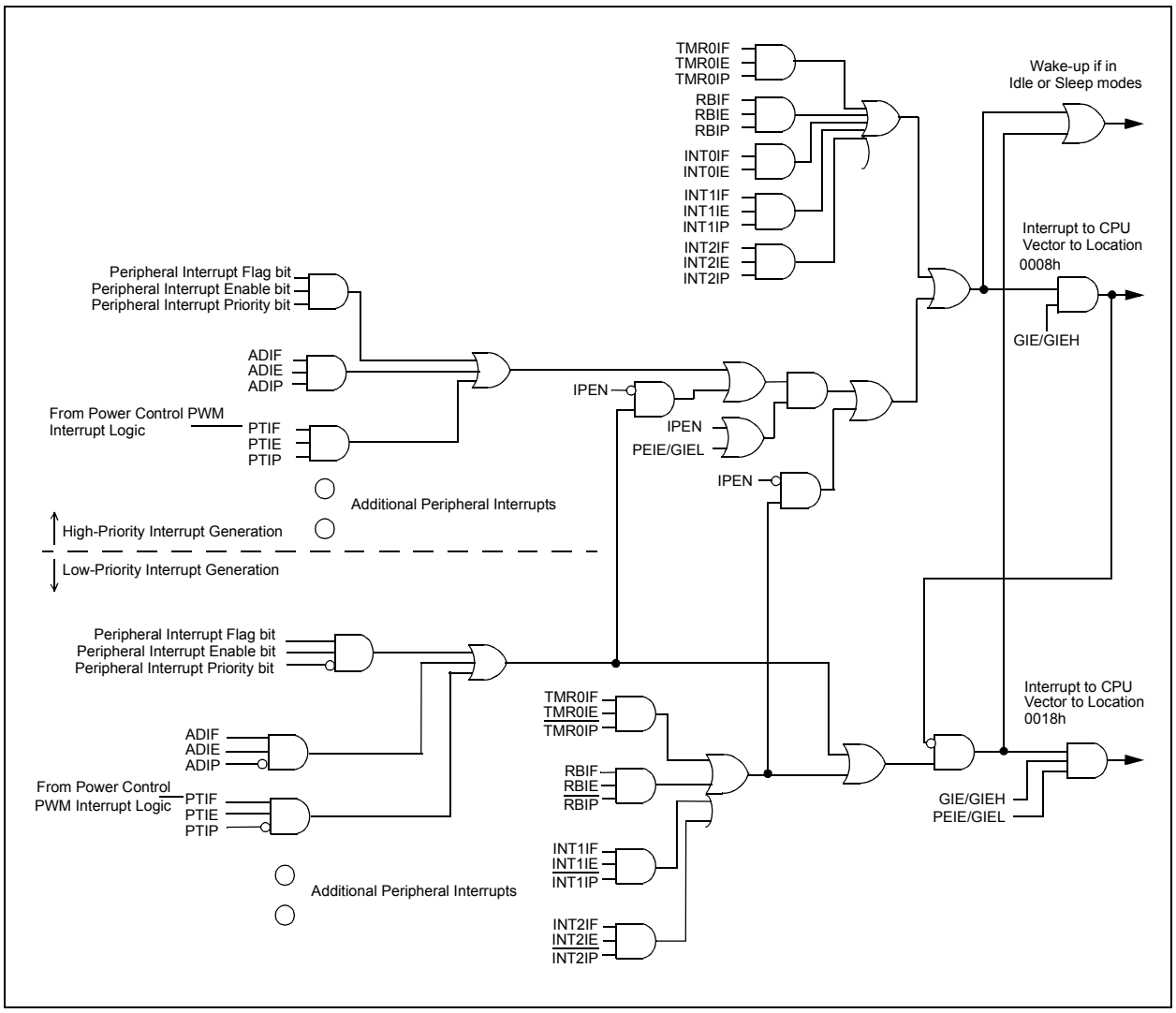
Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0/INT0/ KBI0/CMP0	RA0	0	O	DIG	LATA<0> data output; not affected by analog input.
		1	I	TTL	PORTA<0> data input; disabled when analog input enabled.
	AN0	1	I	ANA	Analog input 0.
	INT0	1	I	ST	External interrupt 0.
	KBI0	1	I	TTL	Interrupt-on-change pin.
	CMP0	1	I	ANA	Comparator 0 input.
RA1/AN1/INT1/ KBI1	RA1	0	O	DIG	LATA<1> data output; not affected by analog input.
		1	I	TTL	PORTA<1> data input; disabled when analog input enabled.
	AN1	1	I	ANA	Analog input 1.
	INT1	1	I	ST	External interrupt 1.
	KBI1	1	I	TTL	Interrupt-on-change pin.
RA2/TX/CK	RA2	0	O	DIG	LATA<2> data output; not affected by analog input. Disabled when CV_{REF} output enabled.
		1	I	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CV_{REF} output enabled.
	TX	0	0	DIG	EUSART asynchronous transmit.
	CK	0	O	DIG	EUSART synchronous clock.
		1	I	ST	
RA3/RX/DT	RA3	0	O	DIG	LATA<3> data output; not affected by analog input.
		1	I	TTL	PORTA<3> data input; disabled when analog input enabled.
	RX	1	I	ANA	EUSART asynchronous receive.
	DT	0	O	DIG	EUSART synchronous data.
		1	I	TTL	
RA4/T0CKI/AN2/ $V_{REF}+$	RA4	0	O	DIG	LATA<4> data output.
		1	I	ST	PORTA<4> data input; default configuration on POR.
	T0CKI	1	I	ST	Timer0 external clock input.
	AN2	1	I	ANA	Analog input 2.
	$V_{REF}+$	1	I	ANA	A/D reference voltage (high) input.
$\overline{MCLR}/V_{PP}$/RA5/ $\overline{FLTA}$	$\overline{MCLR}$	1	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
	V_{PP}	1	I	ANA	Programming voltage input.
	RA5	1	I	ST	Digital input.
	$\overline{FLTA}$(1)	1	I	ST	Fault detect input for PWM.
RA6/OSC2/CLKO/ T1OSO/T1CKI/AN3	RA6	0	O	DIG	LATA<6> data output. Enabled in RCIO, INTIO2 and ECIO modes only.
		1	I	ST	PORTA<6> data input. Enabled in RCIO, INTIO2 and ECIO modes only.
	OSC2	0	O	ANA	Oscillator crystal output or external clock source output.
	CLKO	0	O	ANA	Oscillator crystal output.
	T1OSO(2)	0	O	ANA	Timer1 oscillator output.
	T1CKI(2)	1	I	ST	Timer1 clock input.
	AN3	1	I	ANA	Analog input 3.
RA7/OSC1/CLKI/ T1OSI/$\overline{FLTA}$	RA7	0	O	DIG	LATA<7> data output. Disabled in external oscillator modes.
		1	I	TTL	PORTA<7> data input. Disabled in external oscillator modes.
	OSC1	1	I	ANA	Oscillator crystal input or external clock source input.
	CLKI	1	I	ANA	External clock source input.
	T1OSI(2)	1	I	ANA	Timer1 oscillator input.
	$\overline{FLTA}$(1)	1	I	ST	Fault detect input for PWM.

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Placement of $\overline{FLTA}$ depends on the value of Configuration bit, FLTAMX, of CONFIG3H.

2: Placement of T1OSI and T1OSO/T1CKI depends on the value of Configuration bit, T1OSCMX, of CONFIG3H.

FIGURE 11-1: PIC18 INTERRUPT LOGIC



13.1 Timer1 Operation

Timer1 can operate in one of these modes:

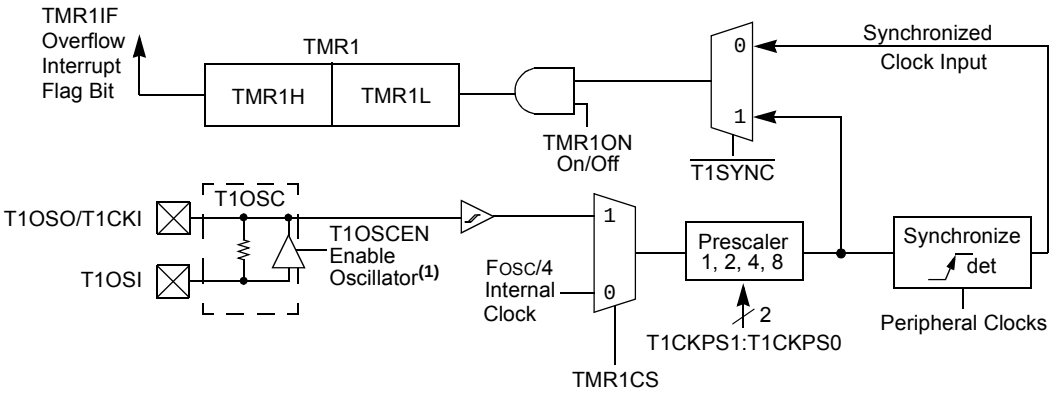
- As a timer
- As a synchronous counter
- As an asynchronous counter

The operating mode is determined by the Clock Select bit, TMR1CS (T1CON<1>).

When TMR1CS = 0, Timer1 increments every instruction cycle. When TMR1CS = 1, Timer1 increments on every rising edge of the external clock input or the Timer1 oscillator, if enabled.

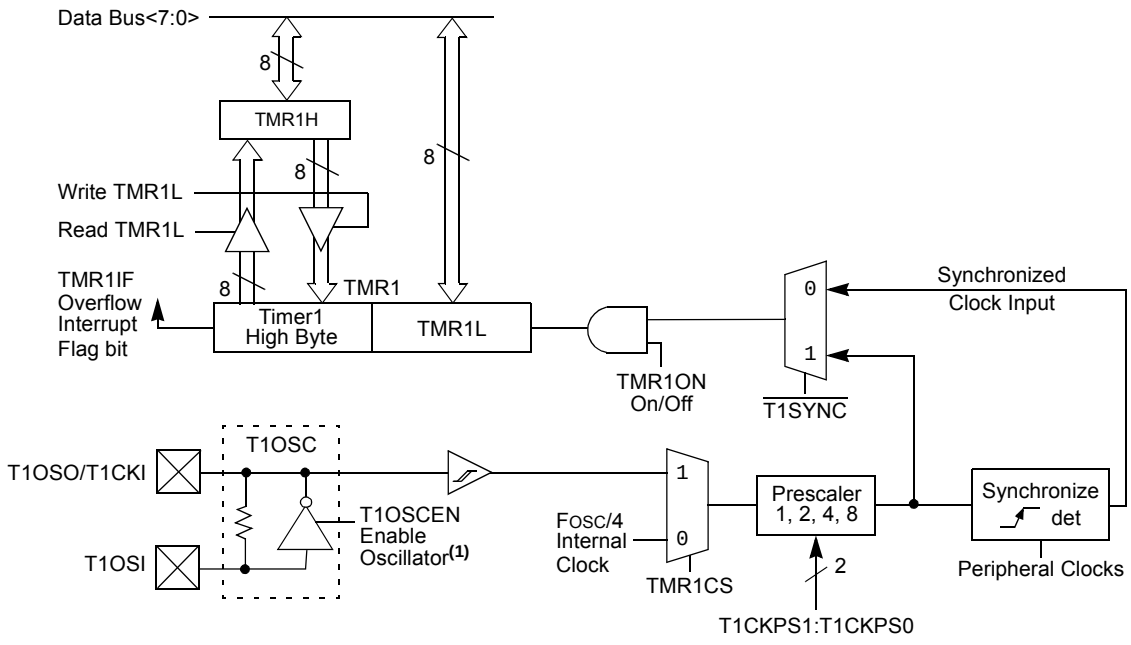
When the Timer1 oscillator is enabled (T1OSCEN is set), the T1OSI and T1OSO/T1CKI pins become inputs. That is, the corresponding TRISA bit value is ignored, and the pins are read as '0'.

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



Note 1: When enable bit T1OSCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

FIGURE 13-2: TIMER1 BLOCK DIAGRAM: 16-BIT READ/WRITE MODE



Note 1: When enable bit T1OSCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

EXAMPLE 13-1: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

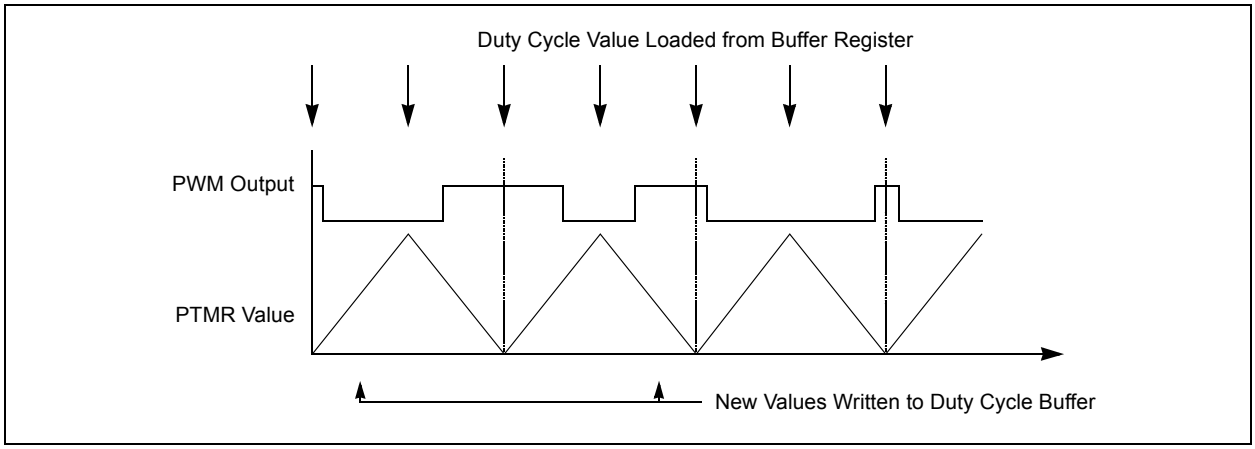
```
RTCinit
            MOVLW     0x80                  ; Preload TMR1 register pair
            MOVWF     TMR1H                 ; for 1 second overflow
            CLRF      TMR1L
            MOVLW     b'00001111'           ; Configure for external clock,
            MOVWF     T1CON                 ; Asynchronous operation, external oscillator
            CLRF      secs                  ; Initialize timekeeping registers
            CLRF      mins                  ;
            MOVLW     .12
            MOVWF     hours
            BSF       PIE1, TMR1IE          ; Enable Timer1 interrupt
            RETURN
RTCisr
            BSF       TMR1H, 7              ; Preload for 1 sec overflow
            BCF       PIR1, TMR1IF          ; Clear interrupt flag
            INCF      secs, F               ; Increment seconds
            MOVLW     .59                   ; 60 seconds elapsed?
            CPFSGT    secs
            RETURN                          ; No, done
            CLRF      secs                  ; Clear seconds
            INCF      mins, F               ; Increment minutes
            MOVLW     .59                   ; 60 minutes elapsed?
            CPFSGT    mins
            RETURN                          ; No, done
            CLRF      mins                  ; clear minutes
            INCF      hours, F              ; Increment hours
            MOVLW     .23                   ; 24 hours elapsed?
            CPFSGT    hours
            RETURN                          ; No, done
            MOVLW     .01                   ; Reset hours to 1
            MOVWF     hours
            RETURN                          ; Done
```

TABLE 13-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	47
PIR1	—	ADIF	RCIF	TXIF	CMP2IF	CMP1IF	CMP0IF	TMR1IF	49
PIE1	—	ADIE	RCIE	TXIE	CMP2IE	CMP1IE	CMP0IE	TMR1IE	49
IPR1	—	ADIP	RCIP	TXIP	CMP2IP	CMP1IP	CMP0IP	TMR1IP	49
TMR1L	Timer1 Register Low Byte								48
TMR1H	Timer1 Register High Byte								48
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	48

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

FIGURE 14-14: DUTY CYCLE UPDATE TIMES IN CONTINUOUS UP/DOWN COUNT MODE WITH DOUBLE UPDATES

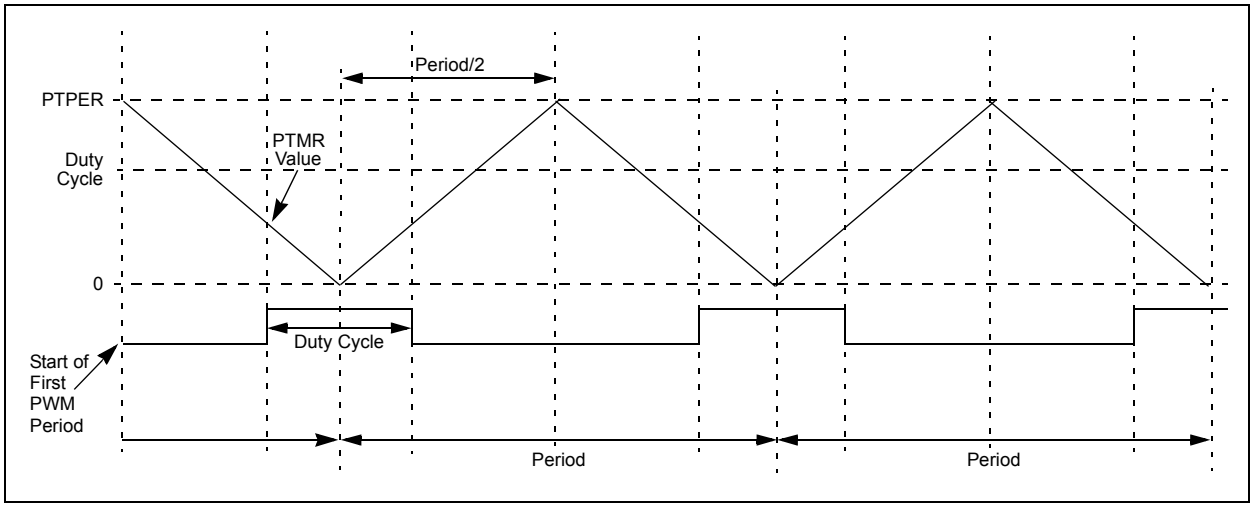


14.6.4 CENTER-ALIGNED PWM

Center-aligned PWM signals are produced by the module when the PWM time base is configured in a Continuous Up/Down Count mode (see Figure 14-15). The PWM compare output is driven to the active state when the value of the Duty Cycle register matches the value of PTMR and the PWM time base is counting downwards (PTDIR = 1). The PWM compare output will be driven to the inactive state when the PWM time base is counting upwards (PTDIR = 0) and the value in the PTMR register matches the duty cycle value. If the value in a particular Duty Cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the Duty Cycle register is equal to or greater than the value in the PTPER register.

Note:	When the PWM is started in Center-Aligned mode, the PWM Time Base Period register (PTPER) is loaded into the PWM Time Base register (PTMR) and the PTMR is configured automatically to start down counting. This is done to ensure that all the PWM signals don't start at the same time.

FIGURE 14-15: START OF CENTER-ALIGNED PWM



16.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 4 inputs for the 18/20/28-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number in PIC18F1230/1330 devices.

The module has five registers:

- A/D Result Register High Byte (ADRESH)
- A/D Result Register Low Byte (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 16-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 16-2, configures the functions of the port pins. The ADCON2 register, shown in Register 16-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 16-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTEN	—	—	—	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **SEVTEN:** Special Event Trigger Enable bit
1 = Special Event Trigger from Power Control PWM module is enabled
0 = Special Event Trigger from Power Control PWM module is disabled (default)

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3-2 **CHS1:CHS0:** Analog Channel Select bits
00 = Channel 0 (AN0)
01 = Channel 1 (AN1)
10 = Channel 2 (AN2)
11 = Channel 3 (AN3)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

17.0 COMPARATOR MODULE

The analog comparator module contains three comparators. The inputs can be selected from the analog inputs multiplexed with pins RA0, RB2 and RB3, as well as the on-chip voltage reference (see **Section 18.0 "Comparator Voltage Reference Module"**). The digital outputs are not available at the pin level and can only be read through the control register, CMCON (Register 17-1). CMCON also selects the comparator input.

REGISTER 17-1: CMCON: COMPARATOR CONTROL REGISTER

R-0	R-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C0OUT	—	—	CMEN2	CMEN1	CMEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2OUT**: Comparator 2 Output bit
1 = C2 VIN+ > C2 VIN- (CVREF)
0 = C2 VIN+ < C2 VIN- (CVREF)

bit 6 **C1OUT**: Comparator 1 Output bit
1 = C1 VIN+ > C1 VIN- (CVREF)
0 = C1 VIN+ < C1 VIN- (CVREF)-

bit 5 **C0OUT**: Comparator 0 Output bit
1 = C0 VIN+ > C0 VIN- (CVREF)
0 = C0 VIN+ < C0 VIN- (CVREF)

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **CMEN2**: Comparator 2 Enable bit
1 = Comparator 2 is enabled
0 = Comparator 2 is disabled

bit 1 **CMEN1**: Comparator 1 Enable bit
1 = Comparator 1 is enabled
0 = Comparator 1 is disabled

bit 0 **CMEN0**: Comparator 0 Enable bit
1 = Comparator 0 is enabled
0 = Comparator 0 is disabled

REGISTER 20-7: CONFIG5L: CONFIGURATION REGISTER 5 LOW (BYTE ADDRESS 300008h)

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
—	—	—	—	—	—	CP1	CP0
bit 7							bit 0

Legend:		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **CP1:** Code Protection bit (Block 1 Code Memory Area)
1 = Block 1 is not code-protected
0 = Block 1 is code-protected

bit 0 **CP0:** Code Protection bit (Block 0 Code Memory Area)
1 = Block 0 is not code-protected
0 = Block 0 is code-protected

REGISTER 20-8: CONFIG5H: CONFIGURATION REGISTER 5 HIGH (BYTE ADDRESS 300009h)

R/C-1	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
CPD	CPB	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7 **CPD:** Code Protection bit (Data EEPROM)
1 = Data EEPROM is not code-protected
0 = Data EEPROM is code-protected

bit 6 **CPB:** Code Protection bit (Boot Block Memory Area)
1 = Boot Block is not code-protected
0 = Boot Block is code-protected

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 20-15: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SWDTEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit(1)
1 = Watchdog Timer is on
0 = Watchdog Timer is off

Note 1: This bit has no effect if the Configuration bit, WDTEN, is enabled.

TABLE 20-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
RCON	IPEN	SBOREN(1)	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	48
WDTCON	—	—	—	—	—	—	—	SWDTEN(2)	48

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

Note 1: The SBOREN bit is only available when the BOREN1:BOREN0 Configuration bits = 01; otherwise, it is disabled and reads as '0'. See **Section 5.4 "Brown-out Reset (BOR)"**.

2: This bit has no effect if the Configuration bit, WDTEN, is enabled.

BNC **Branch if Not Carry**

Syntax: BNC n

Operands: -128 ≤ n ≤ 127

Operation: if Carry bit is '0',
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0011	nnnn	nnnn

Description: If the Carry bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNC Jump

Before Instruction
PC = address (HERE)
After Instruction
If Carry = 0;
PC = address (Jump)
If Carry = 1;
PC = address (HERE + 2)

BNN **Branch if Not Negative**

Syntax: BNN n

Operands: -128 ≤ n ≤ 127

Operation: if Negative bit is '0',
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0111	nnnn	nnnn

Description: If the Negative bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNN Jump

Before Instruction
PC = address (HERE)
After Instruction
If Negative = 0;
PC = address (Jump)
If Negative = 1;
PC = address (HERE + 2)

DECFSZ **Decrement f, Skip if 0**

Syntax: DECFSZ f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) – 1 → dest,
skip if result = 0

Status Affected: None

Encoding:

0010	11da	ffff	ffff

Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.
If the result is '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a two-cycle instruction.
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 22.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    DECFSZ  CNT, 1, 1
        GOTO    LOOP
CONTINUE
```
Before Instruction
PC = Address (HERE)
After Instruction
CNT = CNT – 1
If CNT = 0;
PC = Address (CONTINUE)
If CNT ≠ 0;
PC = Address (HERE + 2)

DCFSNZ **Decrement f, Skip if Not 0**

Syntax: DCFSNZ f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) – 1 → dest,
skip if result ≠ 0

Status Affected: None

Encoding:

0100	11da	ffff	ffff

Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.
If the result is not '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a two-cycle instruction.
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 22.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    DCFSNZ  TEMP, 1, 0
ZERO    :
NZERO   :
```
Before Instruction
TEMP = ?
After Instruction
TEMP = TEMP – 1
If TEMP = 0;
PC = Address (ZERO)
If TEMP ≠ 0;
PC = Address (NZERO)

23.2 DC Characteristics: Power-Down and Supply Current PIC18F1230/1330 (Industrial) PIC18LF1230/1330 (Industrial) (Continued)

PIC18LF1230/1330 (Industrial)	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC18F1230/1330 (Industrial, Extended)	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD)(2)						
	PIC18LF1230/1330	165	347	µA	-40°C	VDD = 2.0V	FOSC = 1 MHz (**RC_IDLE** mode, INTOSC source)
		175	347	µA	+25°C		
		190	347	µA	+85°C		
	PIC18LF1230/1330	250	497	µA	-40°C	VDD = 3.0V	
		270	497	µA	+25°C		
		290	497	µA	+85°C		
	All devices	500	930	µA	-40°C	VDD = 5.0V	
		520	930	µA	+25°C		
		550	930	µA	+85°C		
	Extended devices only	0.6	2.9	mA	+125°C		
	PIC18LF1230/1330	340	497	µA	-40°C	VDD = 2.0V	FOSC = 4 MHz (**RC_IDLE** mode, INTOSC source)
		350	497	µA	+25°C		
		360	497	µA	+85°C		
	PIC18LF1230/1330	520	830	µA	-40°C	VDD = 3.0V	
		540	830	µA	+25°C		
		580	830	µA	+85°C		
	All devices	1.0	1.33	mA	-40°C	VDD = 5.0V	
		1.1	1.33	mA	+25°C		
		1.1	1.33	mA	+85°C		
	Extended devices only	1.1	5.0	mA	+125°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power Timer1 oscillator selected.

4: BOR and LVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

TABLE 23-7: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 4.2V TO 5.5V)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
F10	FOSC	Oscillator Frequency Range	4	—	10	MHz	HS mode only
F11	FSYS	On-Chip VCO System Frequency	16	—	40	MHz	HS mode only
F12	t_{rc}	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13	ΔCLK	CLKO Stability (Jitter)	-2	—	+2	%	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 23-8: AC CHARACTERISTICS: INTERNAL RC ACCURACY

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial
-40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Min	Typ	Max	Units	Conditions	
	INTOSC Accuracy @ Freq = 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 31 kHz(1)						
	PIC18LF1230/1330	-2	+/-1	2	%	+25°C	VDD = 2.7-3.3V
		-5	—	5	%	-10°C to +85°C	VDD = 2.7-3.3V
		-10	+/-1	10	%	-40°C to +85°C	VDD = 2.7-3.3V
	PIC18F1230/1330	-2	+/-1	2	%	+25°C	VDD = 4.5-5.5V
		-5	—	5	%	-10°C to +85°C	VDD = 4.5-5.5V
		-10	+/-1	10	%	-40°C to +85°C	VDD = 4.5-5.5V
	INTRC Accuracy @ Freq = 31 kHz(2,3)						
	PIC18LF1230/1330	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V
	PIC18F1230/1330	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V

Legend: Shading of rows is to assist in readability of the table.

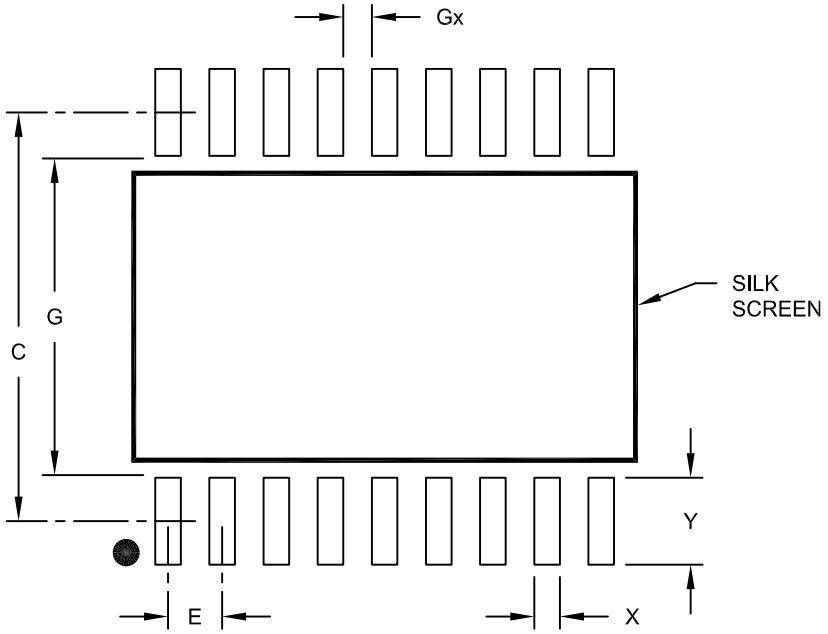
Note 1: Frequency calibrated at 25°C. OSCTUNE register can be used to compensate for temperature drift.

2: INTRC frequency after calibration.

3: Change of INTRC frequency as VDD changes.

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available