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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f1330-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.2 Other Special Features

- Memory Endurance: The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- Self-Programmability: These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- Extended Instruction Set: The PIC18F1230/1330 family introduces an optional extension to the PIC18 instruction set, which adds eight new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- Power Control PWM Module: This module provides up to six modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown on Fault detection and auto-restart to reactivate outputs once the condition has cleared.
- Enhanced Addressable USART: This serial communication module is capable of standard RS-232 operation and provides support for the LIN/J2602 bus protocol. Other enhancements include automatic Baud Rate Detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reducing code overhead.
- Extended Watchdog Timer (WDT): This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See Section 23.0 "Electrical Characteristics" for time-out periods.

1.3 Details on Individual Family Members

Devices in the PIC18F1230/1330 family are available in 18-pin, 20-pin and 28-pin packages.

The devices are differentiated from each other in one way:

1. Flash program memory (4 Kbytes for PIC18F1230, 8 Kbytes for PIC18F1330).

All other features for devices in this family are identical. These are summarized in Table 1-1.

A block diagram of the PIC18F1220/1320 device architecture is provided in Figure 1-1. The pinouts for this device family are listed in Table 1-2.

Like all Microchip PIC18 devices, members of the PIC18F1230/1330 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F1330), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF1330), function over an extended VDD range of 2.0V to 5.5V.

2.0 GUIDELINES FOR GETTING STARTED WITH PIC18F MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC18F1230/1330 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and Vss pins (see Section 2.2 "Power Supply Pins")
- All AVDD and AVss pins, regardless of whether or not the analog device features are used (see Section 2.2 "Power Supply Pins")
- MCLR pin (see Section 2.3 "Master Clear (MCLR) Pin")

These pins must also be connected if they are being used in the end application:

- PGC/PGD pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see **Section 2.4 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used

(see Section 2.5 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

Note: The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED

MINIMUM CONNECTIONS



3.7.1 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 3-2) controls several aspects of the device clock's operation, both in full power operation and in power-managed modes.

The System Clock Select bits, SCS1:SCS0, select the clock source. The available clock sources are the primary clock (defined by the FOSC3:FOSC0 Configuration bits), the secondary clock (Timer1 oscillator) and the internal oscillator block. The clock source changes immediately after one or more of the bits is written to, following a brief clock transition interval. The SCS bits are cleared on all forms of Reset.

The Internal Oscillator Frequency Select bits (IRCF2:IRCF0) select the frequency output of the internal oscillator block to drive the device clock. The choices are the INTRC source, the INTOSC source (8 MHz) or one of the frequencies derived from the INTOSC postscaler (31.25 kHz to 4 MHz). If the internal oscillator block is supplying the device clock, changing the states of these bits will have an immediate change on the internal oscillator's output. On device Resets, the default output frequency of the internal oscillator block is set at 1 MHz.

When a nominal output frequency of 31 kHz is selected (IRCF2:IRCF0 = 000), users may choose which internal oscillator acts as the source. This is done with the INTSRC bit in the OSCTUNE register (OSCTUNE<7>). Setting this bit selects INTOSC as a 31.25 kHz clock source by enabling the divide-by-256 output of the INTOSC postscaler. Clearing INTSRC selects INTRC (nominally 31 kHz) as the clock source.

This option allows users to select the tunable and more precise INTOSC as a clock source, while maintaining power savings with a very low clock speed. Regardless of the setting of INTSRC, INTRC always remains the clock source for features such as the Watchdog Timer and the Fail-Safe Clock Monitor.

The OSTS, IOFS and T1RUN bits indicate which clock source is currently providing the device clock. The OSTS bit indicates that the Oscillator Start-up Timer has timed out and the primary clock is providing the device clock in primary clock modes. The IOFS bit indicates when the internal oscillator block has stabilized and is providing the device clock in RC Clock modes. The T1RUN bit (T1CON<6>) indicates when the Timer1 oscillator is providing the device clock in secondary clock modes. In power-managed modes, only one of these three bits will be set at any time. If none of these bits are set, the INTRC is providing the clock or the internal oscillator block has just started and is not yet stable. The IDLEN bit determines if the device goes into Sleep mode or one of the Idle modes when the SLEEP instruction is executed.

The use of the flag and control bits in the OSCCON register is discussed in more detail in **Section 4.0** "**Power-Managed Modes**".

- Note 1: The Timer1 oscillator must be enabled to select the secondary clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 Control register (T1CON<3>). If the Timer1 oscillator is not enabled, then any attempt to select a secondary clock source will be ignored.
 - 2: It is recommended that the Timer1 oscillator be operating and stable before selecting the secondary clock source or a very long delay may occur while the Timer1 oscillator starts.

3.7.2 OSCILLATOR TRANSITIONS

PIC18F1230/1330 devices contain circuitry to prevent clock "glitches" when switching between clock sources. A short pause in the device clock occurs during the clock switch. The length of this pause is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Clock transitions are discussed in greater detail in **Section 4.1.2 "Entering Power-Managed Modes"**.

6.1.2.4 Stack Full and Underflow Resets

Device Resets on stack overflow and stack underflow conditions are enabled by setting the STVREN bit in Configuration Register 4L. When STVREN is set, a full or underflow will set the appropriate STKFUL or STKUNF bit and then cause a device Reset. When STVREN is cleared, a full or underflow condition will set the appropriate STKFUL or STKUNF bit but not cause a device Reset. The STKFUL or STKUNF bit is cleared by the user software or a Power-on Reset.

6.1.3 FAST REGISTER STACK

A Fast Register Stack is provided for the STATUS, WREG and BSR registers, to provide a "fast return" option for interrupts. The stack for each register is only one level deep and is neither readable nor writable. It is loaded with the current value of the corresponding register when the processor vectors for an interrupt. All interrupt sources will push values into the Stack registers. The values in the registers are then loaded back into their associated registers if the RETFIE, FAST instruction is used to return from the interrupt.

If both low and high-priority interrupts are enabled, the Stack registers cannot be used reliably to return from low-priority interrupts. If a high-priority interrupt occurs while servicing a low-priority interrupt, the Stack register values stored by the low-priority interrupt will be overwritten. In these cases, users must save the key registers in software during a low-priority interrupt.

If interrupt priority is not used, all interrupts may use the Fast Register Stack for returns from interrupt. If no interrupts are used, the Fast Register Stack can be used to restore the STATUS, WREG and BSR registers at the end of a subroutine call. To use the Fast Register Stack for a subroutine call, a CALL label, FAST instruction must be executed to save the STATUS, WREG and BSR registers to the Fast Register Stack. A RETURN, FAST instruction is then executed to restore these registers from the Fast Register Stack.

Example 6-1 shows a source code example that uses the Fast Register Stack during a subroutine call and return.

EXAMPLE 6-1: FAST REGISTER STACK CODE EXAMPLE

CALL	SUB1, FAST •	;STATUS, WREG, BSR ;SAVED IN FAST REGISTER ;STACK
SUB1	• • RETURN, FAST	RESTORE VALUES SAVED
		;IN FAST REGISTER STACK

6.1.4 LOOK-UP TABLES IN PROGRAM MEMORY

There may be programming situations that require the creation of data structures, or look-up tables, in program memory. For PIC18 devices, look-up tables can be implemented in two ways:

- Computed GOTO
- Table Reads

6.1.4.1 Computed GOTO

A computed GOTO is accomplished by adding an offset to the program counter. An example is shown in Example 6-2.

A look-up table can be formed with an ADDWF PCL instruction and a group of RETLW nn instructions. The W register is loaded with an offset into the table before executing a call to that table. The first instruction of the called routine is the ADDWF PCL instruction. The next instruction executed will be one of the RETLW nn instructions that returns the value 'nn' to the calling function.

The offset value (in WREG) specifies the number of bytes that the program counter should advance and should be multiples of 2 (LSb = 0).

In this method, only one data byte may be stored in each instruction location and room on the return address stack is required.

EXAMPLE 6-2: COMPUTED GOTO USING AN OFFSET VALUE

	MOVF	OFFSET,	W
ORG	nn00h	IADUB	
TABLE	ADDWF	PCL	
	RETLW	nnh	
	RETLW	nnh	
	RETLW	nnh	
	•		
	•		

6.1.4.2 Table Reads and Table Writes

A better method of storing data in program memory allows two bytes of data to be stored in each instruction location.

Look-up table data may be stored two bytes per program word by using table reads and writes. The Table Pointer (TBLPTR) register specifies the byte address and the Table Latch (TABLAT) register contains the data that is read from or written to program memory. Data is transferred to or from program memory one byte at a time.

Table read and table write operations are discussed further in Section 7.1 "Table Reads and Table Writes".

NOTES:

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0						
CSRC	TX9	TXEN ⁽¹⁾	SYNC	SENDB	BRGH	TRMT	TX9D						
bit 7							bit (
Legend:													
R = Readabl	e bit	W = Writable	bit	U = Unimplei	mented bit, rea	d as '0'							
-n = Value at	POR	'1' = Bit is set		0' = Bit is cle	eared	x = Bit is unki	nown						
bit 7	CSRC: Clock	Source Select	bit										
	Asvnchronou	is mode:											
	Don't care.												
	Synchronous	<u>s mode:</u>											
	1 = Master m	10de (clock gen ode (clock from	erated interna	ally from BRG)									
bit 6	TX9 · 9-Rit Tr	ansmit Enable I	nit										
Sit 0	1 = Selects 9	1 × 9-Bit Transmit Enable bit 1 = Selects 9-bit transmission											
	0 = Selects 8	B-bit transmissio	n										
bit 5	TXEN: Trans	mit Enable bit ⁽¹)										
	1 = Transmit	enabled											
		disabled											
DIT 4	1 - Sync: EUS	ART Mode Sele	CT DIT										
	0 = Asynchro	onous mode											
bit 3	SENDB: Ser	nd Break Chara	cter bit										
	<u>Asynchronou</u>	<u>is mode:</u>											
	1 = Send Sy	nc Break on nex	t transmissio	on (cleared by h	ardware upon	completion)							
	0 = Sync Bre	eak transmissior	i completed										
	Don't care.	<u>s mode.</u>											
bit 2	BRGH: High	Baud Rate Sel	ect bit										
	Asynchronou	<u>is mode:</u>											
	1 = High spe	ed											
	0 = LOW Spee	eu e mode:											
	Unused in th	is mode.											
bit 1	TRMT: Trans	mit Shift Regist	er Status bit										
	1 = TSR emp	oty											
	0 = TSR full												
bit 0	TX9D: 9th bi	t of Transmit Da	ita										
	Can be addre	ess/data bit or a	parity bit.										

REGISTER 15-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

Note 1: SREN/CREN overrides TXEN in Sync mode.

15.1.3 AUTO-BAUD RATE DETECT

The Enhanced USART module supports the automatic detection and calibration of baud rate. This feature is active only in Asynchronous mode and while the WUE bit is clear.

The automatic baud rate measurement sequence (Figure 15-1) begins whenever a Start bit is received and the ABDEN bit is set. The calculation is self-averaging.

In the Auto-Baud Rate Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. In ABD mode, the internal Baud Rate Generator is used as a counter to time the bit period of the incoming serial byte stream.

Once the ABDEN bit is set, the state machine will clear the BRG and look for a Start bit. The Auto-Baud Rate Detect must receive a byte with the value 55h (ASCII "U", which is also the LIN/J2602 bus Sync character) in order to calculate the proper bit rate. The measurement is taken over both a low and a high bit time in order to minimize any effects caused by asymmetry of the incoming signal. After a Start bit, the SPBRG begins counting up, using the preselected clock source on the first rising edge of RX. After eight bits on the RX pin or the fifth rising edge, an accumulated value totalling the proper BRG period is left in the SPBRGH:SPBRG register pair. Once the 5th edge is seen (this should correspond to the Stop bit), the ABDEN bit is automatically cleared.

If a rollover of the BRG occurs (an overflow from FFFFh to 0000h), the event is trapped by the ABDOVF status bit (BAUDCON<7>). It is set in hardware by BRG rollovers and can be set or cleared by the user in software. ABD mode remains active after rollover events and the ABDEN bit remains set (Figure 15-2).

While calibrating the baud rate period, the BRG registers are clocked at 1/8th the preconfigured clock rate. Note that the BRG clock can be configured by the BRG16 and BRGH bits. The BRG16 bit must be set to use both SPBRG1 and SPBRGH1 as a 16-bit counter. This allows the user to verify that no carry occurred for 8-bit modes by checking for 00h in the SPBRGH register. Refer to Table 15-4 for counter clock rates to the BRG.

While the ABD sequence takes place, the EUSART state machine is held in Idle. The RCIF interrupt is set once the fifth rising edge on RX is detected. The value in the RCREG needs to be read to clear the RCIF interrupt. The contents of RCREG should be discarded.

- Note 1: If the WUE bit is set with the ABDEN bit, Auto-Baud Rate Detection will occur on the byte *following* the Break character.
 - 2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible due to bit error rates. Overall system timing and communication baud rates must be taken into consideration when using the Auto-Baud Rate Detection feature.
 - 3: To maximize baud rate range, it is recommended to set the BRG16 bit if the autobaud feature is used.

TABLE 15-4:BRG COUNTERCLOCK RATES

BRG16	BRGH	BRG Counter Clock
0	0	Fosc/512
0	1	Fosc/128
1	0	Fosc/128
1	1	Fosc/32

15.1.3.1 ABD and EUSART Transmission

Since the BRG clock is reversed during ABD acquisition, the EUSART transmitter cannot be used during ABD. This means that whenever the ABDEN bit is set, TXREG cannot be written to. Users should also ensure that ABDEN does not become set during a transmit sequence. Failing to do this may result in unpredictable EUSART operation.

15.2.4.1 Special Considerations Using Auto-Wake-up

Since auto-wake-up functions by sensing rising edge transitions on RX/DT, information with any state changes before the Stop bit may signal a false End-of-Character and cause data or framing errors. To work properly, therefore, the initial characters in the transmission must be all '0's. This can be 00h (8 bits) for standard RS-232 devices or 000h (12 bits) for LIN/J2602 bus.

Oscillator start-up time must also be considered, especially in applications using oscillators with longer start-up intervals (i.e., XT or HS mode). The Sync Break (or Wake-up Signal) character must be of sufficient length and be followed by a sufficient interval to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

15.2.4.2 Special Considerations Using the WUE Bit

The timing of WUE and RCIF events may cause some confusion when it comes to determining the validity of received data. As noted, setting the WUE bit places the EUSART in an Idle mode. The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared after this when a rising edge is seen on RX/DT. The interrupt condition is then cleared by reading the RCREG register. Ordinarily, the data in RCREG will be dummy data and should be discarded.

The fact that the WUE bit has been cleared (or is still set) and the RCIF flag is set should not be used as an indicator of the integrity of the data in RCREG. Users should consider implementing a parallel method in firmware to verify received data integrity.

To assure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

FIGURE 15-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING NORMAL OPERATION

1. A.	3 - BESSER	n san an an an san Ngangaranang	n an an an an C	с <i>сил</i> 1 1 1 1	100 100 100 1 1	:	 ,					- 2483	
980 SR33	2 2	\$	(;		 ; ; ;	•	;	;; (;	·····		
828 B.Seo	·	1	: 	;	UNIUUUU	Hi.	, [· · · · · · · · · · · · · · · · · · ·	.9771	gaanaadi			
8038		s hjeronomonomo	; ;,	· · ·	,		 ,			5 X	» 		, ;
	1. 2	* * *					;	igered for T	e xi	gest Read	808880908 	50 ····^	-

FIGURE 15-9: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP



NOTES:

The module is enabled by setting the LVDEN bit. Each time that the LVD module is enabled, the circuitry requires some time to stabilize. The IRVST bit is a read-only bit and is used to indicate when the circuit is stable. The module can only generate an interrupt after the circuit is stable and IRVST is set.

19.1 Operation

When the LVD module is enabled, a comparator uses an internally generated reference voltage as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The "trip point" voltage is the voltage level at which the device detects a low-voltage event depending on the configuration of the module. When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the LVDIF bit.

The trip point voltage is software programmable to any 1 of 15 values. The trip point is selected by programming the LVDL3:LVDL0 bits (LVDCON<3:0>).



FIGURE 19-1: LVD MODULE BLOCK DIAGRAM

TABLE 22-2: PICTOFAXAX INSTRUCTION SET (CONTINUED)									
Mnemo	onic,	Description		16-	-Bit Instr	uction W	/ord	Status	Neter
Opera	nds	Description	Cycles	MSb			LSb	Affected	Notes
BIT-ORIEN	TED OP	ERATIONS							
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF	f, b, a	Bit Set f	1	1000	bbba	ffff	ffff	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011	bbba	ffff	ffff	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG	f, d, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1, 2
CONTROL	OPERA	TIONS							•
BC	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	1 (2)	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	n, s	Call subroutine 1st word	2	1110	110s	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	_	Decimal Adjust WREG	1	0000	0000	0000	0111	С	
GOTO	n	Go to address 1st word	2	1110	1111	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
NOP	—	No Operation	1	0000	0000	0000	0000	None	
NOP	—	No Operation	1	1111	XXXX	XXXX	XXXX	None	4
POP	—	Pop Top of Return Stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	—	Push Top of Return Stack (TOS)	1	0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET		Software Device Reset	1	0000	0000	1111	1111	All	
RETFIE	S	Return from Interrupt Enable	2	0000	0000	0001	000s	GIE/GIEH, PEIE/GIEL	
RETLW	k	Return with Literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	s	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP	_	Go into Standby mode	1	0000	0000	0000	0011	TO, PD	

TABLE 22-2: PIC18FXXXX INSTRUCTION SET (CONTINUED)

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTE, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

CLRF	Clear f			CLR	WDT	Clear Wat	chdog Time	er		
Syntax:	CLRF f{,a	a}		Synt	ax:	CLRWDT				
Operands:	$0 \leq f \leq 255$			Oper	ands:	None				
	a ∈ [0,1]		Oper	Operation: $000h \rightarrow WDT$,						
Operation: $000h \rightarrow f,$ $1 \rightarrow Z$				$\begin{array}{l} \text{000h} \rightarrow \text{WDT postscaler,} \\ 1 \rightarrow \overline{\text{TO}}, \end{array}$						
Status Affected: Z		e t 1		$1 \rightarrow PD$						
Encoding:	0110 101a ffff ffff		Statu	is Affected:	TO, PD					
Description:	Clears the o	contents of the	specified	Enco	oding:	0000	0000 00	00 0100		
	register.	register.			cription:	CLRWDT in	CLRWDT instruction resets the			
	If a is 0, ti	he BSR is use	d to select the	ted. the		postscaler of the WDT. Status bits. TO				
	GPR bank. If 'a' is '0' and the extended instruction					and PD, are set.		,		
			Word	ls:	1					
	in Indexed I	ed, this instruct iteral Offset A	ddressing	Cycle	es:	1				
	mode whenever $f \le 95$ (5Fh). See Section 22.2.3 "Byte-Oriented and			QC	vcle Activity:					
					Q1	Q2	Q3	Q4		
	Literal Offs	Bit-Oriented Instructions in Indexed			Decode	No	Process	No		
Words:	1					operation	Data	operation		
Cycles:	1			_						
				Exar	<u>nple:</u>	CLRWDT				
	02	03	04		Before Instruc	tion –	2			
Decode	Read	Process	Write		After Instructio	on =	?			
200000	register 'f'	Data	register 'f'		WDT Co	unter =	00h			
						stscaler =	0			
Example:	CLRF	FLAG_REG,	1			=	1			
Before Instruc	tion				. 2		·			
FLAG_R	EG = 5A	h								
After Instruction	on FG = 001	h								

NEGF	Negate f					
Syntax:	NEGF f {,a}					
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]					
Operation:	$(\overline{f}) + 1 \rightarrow f$					
Status Affected:	N, OV, C, DC, Z					
Encoding:	0110 110a ffff ffff					
Description.	complement. The result is placed using two s complement. The result is placed in the data memory location 'f'. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 22.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.					
Words:	1					
Cycles:	1					

NOF)	No Operation							
Synta	ax:	NOP							
Oper	ands:	None							
Oper	ation:	No operati	on						
Statu	s Affected:	None							
Encoding:		0000	0000	000	0	0000			
		1111	xxxx	XXX	x	xxxx			
Desc	ription:	No operati	No operation.						
Word	ls:	1							
Cycle	es:	1							
QC	ycle Activity:								
	Q1	Q2	Q	3		Q4			
	Decode	No	No)		No			
		operation	opera	tion	0	peration			

Example:

None.

Q Cycle Activity:

_	Q1	Q2	Q3	Q4
	Decode	Read	Process	Write
		register 'f'	Data	register 'f'

Example: NEGF REG, 1

> Before Instruction REG = 0011 1010 [3Ah] After Instruction REG = 1100 0110 [C6h]

MOVSS	Move Inc	Move Indexed to Indexed						
Syntax:	MOVSS	[z _s], [z _d]						
Operands:	$0 \le z_s \le 12$ $0 \le z_d \le 12$	$\begin{array}{l} 0 \leq z_s \leq 127 \\ 0 \leq z_d \leq 127 \end{array}$						
Operation:	((FSR2) +	$z_s) \rightarrow ((F$	SR2) + z _d)				
Status Affected:	None	None						
Encoding: 1st word (source) 2nd word (dest.)	1110 1011 1zzz zzz 1111 xxxx xzzz zzz							
Description	The conter moved to the addresses registers a 7-bit literal respective registers of the 4096-b (000h to F The MOVS: PCL, TOS destination If the result an indirect value retur resultant d an indirect	1111xxxxxzzzzzzz_dThe contents of the source register are moved to the destination register. The addresses of the source and destination registers are determined by adding the 7-bit literal offsets 'zs' or 'zd', respectively, to the value of FSR2. Both registers can be located anywhere in the 4096-byte data memory space (000h to FFFh).The MOVSS instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register.If the resultant source address points to an indirect addressing register, the value returned will be 00h. If the resultant destination address points to an indirect addressing register, the						
vvoras:	2							
Cycles:	2							
Q Cycle Activity:								
Q1	Q2	Q	3	Q4				

Q1	Q2	Q3	Q4	
Decode	Determine	Determine	Read	
	source addr	source addr	source reg	
Decode	Determine dest addr	Determine dest addr	Write to dest reg	

Example:	MOVSS	[05h],	[06h]
Before Instruction	on		
FSR2	=	80h	
Contents of 85h Contents	=	33h	
of 86h	=	11h	
After Instruction			
FSR2	=	80h	
Contents of 85h Contents	=	33h	
of 86h	=	33h	

PUSHL	s	tore Liter	al at l	FSR	2, Decr	em	ent FSR2
Syntax:	Р	USHL k					
Operands:	0	$\leq k \leq 255$					
Operation:	k F	→ (FSR2) SR2 – 1 –), → FSR:	2			
Status Affect	ted: N	one					
Encoding:		1110	101	0	kkkk		kkkk
	m is T O	nemory ad decrement his instruct nto a softwork	dress anted by tion all vare st	spec / 1 a lows ack.	tified by l after the o susers to	FSI ope o pu	R2. FSR2 eration. Ish values
Words:	1						
Cycles:	1						
Q Cycle Ad	ctivity:						
	Q1	Q2			Q3		Q4
Dee	code	Read '	K'	Pro d	ocess ata	de	Write to estination
<u>Example:</u> Before F N	Instruc SR2H:F lemory	PUSHL tion SR2L (01ECh)	08h	=	01ECh 00h		

After Instruction		
FSR2H:FSR2L Memory (01ECh)	=	01EBh 08h

22.2.3 BYTE-ORIENTED AND BIT-ORIENTED INSTRUCTIONS IN INDEXED LITERAL OFFSET MODE

Note:	Enabling	the	PIC18	3 inst	instruction		
	extension	may	cause I	legacy	applicat	tions	
	to behave	errat	ically or	tirely.			

In addition to eight new commands in the extended set, enabling the extended instruction set also enables Indexed Literal Offset Addressing mode (**Section 6.5.1 "Indexed Addressing with Literal Offset**"). This has a significant impact on the way that many commands of the standard PIC18 instruction set are interpreted.

When the extended set is disabled, addresses embedded in opcodes are treated as literal memory locations: either as a location in the Access Bank ('a' = 0) or in a GPR bank designated by the BSR ('a' = 1). When the extended instruction set is enabled and 'a' = 0, however, a file register argument of 5Fh or less is interpreted as an offset from the pointer value in FSR2 and not as a literal address. For practical purposes, this means that all instructions that use the Access RAM bit as an argument – that is, all byte-oriented and bitoriented instructions, or almost half of the core PIC18 instructions – may behave differently when the extended instruction set is enabled.

When the content of FSR2 is 00h, the boundaries of the Access RAM are essentially remapped to their original values. This may be useful in creating backward compatible code. If this technique is used, it may be necessary to save the value of FSR2 and restore it when moving back and forth between C and assembly routines in order to preserve the Stack Pointer. Users must also keep in mind the syntax requirements of the extended instruction set (see Section 22.2.3.1 "Extended Instruction Syntax with Standard PIC18 Commands").

Although the Indexed Literal Offset Addressing mode can be very useful for dynamic stack and pointer manipulation, it can also be very annoying if a simple arithmetic operation is carried out on the wrong register. Users who are accustomed to the PIC18 programming must keep in mind that, when the extended instruction set is enabled, register addresses of 5Fh or less are used for Indexed Literal Offset Addressing mode.

Representative examples of typical byte-oriented and bit-oriented instructions in the Indexed Literal Offset Addressing mode are provided on the following page to show how execution is affected. The operand conditions shown in the examples are applicable to all instructions of these types.

22.2.3.1 Extended Instruction Syntax with Standard PIC18 Commands

When the extended instruction set is enabled, the file register argument, 'f', in the standard byte-oriented and bit-oriented commands is replaced with the literal offset value, 'k'. As already noted, this occurs only when 'f' is less than or equal to 5Fh. When an offset value is used, it must be indicated by square brackets ("[]"). As with the extended instructions, the use of brackets indicates to the compiler that the value is to be interpreted as an index or an offset. Omitting the brackets, or using a value greater than 5Fh within brackets, will generate an error in the MPASM Assembler.

If the index argument is properly bracketed for Indexed Literal Offset Addressing mode, the Access RAM argument is never specified; it will automatically be assumed to be '0'. This is in contrast to standard operation (extended instruction set disabled) when 'a' is set on the basis of the target address. Declaring the Access RAM bit in this mode will also generate an error in the MPASM Assembler.

The destination argument, 'd', functions as before.

In the latest versions of the MPASM Assembler, language support for the extended instruction set must be explicitly invoked. This is done with either the command line option, $/_{Y}$, or the PE directive in the source listing.

22.2.4 CONSIDERATIONS WHEN ENABLING THE EXTENDED INSTRUCTION SET

It is important to note that the extensions to the instruction set may not be beneficial to all users. In particular, users who are not writing code that uses a software stack may not benefit from using the extensions to the instruction set.

Additionally, the Indexed Literal Offset Addressing mode may create issues with legacy applications written to the PIC18 assembler. This is because instructions in the legacy code may attempt to address registers in the Access Bank below 5Fh. Since these addresses are interpreted as literal offsets to FSR2 when the instruction set extension is enabled, the application may read or write to the wrong data addresses.

When porting an application to the PIC18F1230/1330, it is very important to consider the type of code. A large, re-entrant application that is written in 'C' and would benefit from efficient compilation will do well when using the instruction set extensions. Legacy applications that heavily use the Access Bank will most likely not benefit from using the extended instruction set.

23.2 DC Characteristics: Power-Down and Supply Current PIC18F1230/1330 (Industrial) PIC18LF1230/1330 (Industrial) (Continued)

PIC18LF1230/1330 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial						
PIC18F12 (Indus	30/1330 trial, Extended)	Standa Operat	i rd Ope ing tem	perating (Conditions (unle -40°C ≤ TA -40°C ≤ TA	ss otherwise sta $\leq +85^{\circ}$ C for indus $\leq +125^{\circ}$ C for exte	ted) strial ended	
Param No.	Device	Тур	Max	Units	Conditions			
	Supply Current (IDD) ⁽²⁾							
	PIC18LF1230/1330	0.8	1.83	mA	-40°C			
		0.8	1.83	mA	+25°C	VDD = 2.0V		
		0.8	1.83	mA	+85°C			
	PIC18LF1230/1330	1.3	2.93	mA	-40°C			
		1.3	2.93	mA	+25°C	VDD = 3.0V	FOSC = 4 MHz (RC RUN mode	
		1.3	2.93	mA	+85°C		INTOSC source)	
	All devices	2.5	4.73	mA	-40°C		,	
		2.5	4.73	mA	+25°C	VDD = 5 0V		
		2.5	4.73	mA	+85°C	100 0.01		
	Extended devices only	2.5	10.0	mA	+125°C			
	PIC18LF1230/1330	2.9	7.6	μΑ	-40°C			
		3.1	7.6	μΑ	+25°C	VDD = 2.0V		
		3.6	10.6	μA	+85°C			
	PIC18LF1230/1330	4.5	10.6	μΑ	-40°C			
		4.8	10.6	μA	+25°C	VDD = 3.0V	(RC IDLE mode.	
		5.8	14.6	μΑ	+85°C		INTRC source)	
	All devices	9.2	15.6	μΑ	-40°C			
		9.8	15.6	μΑ	+25°C	VDD = 5.0V		
		11.4	35.6	μΑ	+85°C			
	Extended devices only	21	179	μA	+125°C			

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;

MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power Timer1 oscillator selected.

4: BOR and LVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.





FIGURE 23-9: BROWN-OUT RESET TIMING



TABLE 23-10:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER
AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Тур	Мах	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	_		μS	
31	Twdt	Watchdog Timer Time-out Period (no postscaler)	3.4	4.0	4.6	ms	
32	Tost	Oscillation Start-up Timer Period	1024 Tosc	_	1024 Tosc	_	Tosc = OSC1 period
33	TPWRT	Power-up Timer Period	55.6	65.5	75	ms	
34	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μS	
35	TBOR	Brown-out Reset Pulse Width	200	_	—	μS	$VDD \le BVDD$ (see D005)
36	TIRVST	Time for Internal Reference Voltage to become Stable	—	20	50	μS	
37	Tlvd	Low-Voltage Detect Pulse Width	200	_	—	μS	$V D D \leq V L V D$
38	TCSD	CPU Start-up Time	—	10	—	μS	
39	TIOBST	Time for INTOSC to Stabilize	_	1	_	μS	

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Param No.	Symbol	Characteristic		Min	Мах	Units	Conditions
130	Tad	A/D Clock Period	PIC18FXXXX	0.7	25.0 ⁽¹⁾	μS	Tosc based, VREF $\geq 3.0V$
			PIC18LFXXXX	1.4	25.0 ⁽¹⁾	μS	VDD = 2.0V, Tosc based, VREF full range
			PIC18FXXXX	_	1	μS	A/D RC mode
			PIC18 LF XXXX		3	μS	VDD = 2.0V, A/D RC mode
131	TCNV	Conversion Time (not including acquisition time) ⁽²⁾		11	12	Tad	
132	TACQ	Acquisition Time ⁽³⁾		1.4	_	μS	-40°C to +85°C
135	Tswc	Switching Time from Convert \rightarrow Sample		_	(Note 4)		
136	TDIS	Discharge Time		0.2	—	μS	

Note 1: The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

2: ADRES register may be read on the following TCY cycle.

3: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to Vss or Vss to VDD). The source impedance (Rs) on the input channels is 50Ω.

4: On the following cycle of the device clock.

NOTES:

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	N	S	
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	С		9.40	
Contact Pad Width	Х			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A