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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA
Supplier Device Package	169-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5aii6p

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- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited:
  – In single bank mode, two areas can be selected with 128-bit granularity.
  – In dual bank mode, one area per bank can be selected with 64-bit granularity.

  An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

3.5 Embedded SRAM

The STM32L4R5xx, STM32L4R7xx and STM32L4R9xx devices feature 640 Kbytes of embedded SRAM. This SRAM is split into three blocks:

- 192 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x1000 0000 with hardware parity check (SRAM2). This memory is also mapped at address 0x2003 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the ICode/DCode buses for maximum performance.
  These 64 Kbytes SRAM can also be retained in Standby mode.
  The SRAM2 can be write-protected with 1 Kbyte granularity.
- 384 Kbytes mapped at address 0x2004 0000 - (SRAM3).

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.12 Clocks and startup

The clock controller (see *Figure 7*) distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock. The HSE must be available when the DSI-HOST peripheral is used.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 120 MHz.
- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG, the two SAIs, LCD-TFT and DSI-HOST. When using DSI-HOST peripheral, the high-speed external crystal (HSE) must be available.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.21 Voltage reference buffer (VREFBUF)

The STM32L4Rxxx devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

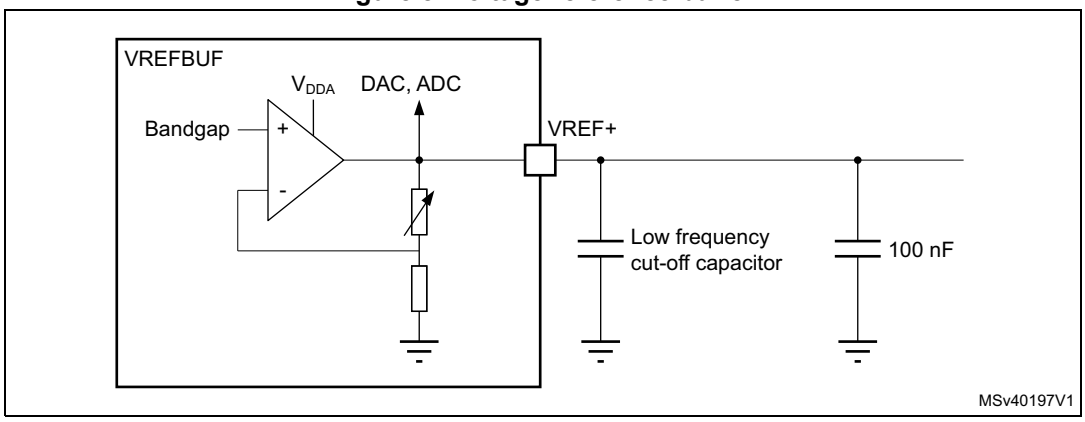
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 8. Voltage reference buffer



3.22 Comparators (COMP)

The STM32L4Rxxx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

The DSI Host main features are:

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video Mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for end of transmission packet (EoTp)
- Fault recovery schemes
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for generic and DCS commands
  - Video Mode interface through LTDC
  - Adapted command mode interface through LTDC
- Independently programmable virtual channel ID in
  - Video mode
  - Adapted command mode
  - APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2 and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps

Adapted interface features:

- Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2 and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 7: Clock tree*
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 11. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop 0, Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
3	B1	B1	3	3	C12	D1	D1	3	3	D3	C12	C12	D1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, SAI1_D2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4, LCD_B0, FMC_A20, SAI1_FS_A, EVENTOUT	-
4	C2	C2	4	4	D9	E4	E4	4	4	C2	D9	D9	E4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, SAI1_CK2, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6, LCD_G0, FMC_A21, SAI1_SCK_A, EVENTOUT	-
5	D2	D2	5	5	D10	E3	E3	5	5	D4	D10	D10	E3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_D1, DCMI_D7, LCD_G1, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3,WKUP3
6	E2	E2	6	6	E10	E2	E2	6	6	B1	E10	E10	E2	VBAT	S	-	-	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
7	C1	C1	7	7	D11	E1	E1	7	7	E4	D11	D11	E1	PC13	I/O	FT	- (1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/RTC_OUT,WKUP2
8	D1	D1	8	8	E11	F1	F1	8	8	D1	E11	E11	F1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
9	E1	E1	9	9	E12	G1	G1	9	9	D2	E12	E12	G1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	D6	D6	10	10	E9	F5	F5	-	10	E3	E9	E9	F5	PF0	I/O	FT_f	-	I2C2_SDA, OCTOSPIM_P2_IO0, FMC_A0, EVENTOUT	-
-	D5	D5	11	11	F8	F4	F4	-	11	E2	F8	F8	F4	PF1	I/O	FT_f	-	I2C2_SCL, OCTOSPIM_P2_IO1, FMC_A1, EVENTOUT	-
-	D4	D4	12	12	F12	F3	F3	-	12	E1	F12	F12	F3	PF2	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_IO2, FMC_A2, EVENTOUT	-
-	E4	E4	13	13	F11	G3	G3	-	13	E5	F11	F11	G3	PF3	I/O	FT	-	OCTOSPIM_P2_IO3, FMC_A3, EVENTOUT	-

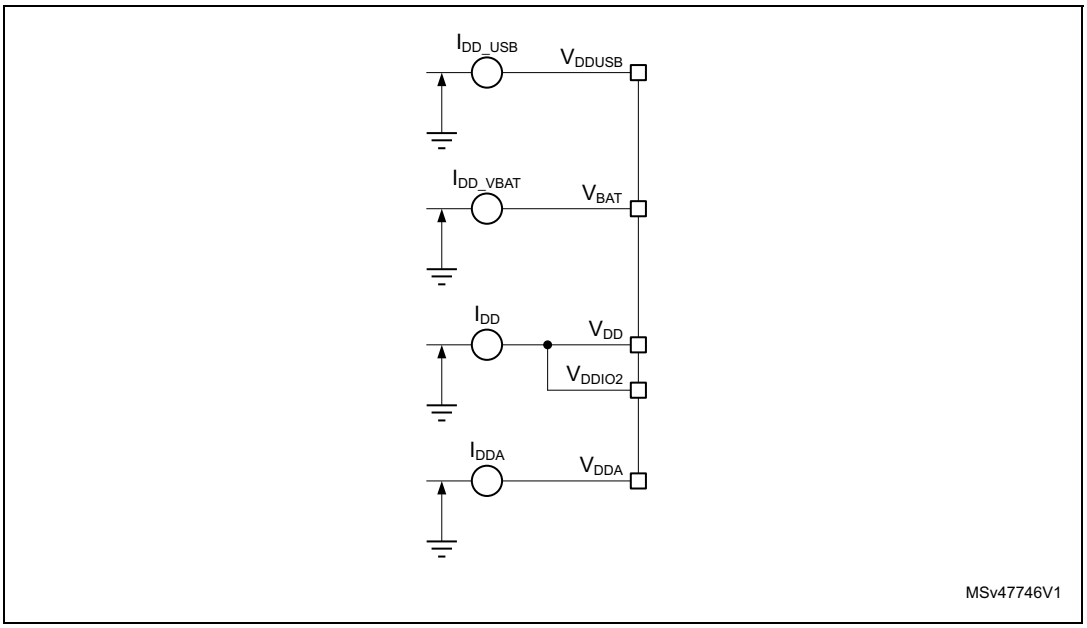
Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00- 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

6.1.7 Current consumption measurement

Figure 27. Current consumption measurement



The I_{DD_ALL} parameters given in *Table 26* to *Table 40* represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, V_{DDUSB} and V_{BAT}.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics* and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

6.3.4 Embedded voltage reference

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.60	3.95	5.05	6.65	9.55	4.2	5.0	7.1	11.0	17.0	mA
				16 MHz	2.30	2.65	3.75	5.35	8.20	2.7	3.6	5.6	8.9	15.0	
				8 MHz	1.30	1.65	2.70	4.30	7.15	1.6	2.4	4.4	7.7	14.0	
				4 MHz	0.770	1.10	2.20	3.75	6.60	1.0	1.8	3.8	7.1	14.0	
				2 MHz	0.515	0.865	1.95	3.50	6.35	0.7	1.5	3.5	6.8	13.0	
				1 MHz	0.380	0.735	1.80	3.35	6.20	0.6	1.4	3.4	6.7	13.0	
				100 KHz	0.265	0.620	1.70	3.25	6.10	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	17.0	18.0	19.5	21.5	25.5	19.0	21.0	24.0	28.0	36.0	
			Range 1 Normal Mode	80 MHz	12.5	13.0	14.0	16.0	19.5	14.0	15.0	18.0	22.0	29.0	
				72 MHz	11.0	11.5	13.0	15.0	18.5	13.0	14.0	17.0	21.0	28.0	
				64 MHz	9.90	10.5	12.0	14.0	17.5	12.0	13.0	15.0	19.0	26.0	
				48 MHz	7.85	8.30	9.75	11.5	15.0	8.7	9.9	13.0	17.0	24.0	
				32 MHz	5.35	5.80	7.20	9.20	12.5	6.1	7.1	9.6	14.0	21.0	
				24 MHz	4.10	4.55	5.95	7.90	11.5	4.7	5.7	8.2	13.0	20.0	
				16 MHz	2.80	3.30	4.65	6.60	10.0	3.3	4.3	6.8	11.0	18.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	460	905	2150	3950	7100	660	1700	4100	7700	15000	µA
				1 MHz	355	760	2000	3800	6950	540	1500	3900	7600	14000	
				400 KHz	240	685	1950	3700	6850	410	1400	3800	7500	14000	
				100 KHz	200	635	1900	3650	6800	370	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 32. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	4.10	4.50	5.60	7.20	10.00	4.7	5.6	7.6	11.0	17.0	mA
				16 MHz	2.75	3.10	4.25	5.85	8.70	3.2	4.1	6.1	9.4	16.0	
				8 MHz	1.25	1.90	2.95	4.55	7.35	1.7	2.7	4.7	8.0	14.0	
				4 MHz	0.91	1.25	2.35	3.90	6.75	1.2	2.0	4.0	7.3	14.0	
				2 MHz	0.59	0.94	2.00	3.60	6.40	0.8	1.6	3.6	6.9	13.0	
				1 MHz	0.42	0.77	1.85	3.40	6.25	0.6	1.4	3.4	6.7	13.0	
				100 KHz	0.27	0.63	1.70	3.25	6.10	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	17.00	18.00	19.50	21.50	25.50	19.0	21.0	24.0	28.0	36.0	
			Range 1 Normal Mode	80 MHz	13.00	13.50	15.00	17.00	20.50	15.0	16.0	19.0	23.0	30.0	
				72 MHz	11.50	12.00	14.00	16.00	19.50	13.0	15.0	18.0	22.0	29.0	
				64 MHz	10.50	11.00	12.50	14.50	18.00	12.0	13.0	16.0	20.0	27.0	
				48 MHz	9.00	9.50	11.00	13.00	16.50	11.0	12.0	15.0	19.0	26.0	
				32 MHz	6.45	6.95	8.40	10.50	14.00	7.3	8.5	12.0	16.0	23.0	
				24 MHz	4.90	5.40	6.85	8.80	12.50	5.6	6.7	9.3	14.0	21.0	
				16 MHz	3.55	4.00	5.40	7.40	11.00	4.1	5.2	7.7	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	590	1000	2300	4050	7200	800.0	1800	4200	7800	15000	µA
				1 MHz	390	805	2100	3850	7000	580.0	1600	4000	7600	14000	
				400 KHz	245	655	1950	3750	6900	420.0	1400	3800	7500	14000	
				100 KHz	195	610	1900	3700	6850	370.0	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

High-speed internal 48 MHz (HSI48) RC oscillator

Table 62. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Table 97. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	8.33	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 120 MHz	0	60	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	0.00833	546.13	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	-	35.77	s

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 98. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 99. WWDG min/max timeout value at 120 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0341	2.1845	ms
2	1	0.0683	4.3691	
4	2	0.1356	8.7381	
8	3	0.2731	17.4763	

6.3.30 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0351 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.17: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 100* below for the analog filter characteristics:

Table 100. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 116. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 57. Synchronous non-multiplexed PSRAM write timings

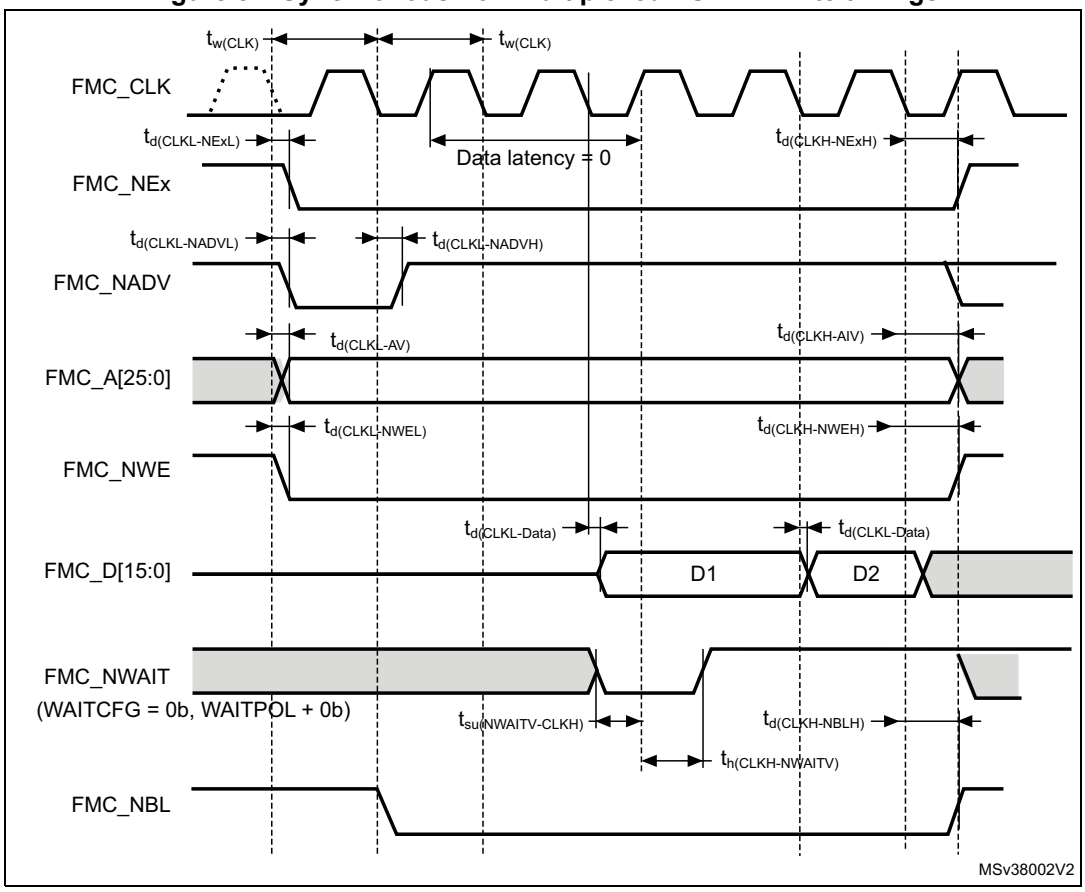


Figure 61. NAND controller waveforms for common memory write access

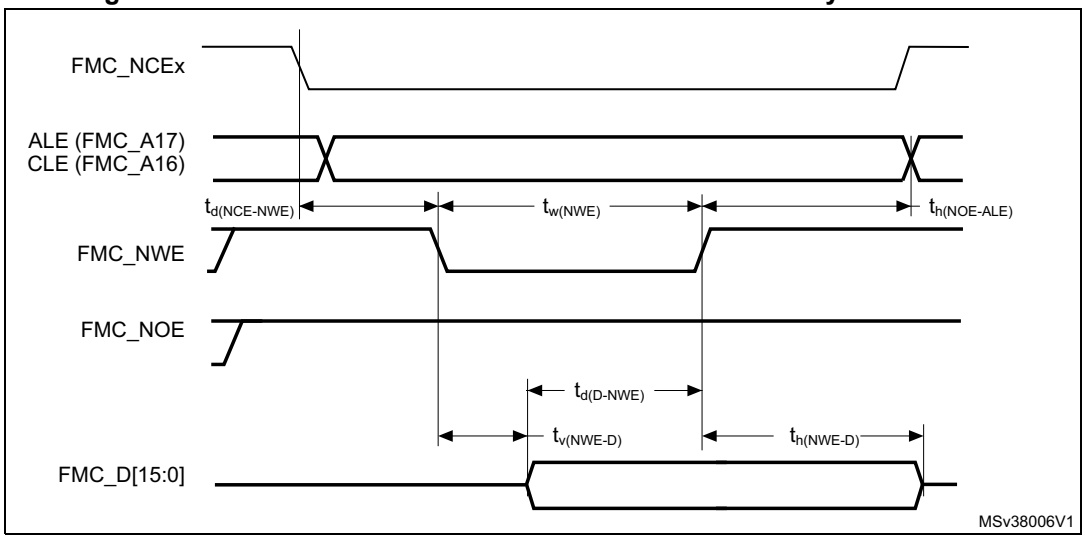


Table 118. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	14	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 119. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$2T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$-1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.32 OctoSPI characteristics

Unless otherwise specified, the parameters given in *Table 120*, *Table 121* and *Table 122* for OctoSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency

6.3.33 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 123* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 21*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Figure 68. DCMI timing diagram

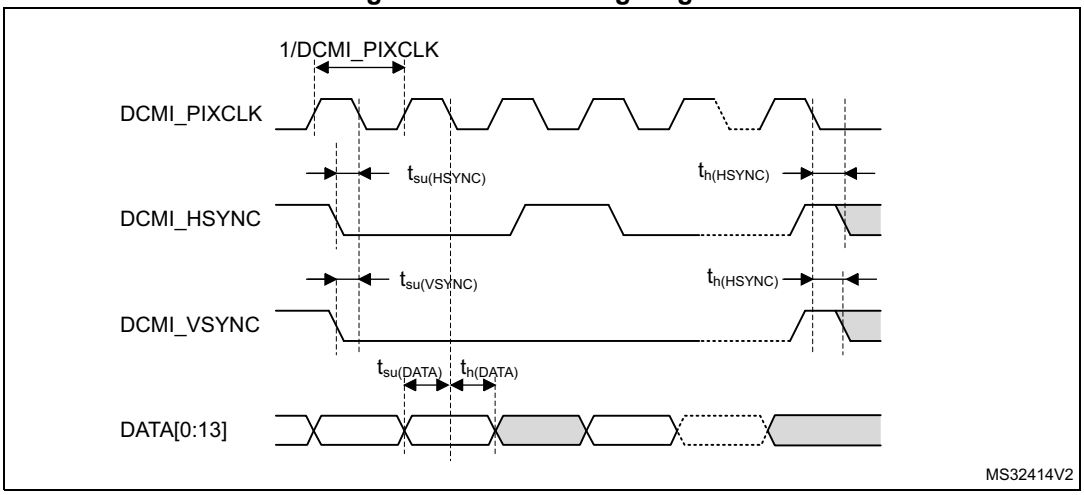


Table 123. DCMI characteristics(1)

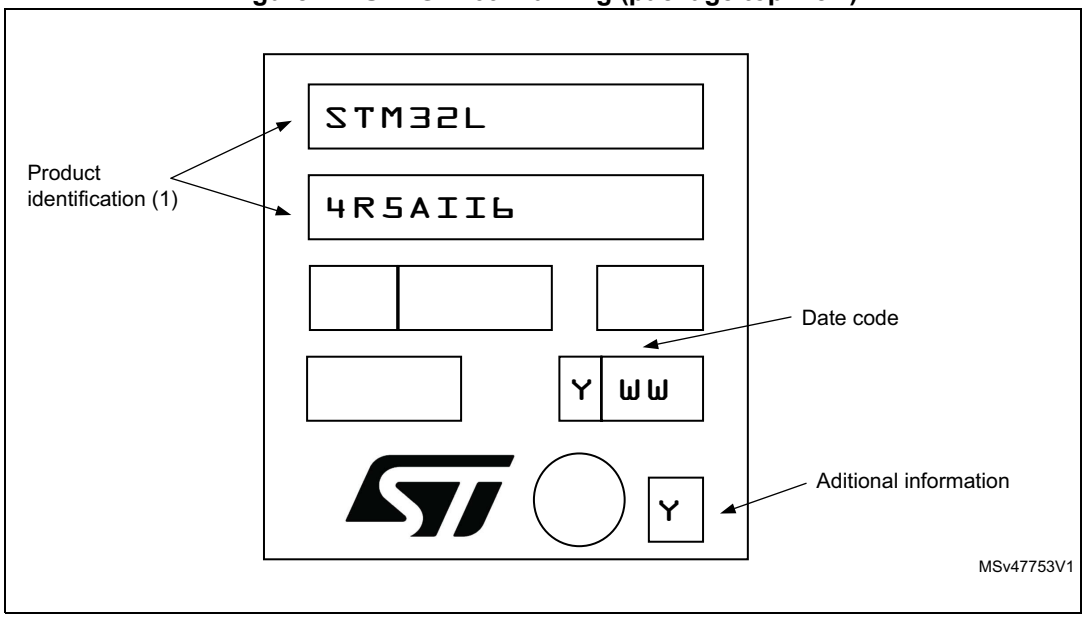
Symbol	Parameter	Condition	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	1.71 < VDD < 3.6 Voltage range V1	-	48	MHz
		1.71 < VDD < 3.6 Voltage range V2	-	10	
D_{pixel}	Pixel clock input duty cycle	-	30	70	%

UFBGA169 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 74. UFBGA169 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.