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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	110
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5qgi6

Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.30.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.30.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

4 Pinouts and pin description

Figure 9. STM32L4R5xx and STM32L4R7xx UFBGA169 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv38036V4

1. The above figure shows the package top view.

Figure 10. STM32L4R9xx UFBGA169 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PH9	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PA10	VDDUSB	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PA8	PA9	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PC8	PG8	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG13	PG4	PG3	PG5	PG7	PC7	PG6	PC9
H	PH0-OSC_IN	VSS	NRST	PF10	PG1	PE10	PB11	PD13	PG2	PD15	PD14	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PG0	PE9	PE15	PD12	PD11	PD10	DSI_D1P	DSI_D1N	VSSDSI
K	PC3	VSSA/VREF-	PA0	PC4	PF15	PE8	PE14	PH4	PD9	PD8	DSI_CKP	DSI_CKN	VSSDSI
L	VREF+	VDDA	PA5	PA6	PB1	PF14	PE7	PE13	PH5	PB15	DSI_D0P	DSI_D0N	VCAPDSI
M	PA1	PA3	VSS	PA7	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB14	VDDDSI
N	PA2	PA4	VDD	PB0	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv45223V2

1. The above figure shows the package top view.

Figure 15. STM32L4R9xx UFBGA144 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PE0	PB9	PH3-BOOT0	PB4	VDDIO2	VSS	PD3	PC11	PA14	VDD	VSS
B	VBAT	VDD	PE3	PB8	PB5	PB3	PD6	PD1	PA15	PA13	PA12	PA11
C	VSS	PE5	PE2	PE1	PB7	PG13	PD4	PD0	PC10	PA10	VDDUSB	PC9
D	PC14-OSC32_IN	PC15-OSC32_OUT	PE4	PE6	PB6	PG12	PD5	PD2	PC12	PA9	PA8	PC6
E	PF2	PF1	PF0	PC13	PF3	PG10	PD7	PG8	PC7	PC8	PG7	VDDIO2
F	PF8	PF6	PF4	PF5	PF7	PG9	PG3	PG5	PG6	PG4	VSS	PG2
G	VDD	VSS	PF10	PF9	PF12	PE7	PD15	PD14	PD12	PD13	PD11	VDD
H	PH0-OSC_IN	PH1-OSC_OUT	PC0	PC2	PB2	PF15	PE11	PD10	PD9	PD8	DSI_D1P	DSI_D1N
J	NRST	PC1	PC3	PA6	PB1	PF13	PE9	PE13	PB15	VSSDSI	DSI_CKP	DSI_CKN
K	VSSA/VREF-	VREF+	PA0	PA4	PC5	PF11	PE8	PE15	PB11	PB14	DSI_D0P	DSI_D0N
L	VDDA	PA1	PA2	PA5	PC4	VSS	PG0	PE10	PB10	PB12	VDD	VCAPDSI
M	VSS	VDD	PA3	PA7	PB0	VDD	PF14	PG1	PE12	PE14	PB13	VSS

MSv38491V4

1. The above figure shows the package top view.

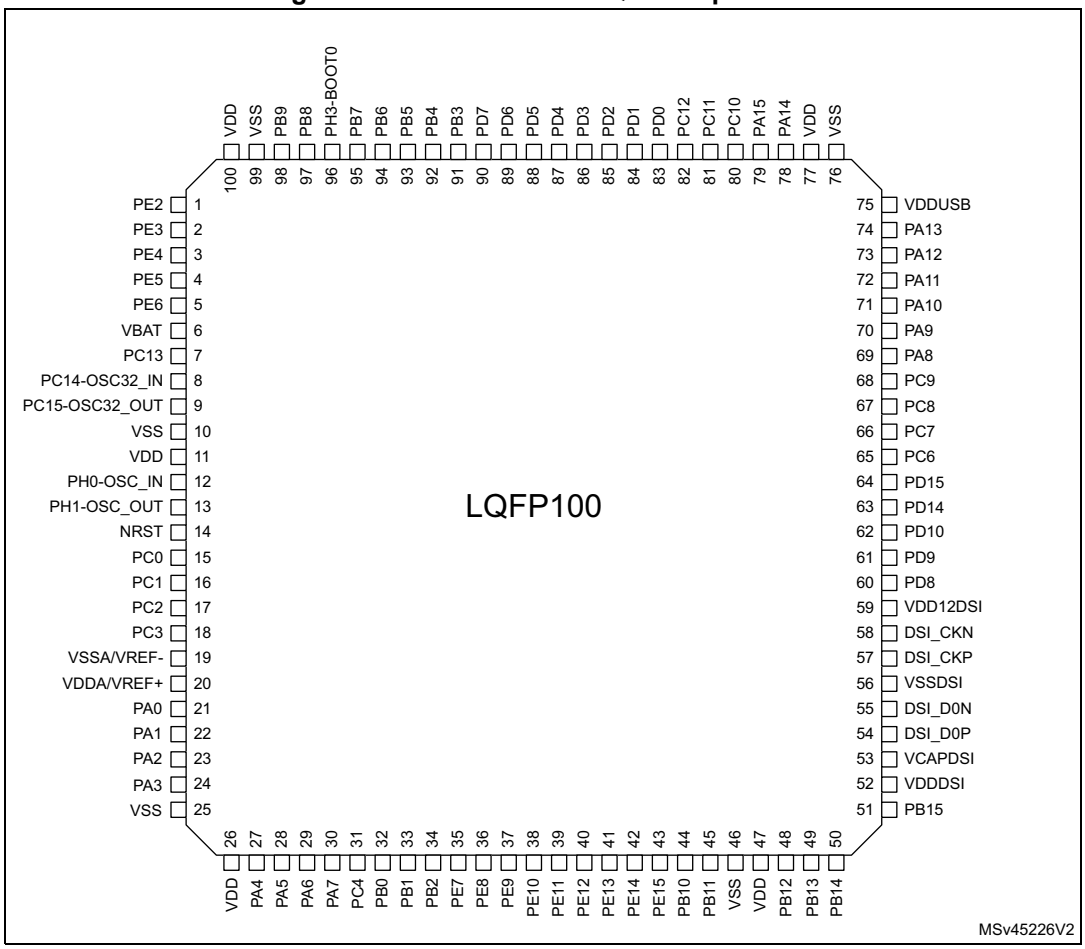
Figure 16. STM32L4R9xx WLCSP144 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PA14	PA15	PD0	PD5	VDD	PG12	VDDIO2	PB7	PE0	PE1	VSS
B	VDD	VDDUSB	PA13	PC12	PD2	VSS	PG10	PB3	PH3-BOOT0	PB9	PE2	VDD
C	PA11	PA12	PC10	PC11	PD1	PD4	PG9	PB4	PB6	PB8	PE3	PE4
D	PC8	PC9	PA8	PA9	PA10	PD3	PD7	PG13	PE5	PE6	PC13	VSS
E	PG7	PG8	VDDIO2	PC6	PG6	PC7	PD6	PB5	PF0	VBAT	PC14-OSC32_IN	PC15-OSC32_OUT
F	PD15	PG2	PD14	PD12	PG3	PG4	PG5	PF1	PF5	PF4	PF3	PF2
G	VSS	VDD	PD13	PD11	PD10	PE9	PF14	PA5	PF7	PF6	VSS	VDD
H	PD9	PD8	PB14	PB13	PE14	PE8	PB1	PA2	PC2	PF10	NRST	PH0-OSC_IN
J	DSI_D1N	DSI_D1P	PB15	PB12	PE13	PF15	PB2	PA6	PA0	PC3	PC0	PH1-OSC_OUT
K	DSI_CKP	DSI_CKN	VSSDSI	PE15	PE10	PG0	PF11	PC5	PA4	PA1	VSSA/VREF-	PC1
L	DSI_D0P	DSI_D0N	VCAPDSI	PB10	PE11	PG1	VDD	PF12	PC4	PA3	VREF+	VDDA
M	VDD	VDD	VSS	PB11	PE12	PE7	PF13	VSS	PB0	PA7	VDD	VSS

MSv42219V2

1. The above figure shows the package top view

Figure 22. STM32L4R9xx LQFP100 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	M4	M4	-	-	-	N4	N4	-	-	-	-	-	-	OPAMP2_VINM	I	TT	-	-	-
32	J5	J5	43	43	M10	L4	L4	30	40	M4	M10	M10	M4	PA7	I/O	FT_fla	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, OCTOSPIM_P1_IO2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC1_IN12
33	K5	K5	44	44	L9	H5	H5	31	41	L5	L9	L9	K4	PC4	I/O	FT_a	-	USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT	COMP1_INM, ADC1_IN13
34	L5	L5	45	45	K8	J5	J5	-	-	K5	K8	K8	-	PC5	I/O	FT_a	-	SAI1_D3, USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
35	M5	M5	46	46	M9	K5	K5	32	42	M5	M9	M9	N4	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC1_IN15

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
54	K10	K10	76	76	J3	M12	M12	51	72	J9	J3	J3	L10	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	M2	L12	L12	-	-	-	M2	M2	-	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	52	73	-	-	-	M13	VDDDSI	S	-	-	-	-
-	-	-	-	-	-	L13	L13	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	53	74	L12	L3	L3	L13	VCAPDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	54	75	K11	L1	L1	L11	DSI_D0P	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	55	76	K12	L2	L2	L12	DSI_D0N	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	56	77	-	-	-	J13	VSSDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	57	78	J11	K1	K1	K11	DSI_CKP	I/O	-	(3)	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
86	A6	A6	119	119	A5	D7	D7	88	121	D7	A5	A5	D7	PD5	I/O	FT	-	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	-	120	120	B6	M3	M3	-	122	-	B6	B6	M3	VSS	S	-	-	-	-
-	-	-	121	121	A6	A8	A8	-	123	-	A6	A6	A8	VDD	S	-	-	-	-
87	B6	B6	122	122	E7	E7	E7	89	124	B7	E7	E7	E7	PD6	I/O	FT	-	SAI1_D1, DCMI_D10, SPI3_MOSI, DFSDM1_DATIN1, USART2_RX, OCTOSPIM_P1_IO6, LCD_DE, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
88	A5	A5	123	123	D7	F7	F7	90	125	E7	D7	D7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, OCTOSPIM_P1_IO7, FMC_NCE/FMC_NE1, EVENTOUT	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	OCTOSPIM_P2_IO0	-	-
	PF1	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_IO1	-	-
	PF2	-	-	-	-	I2C2_SMBA	OCTOSPIM_P2_IO2	-	-
	PF3	-	-	-	-	-	OCTOSPIM_P2_IO3	-	-
	PF4	-	-	-	-	-	OCTOSPIM_P2_CLK	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	OCTOSPIM_P1_CLK	-	-	DFSDM1_CKOUT	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	OCTOSPIM_P2_DQS	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM1_DATIN6	-
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port B	PB0	-	-	OCTOSPIM_P1_IO1	-	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_ RTS_DE	-	OCTOSPIM_P1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	OCTOSPIM_P1_DQS	LCD_B1	-	-	-	EVENTOUT
	PB3	-	-	OTG_FS_CRS_SYNC	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_ DE	TSC_G2_IO1	DCMI_D12	-	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	DCMI_D10	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	DCMI_D5	-	TIM8_BKIN2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	DCMI_VSYNC	DSI_TE	FMC_NL	TIM8_BKIN	TIM17_CH1N	EVENTOUT
	PB8	SDMMC1_ CKIN	CAN1_RX	DCMI_D6	LCD_B1	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	SDMMC1_ CDIR	CAN1_TX	DCMI_D7	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPIM_P1_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	OCTOSPIM_P1_NCS	DSI_TE	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RT S_DE	TSC_G1_IO1	-	-	-	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CT S	TSC_G1_IO2	-	-	-	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	-	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	-	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses(1)

Bus	Boundary address	Size (bytes)	Peripheral
-	0xA000 1800 - 0xDFFF FFFF	1 KB	Reserved
	0xA000 1400 - 0xA000 17FF	1 KB	OCTOSPI2 registers
	0xA000 1000 - 0xA000 13FF	1 KB	OCTOSPI1 registers
	0xA000 0400 - 0xA000 0FFF	1 KB	Reserved
	0xA000 0000 - 0xA000 03FF	1 KB	FSMC registers
AHB2	0x5006 2000 - 0x5FFF FFFF	~260 MB	Reserved
	0x5006 2400 - 0x5006 27FF	1 KB	SDMMC1
	0x5006 2000 - 0x5006 23FF	1 KB	Reserved
	0x5006 1C00 - 0x5006 1FFF	1 KB	OCTOSPIIOM
	0x5006 0C00 - 0x5006 1BFF	4 KB	Reserved
	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5005 0800 - 0x5006 07FF	61 KB	Reserved
	0x5005 0400 - 0x5005 07FF	1 KB	Reserved
	0x5005 0000 - 0x5005 03FF	1 KB	DCMI
	0x5004 0400 - 0x5004 FFFF	62 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	OTG_FS
	0x4800 2400 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 2000 - 0x4800 23FF	1 KB	GPIOI
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA

Table 61. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DD}(MSI)(6)	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI @48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI @48 MHz clock.
5. Only accumulated jitter of MSI @48 MHz is extracted over 28 cycles.
   For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI @48 MHz, for 1000 captures over 28 cycles.
   For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI @48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

Figure 34. Typical current consumption versus MSI frequency

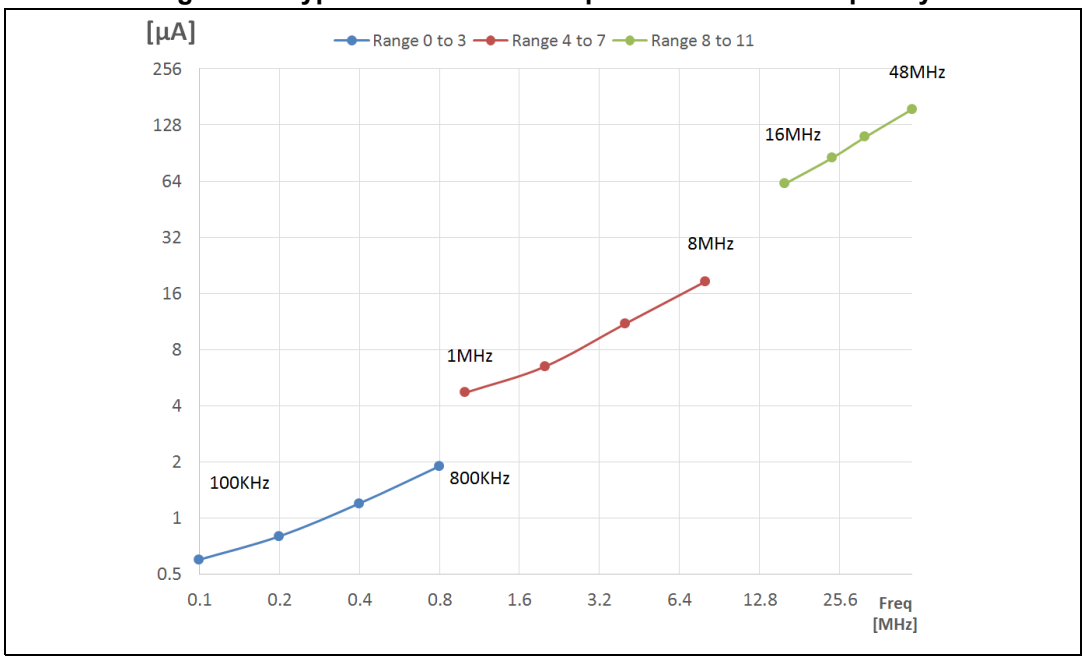


Table 65. MIPI D-PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hi-speed input/output characteristics						
U_{INST}	UI instantaneous	-	2	-	12.5	ns
V_{CMTX}	HS transmit common mode voltage	-	150	200	250	mV
$\|\Delta V_{CMTX}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0	-	-	-	5	
$\|V_{OD}\|$	HS transmit differential voltage	-	140	200	270	
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0	-	-	-	14	
V_{OHHS}	HS output high voltage	-	-	-	360	
Z_{OS}	Single ended output impedance	-	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch	-	-	-	10	%
t_{HSr} & t_{HSf}	20%-80% rise and fall time	-	100	-	0.35*UI	ps
LP receiver input characteristics						
V_{IL}	Logic 0 input voltage (not in ULP State)	-	-	-	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage in ULP State	-	-	-	300	
V_{IH}	Input high level voltage	-	880	-	-	
V_{hys}	Voltage hysteresis	-	25	-	-	
LP emitter output characteristics						
V_{IL}	Output low level voltage	-	1.1	1.2	1.2	V
$V_{IL-ULPS}$	Output high level voltage	-	-50	-	50	mV
V_{IH}	Output impedance of LP transmitter	-	110	-	-	Ω
V_{hys}	15%-85% rise and fall time	-	-	-	25	ns
LP contention detector characteristics						
V_{ILCD}	Logic 0 contention threshold	-	-	-	200	mV
V_{IHCD}	Logic 0 contention threshold	-	450	-	-	

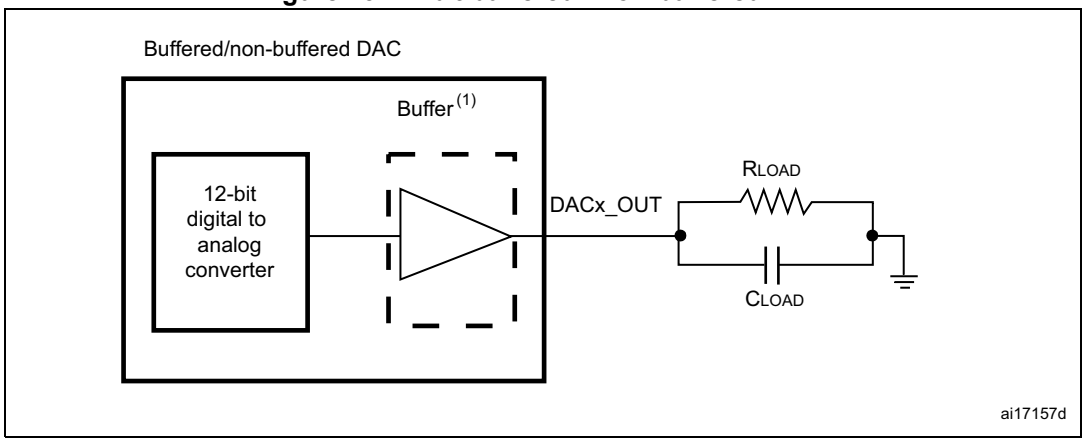
1. Guaranteed by characterization results.

Table 88. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 76: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0351 reference manual for more details.

Figure 43. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

USB OTG full speed (FS) characteristics

The device's USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 103. USB electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
V_{DI}(3)	Differential input sensitivity	Over VCM range	0.2	-	-	
V_{CM}(3)	Differential input common mode range	Includes V_{DI} range	0.8	-	2.5	
V_{SE}(3)	Single ended receiver input threshold	-	0.8	-	2.0	
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	
V_{OH}	Static output level high	R_L of 15 kΩ to 3.6 V(4)	2.8	-	3.6	
R_{PD}(3)	Pull down resistor on PA11, PA12 (USB_FS_DP/DM)	V_{IN} = V_{DD}	14.25	-	24.8	kΩ
R_{PU}(3)	Pull Up Resistor on PA12 (USB_FS_DP)	V_{IN} = V_{SS} during idle	0.9	1.25	1.575	
	Pull Up Resistor on PA12 (USB_FS_DP)	V_{IN} = V_{SS} during reception	1.425	2.25	3.09	
	Pull Up Resistor on PA10 (OTG_FS_ID)	-	-	-	14.5	

1. All the voltages are measured from the local ground potential.
2. The STM32L4R5xx USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at its default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 49. USB OTG timings – definition of data signal rise and fall time

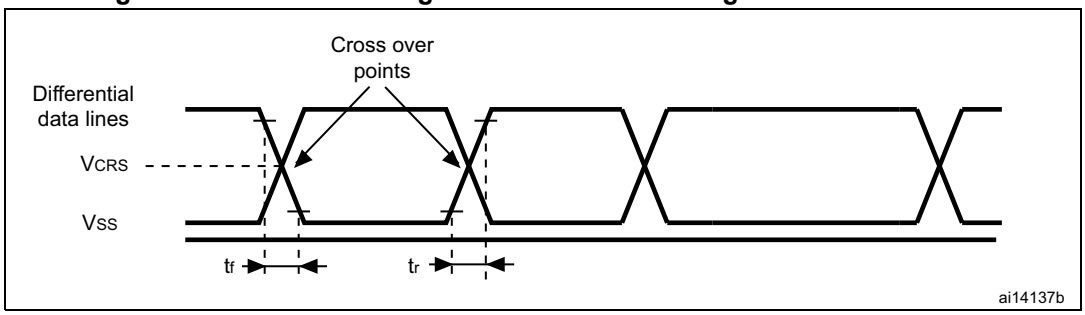


Table 104. USB OTG electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(2)				
t_{rfmLS}	Rise/ fall time matching in LS	t_r / t_f	80	125	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF			
t_{rfmFS}	Rise/ fall time matching in FS	t_r / t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 105. USB BCD DC electrical characteristics(1)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-		
RDAT_LKG	Data line leakage resistance	-	300	-	-	kΩ
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	V

Table 122. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and Hyperbus (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
$t_{w(CKH)}$	OctoSPI clock high and low time	-		$t_{(CK)}/2-1$	-	$t_{(CK)}/2+0.5$	ns
$t_{w(CKL)}$				$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2+0.5$	
$t_{v(CK)}$	Clock valid time	-		-	-	$t_{(CK)}+1$	
$t_{h(CK)}$	Clock hold time	-		$t_{(CK)}/2-0.5$	-	-	
$t_{w(CS)}$	Chip select high time	-		3 x $t_{(CK)}$	-	-	
$t_{v(DQ)}$	Data input vallid time	-		0	-	-	
$t_{v(DS)}$	Data storbe input valid time	-		0	-	-	
$t_{h(DS)}$	Data storbe input hold time	-		0	-	-	
$t_{v(RWDS)}$	Data storbe output valid time	-		-	-	3 x $t_{(CK)}$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	Voltage Range 1		-3.5	-	$t_{(CK)}/2-5.75$(3)	
		Voltage Range 2		-5.5	-	$t_{(CK)}/2-9$(3)	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	Voltage Range 1		5.75	-	-	
		Voltage Range 2		9	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	-	4.5	6	ns
			DHQC = 1 Pres=1,2 ...		tpclk/4+1.5	tpclk/4+2.25	
		Voltage Range 2	DHQC = 0		8	11	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	0.5	-	-	
			DHQC = 1 Pres=1,2 ...	tpclk/4-1.75	-	-	
		Voltage Range 2	DHQC = 0	0.75	-	-	

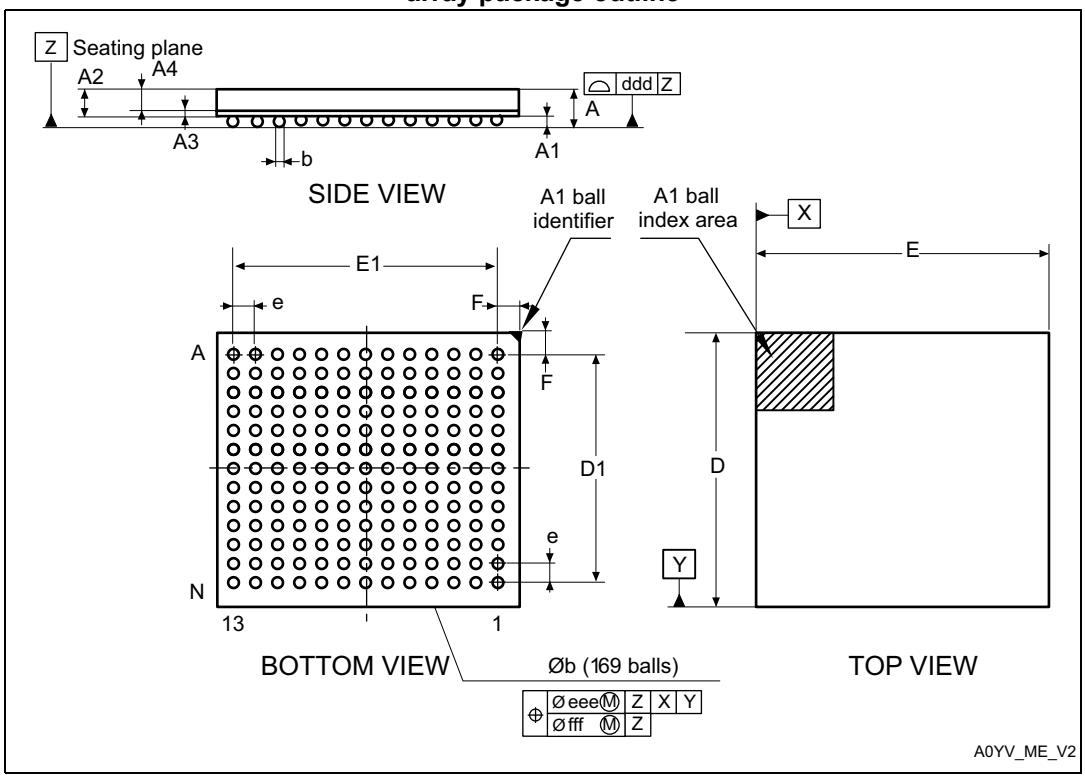
1. Guaranteed by characterization results.
2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.
3. Data input setup time maximum does not take into account Data level switching duration.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA169 package information

Figure 72. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



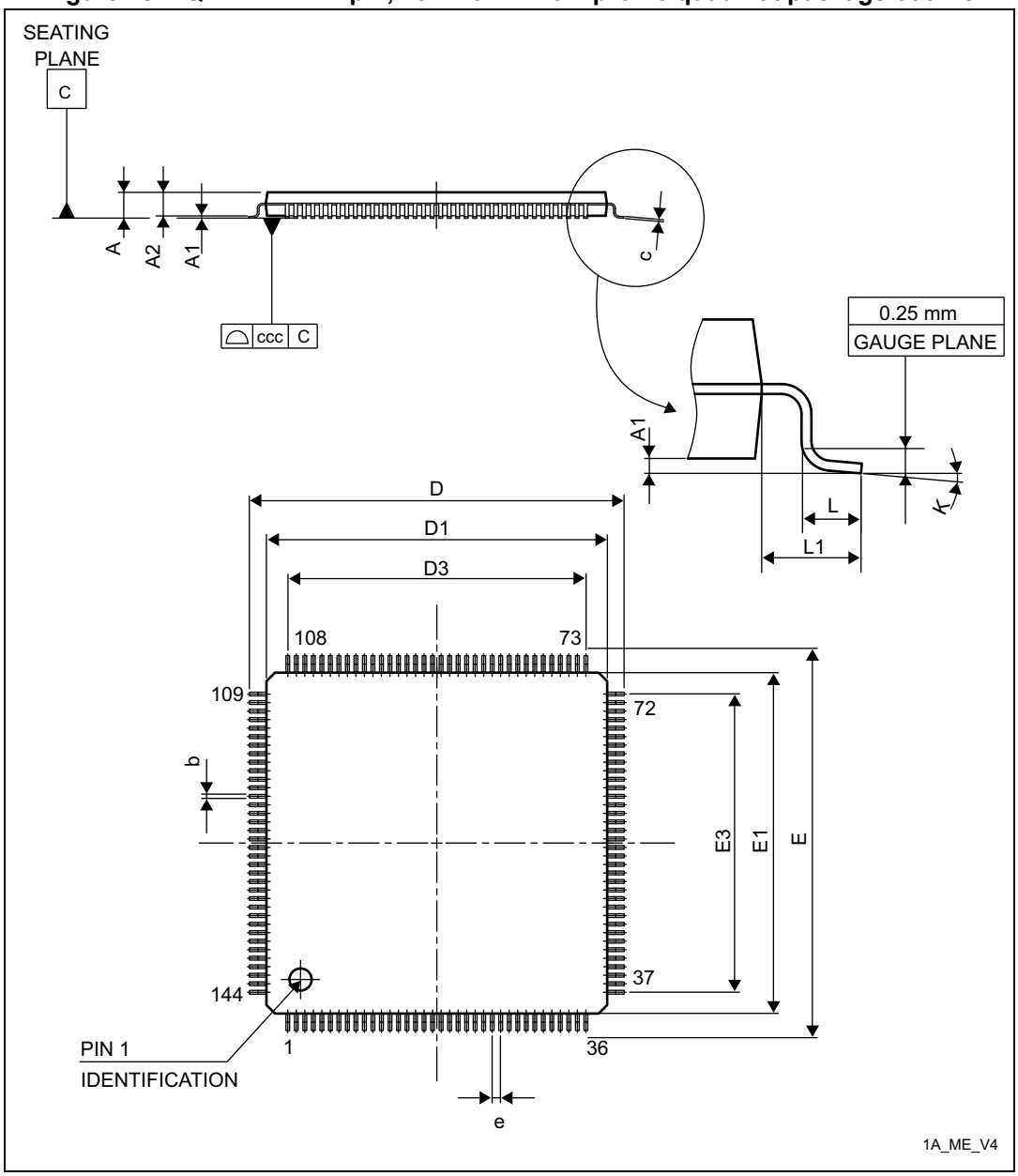
1. Drawing is not to scale.

Table 127. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146

7.3 LQFP144 package information

Figure 78. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



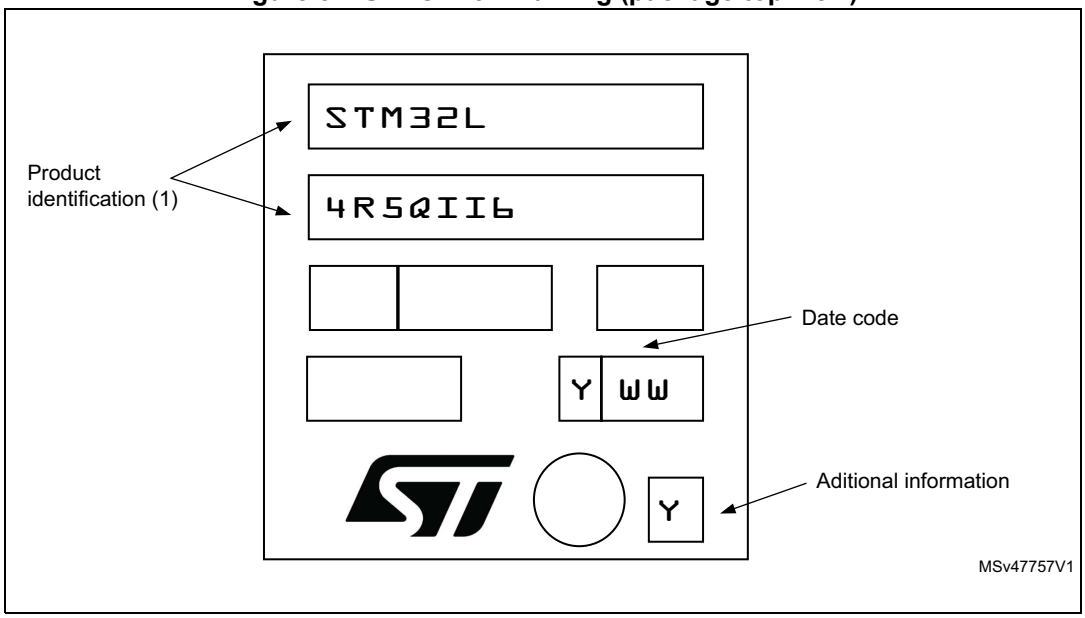
1. Drawing is not to scale.

UFBGA132 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 87. UFBGA132 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.