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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	110
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5qii6

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Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Gray cells highlight the wakeup capability in each mode.

2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off. In Stop 2 mode, the content of SRAM3 is preserved or not depending on the RRSTP bit in PWR_CR1 register.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.10.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.39 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume.

The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

The major features are:

- Combined Rx and Tx FIFO size of 1.25 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- One bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- Eight host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- Software configurable to OTG 1.3 and OTG 2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery charging specification revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

The synchronization for this oscillator can also be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.40 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.41 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named flexible memory controller (FMC).

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN0	USART3_RTS_DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS_NSS
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	DFSDM1_DATIN5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	DFSDM1_CKIN5	USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	DFSDM1_CKOUT	DFSDM1_DATIN6	-
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	DFSDM1_CKIN6	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	DFSDM1_DATIN7	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C2_SMBA	SPI2_NSS	DFSDM1_DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS_NSS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS_DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port I	PI0	-	-	TIM5_CH4	OCTOSPIM_P1_IO5	-	SPI2_NSS	-	-
	PI1	-	-	-	-	-	SPI2_SCK	-	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI	-	-
	PI4	-	-	-	TIM8_BKIN	-	-	-	-
	PI5	-	-	-	TIM8_CH1	-	OCTOSPIM_P2_NCS	-	-
	PI6	-	-	-	TIM8_CH2	-	OCTOSPIM_P2_CLK	-	-
	PI7	-	-	-	TIM8_CH3	-	-	-	-
	PI8	-	-	-	-	-	OCTOSPIM_P2_NCS	-	-
	PI9	-	-	-	-	-	OCTOSPIM_P2_IO2	-	-
	PI10	-	-	-	-	-	OCTOSPIM_P2_IO1	-	-
	PI11	-	-	-	-	-	OCTOSPIM_P2_IO0	-	-

1. Refer to *Table 17* for AF8 to AF15.

3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	120	
f_{PCLK2}	Internal APB2 clock frequency	-	0	120	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DD12}	Standard operating voltage	Up to 120 MHz	1.14	1.32	
		Up to 80 MHz	1.08	1.32	
		Up to 26 MHz	1.05 (2)	1.32	
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	

Table 34. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.75	4.85	6.45	9.30	4.70	5.6	7.6	11.0	17.0	mA
				16 MHz	2.20	2.55	3.65	5.20	8.10	3.20	4.1	6.1	9.4	16.0	
				8 MHz	1.20	1.55	2.65	4.25	7.10	1.70	2.7	4.7	8.0	14.0	
				4 MHz	0.74	1.10	2.15	3.75	6.60	1.20	2.0	4.0	7.3	14.0	
				2 MHz	0.49	0.85	1.95	3.50	6.35	0.79	1.6	3.6	6.9	13.0	
				1 MHz	0.37	0.73	1.80	3.40	6.20	0.61	1.4	3.4	6.7	13.0	
				100 KHz	0.26	0.62	1.70	3.25	6.10	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.00	18.50	20.00	22.50	26.50	19.00	21.0	24.0	28.0	36.0(2)	
			Range 1 Normal Mode	80 MHz	11.00	11.50	13.50	15.50	19.00	15.00	16.0	19.0	23.0	30.0(2)	
				72 MHz	10.00	10.50	12.00	14.00	18.00	13.00	15.0	18.0	22.0	29.0	
				64 MHz	9.10	9.60	11.00	13.00	16.50	12.00	13.0	16.0	20.0	27.0	
				48 MHz	7.20	7.70	9.20	11.00	14.50	11.00	12.0	15.0	19.0	26.0	
				32 MHz	4.90	5.40	6.85	8.80	12.50	7.30	8.5	12.0	16.0	23.0	
				24 MHz	3.75	4.25	5.65	7.65	11.00	5.60	6.7	9.3	14.0	21.0	
				16 MHz	2.60	3.10	4.50	6.45	9.90	4.10	5.2	7.7	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable FLASH in power-down		2 MHz	435	885	2150	3950	7100	800	1800	4200	7800	15000	µA
				1 MHz	300	745	2000	3800	6950	580	1600	4000	7600	14000	
				400 KHz	225	655	1900	3700	6850	420	1400	3800	7500	14000	
				100 KHz	180	620	1900	3650	6800	370	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 40. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions		Code	TYP	Unit	TYP	Unit
		-	Voltage scaling		25°C		25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	3.35	mA	129	µA/MHz
				Coremark	3.10		119	
				Dhrystone2.1	3.65		140	
				Fibonacci	3.20		123	
				While(1)	2.85		110	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	11.0	mA	138	µA/MHz
				Coremark	10.5		131	
				Dhrystone2.1	12.5		156	
				Fibonacci	10.5		131	
				While(1)	9.40		118	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.0	mA	150	µA/MHz
				Coremark	16.5		138	
				Dhrystone2.1	19.5		163	
				Fibonacci	17.5		146	
				While(1)	15.0		125	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	435	µA	218	µA/MHz
				Coremark	395		198	
				Dhrystone2.1	470		235	
				Fibonacci	425		213	
				While(1)	455		228	

1. Reduced code used for characterization results provided in *Table 26*, *Table 30*, *Table 34*.

Table 44. Current consumption in Low-power sleep mode, Flash in power-down

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (LPSleep)	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	255	645	1950	3700	6850	430	1400	3700	7400	14000	µA
				1 MHz	195	620	1900	3700	6850	370	1300	3700	7400	14000	
				400 KHz	180	600	1900	3700	6800	350	1300	3700	7400	14000	
				100 KHz	175	595	1900	3650	6800	340	1300	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 47. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	120	430	1400	2750	5050	280	1100	3300	6500	13000	µA
			2.4 V	120	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3.6 V	120	430	1400	2750	5150	280	1100	3300	6600	13000(2)	
IDD (Stop 1 with RTC)	Supply current in STOP 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	120	430	1400	2700	5050	280	1100	3300	6500	13000	
			2.4 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6600	13000	
			3.6 V	125	435	1400	2750	5150	280	1100	3300	6600	13000	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	120	430	1400	2750	5050	300	1100	3500	6900	13000	
			2.4 V	120	435	1400	2750	5100	300	1100	3500	6900	13000	
			3 V	125	435	1400	2750	5100	320	1100	3500	6900	13000	
			3.6 V	125	435	1400	2750	5150	320	1100	3500	6900	13000	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			2.4 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3.6 V	120	425	1350	2700	-	300	1100	3400	6800	-	
IDD (wakeup from Stop 1)	Supply current during wakeup from Stop 1 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(4)	3 V	2.10	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(4)	3 V	0.70	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(4)	3 V	1.50	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*

Table 53. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	12.6	14.5	µs
			Wakeup clock HSI16 = 16 MHz	12.2	14.0	
		Range 2	Wakeup clock MSI = 24 MHz	22.1	24.1	
			Wakeup clock HSI16 = 16 MHz	21.3	23.3	
			Wakeup clock MSI = 4 MHz	25.1	27.1	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.3	7.0	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
		Range 2	Wakeup clock MSI = 24 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
			Wakeup clock MSI = 4 MHz	10.9	12.6	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	20.4	22.4	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			16.8	19.0	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	13.1	14.8	µs
			Wakeup clock HSI16 = 16 MHz	12.6	14.4	
		Range 2	Wakeup clock MSI = 24 MHz	22.6	24.6	
			Wakeup clock HSI16 = 16 MHz	21.7	23.7	
			Wakeup clock MSI = 4 MHz	25.8	27.9	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
		Range 2	Wakeup clock MSI = 24 MHz	6.4	8.0	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
			Wakeup clock MSI = 4 MHz	11.9	13.6	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 58*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 58. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 31*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 36. MIPI D-PHY HS/LP clock lane transition timing diagram

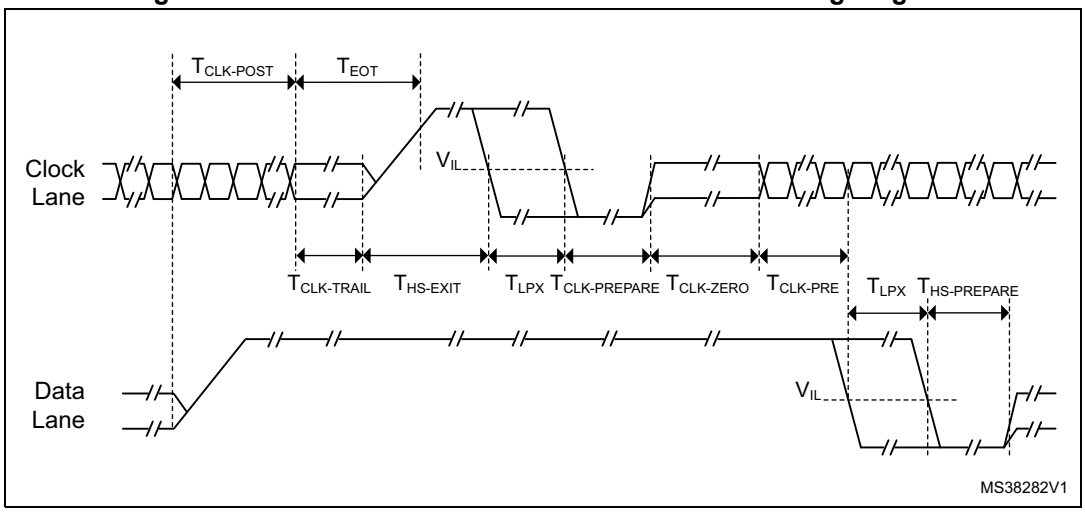
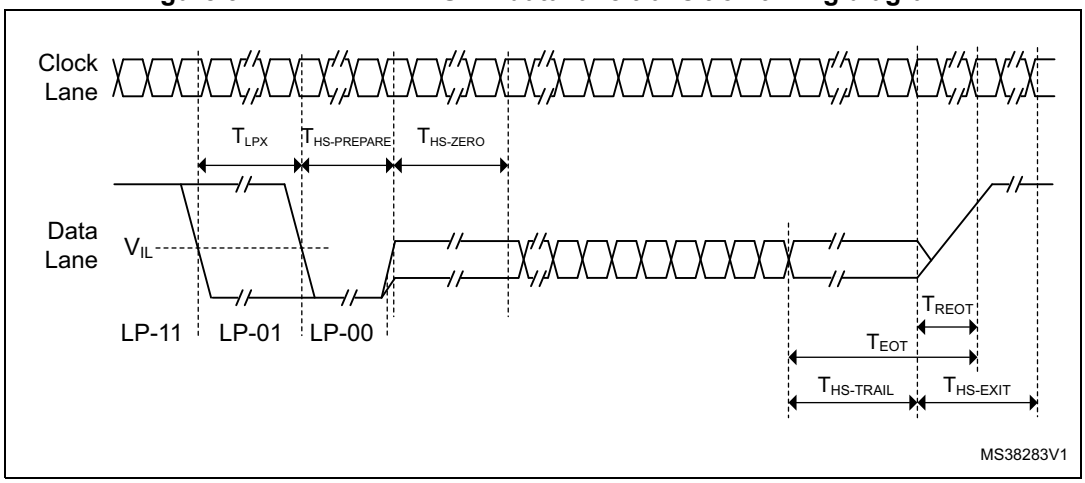


Figure 37. MIPI D-PHY HS/LP data lane transition timing diagram



6.3.11 MIPI D-PHY PLL characteristics

The parameters given in *Table 67* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 67. DSI-PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	4	-	100	MHz
f_{PLL_INFIN}	PFD input clock	-	4	-	25	
f_{PLL_OUT}	PLL multiplier output clock	-	31.25	-	500	
f_{VCO_OUT}	PLL VCO output	-	500	-	1000	
t_{LOCK}	PLL lock time	-	-	-	200	µs

Table 78. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0351 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

6.3.21 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 82* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 22: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 82. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	80	MHz
		Range 2	-	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$

Table 91. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	-(4)	nA

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 25: Embedded internal voltage reference*.
3. Guaranteed by characterization results.
4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in *Table 76: I/O static characteristics*.

6.3.25 Operational amplifiers characteristics

Table 92. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.	-	-	±1.5	mV
		All voltage/Temp.	-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode	-	±5	-	µV/°C
		Low-power mode	-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-	-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-	-	1	1.35	

Figure 54. Synchronous multiplexed NOR/PSRAM read timings

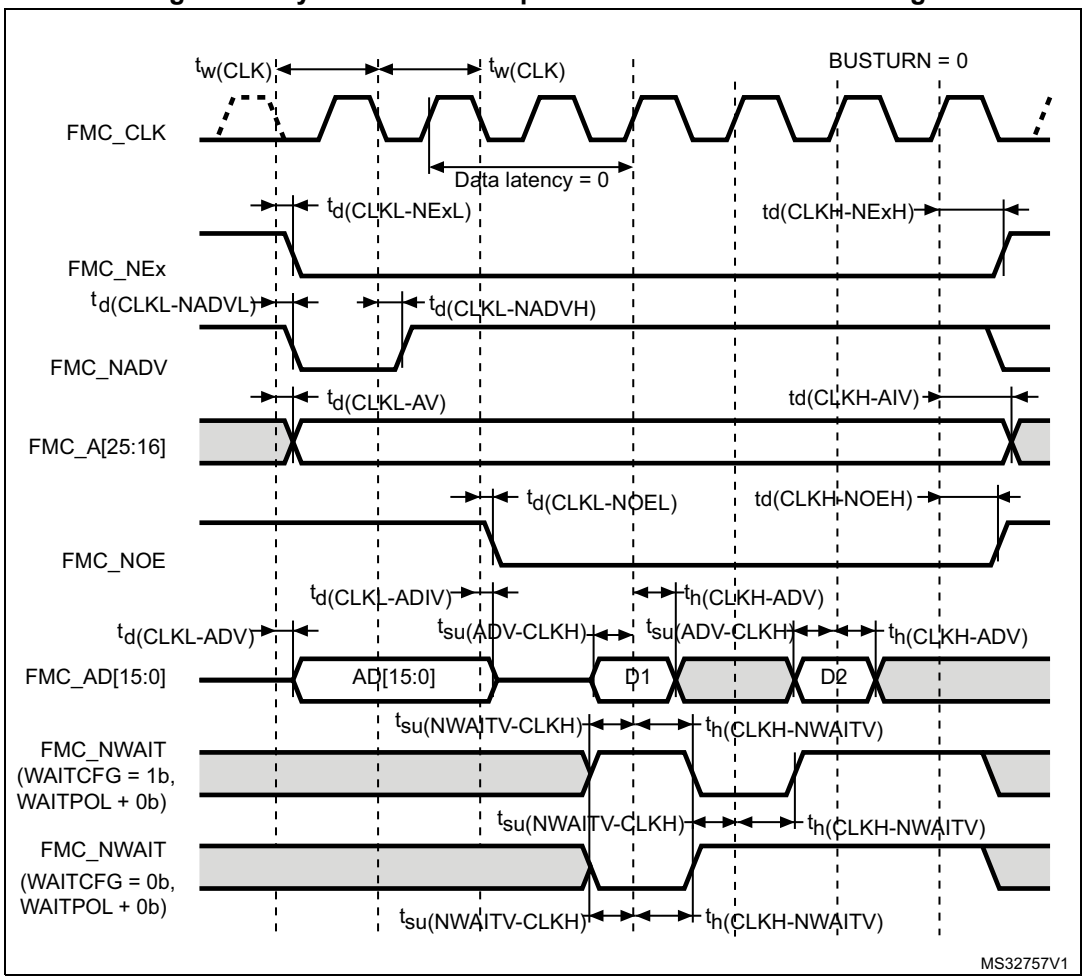


Figure 61. NAND controller waveforms for common memory write access

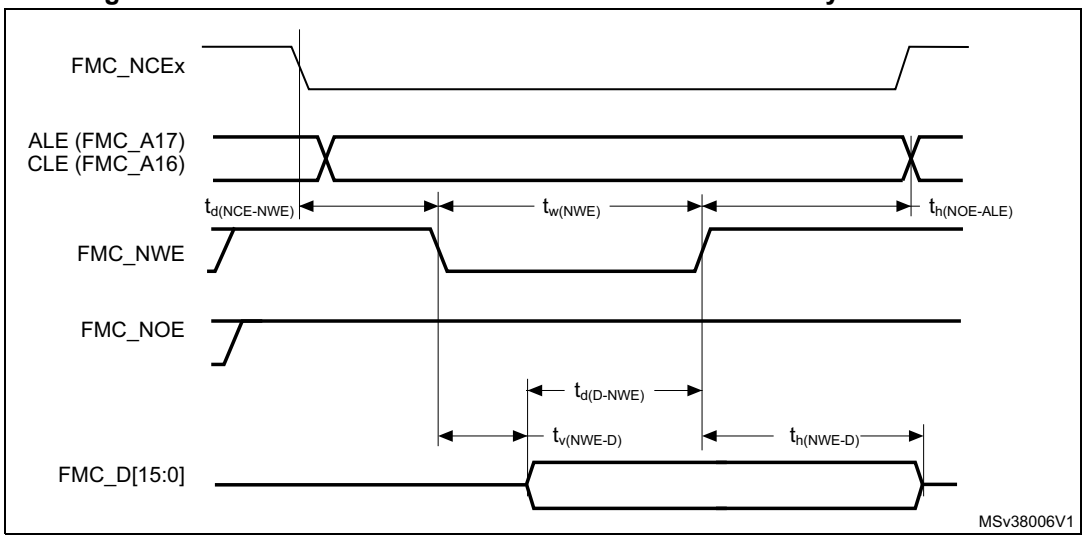


Table 118. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	14	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 119. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$2T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$-1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.32 OctoSPI characteristics

Unless otherwise specified, the parameters given in *Table 120*, *Table 121* and *Table 122* for OctoSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency

Figure 62. OctoSPI timing diagram - SDR mode

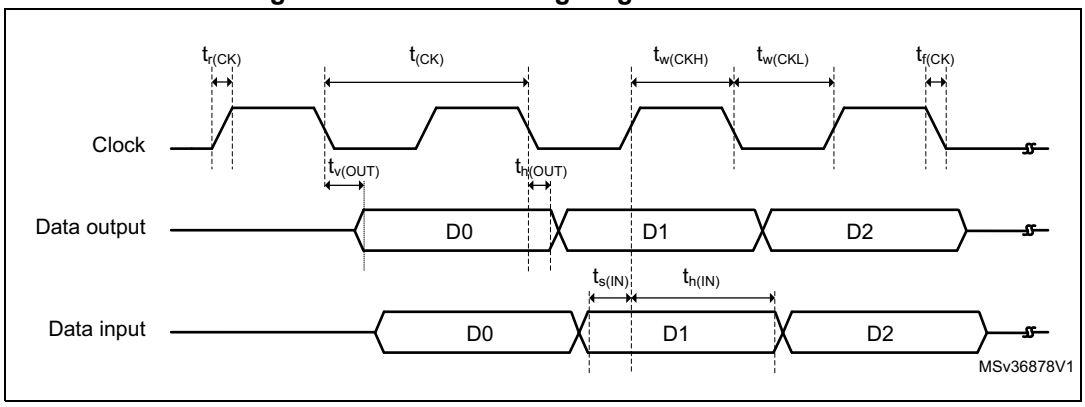


Figure 63. OctoSPI timing diagram - DDR mode

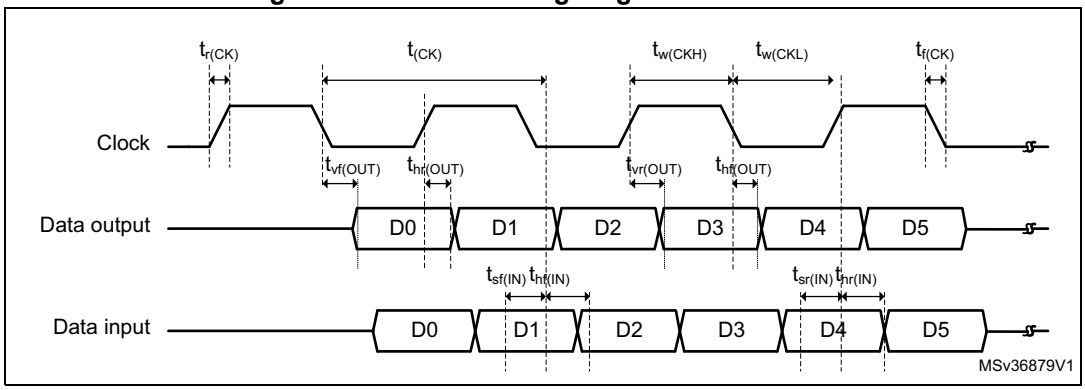


Figure 64. OctoSPI Hyperbus clock