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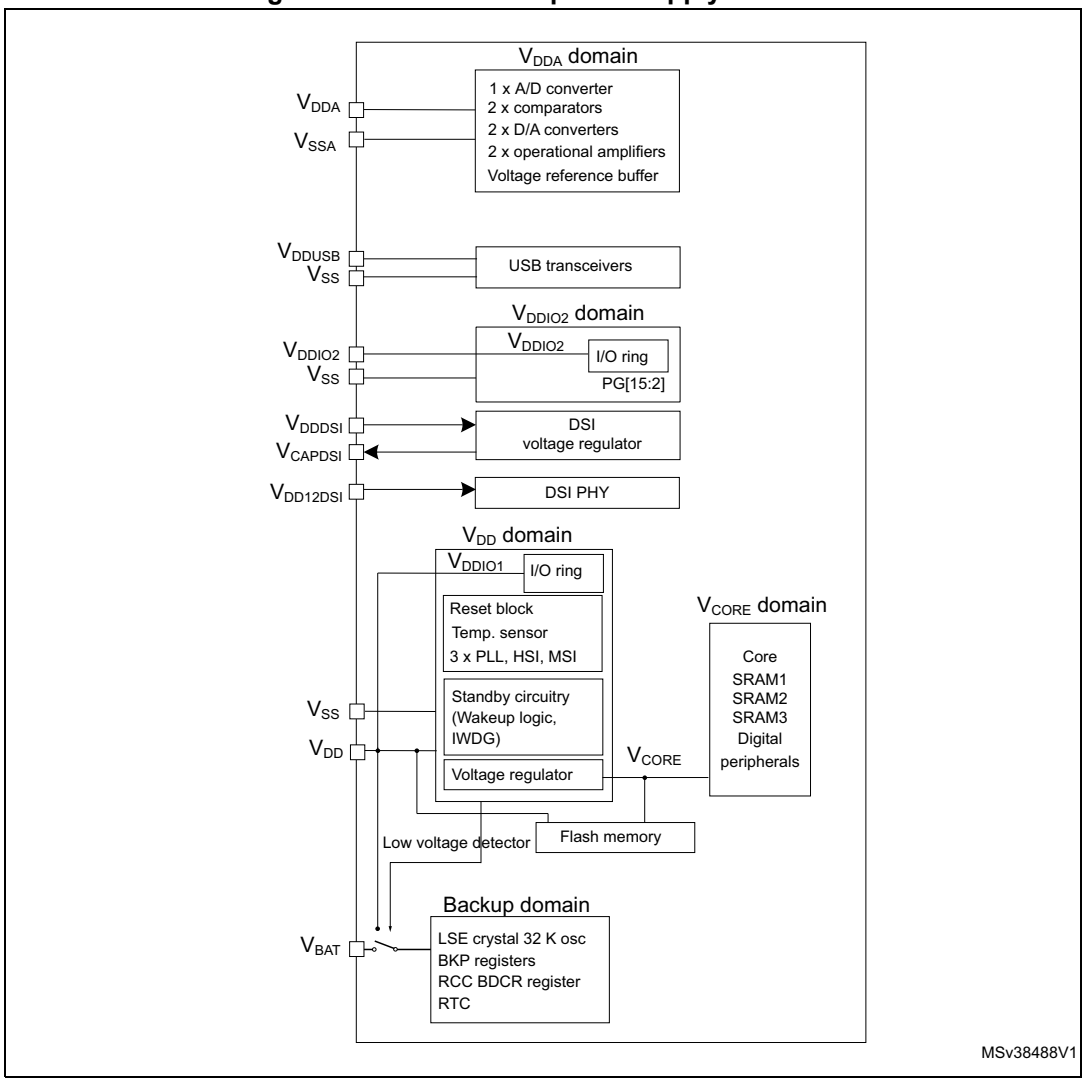
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5vgt6

Figure 5. STM32L4R9xx power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}) must remain below VDD +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

retained in Standby mode, supplied by the low-power regulator (standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2, SRAM3 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.30.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.30.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

4 Pinouts and pin description

Figure 9. STM32L4R5xx and STM32L4R7xx UFBGA169 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv38036V4

1. The above figure shows the package top view.

Figure 10. STM32L4R9xx UFBGA169 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PH9	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PA10	VDDUSB	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PA8	PA9	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PC8	PG8	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG13	PG4	PG3	PG5	PG7	PC7	PG6	PC9
H	PH0-OSC_IN	VSS	NRST	PF10	PG1	PE10	PB11	PD13	PG2	PD15	PD14	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PG0	PE9	PE15	PD12	PD11	PD10	DSI_D1P	DSI_D1N	VSSDSI
K	PC3	VSSA/VREF-	PA0	PC4	PF15	PE8	PE14	PH4	PD9	PD8	DSI_CKP	DSI_CKN	VSSDSI
L	VREF+	VDDA	PA5	PA6	PB1	PF14	PE7	PE13	PH5	PB15	DSI_D0P	DSI_D0N	VCAPDSI
M	PA1	PA3	VSS	PA7	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB14	VDDDSI
N	PA2	PA4	VDD	PB0	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv45223V2

1. The above figure shows the package top view.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	F3	F3	14	14	F10	G4	G4	-	14	F3	F10	F10	G4	PF4	I/O	FT	-	OCTOSPIM_P2_CLK, FMC_A4, EVENTOUT	-
-	F4	F4	15	15	F9	G5	G5	-	15	F4	F9	F9	G5	PF5	I/O	FT	-	FMC_A5, EVENTOUT	-
10	F2	F2	16	16	G11	F2	F2	10	16	L6	G11	G11	F2	VSS	S	-	-	-	-
11	G2	G2	17	17	G12	G2	G2	11	17	G1	G12	G12	G2	VDD	S	-	-	-	-
-	-	-	18	18	G10	-	-	-	18	F2	G10	G10	-	PF6	I/O	FT	-	TIM5_ETR, TIM5_CH1, OCTOSPIM_P1_IO3, SAI1_SD_B, EVENTOUT	-
-	-	-	19	19	G9	-	-	-	19	F5	G9	G9	-	PF7	I/O	FT	-	TIM5_CH2, OCTOSPIM_P1_IO2, SAI1_MCLK_B, EVENTOUT	-
-	-	-	20	20	NC	-	-	-	-	F1	NC	NC	-	PF8	I/O	FT	- (3)	TIM5_CH3, OCTOSPIM_P1_IO0, SAI1_SCK_B, EVENTOUT	-
-	-	-	21	21	NC	-	-	-	-	G4	NC	NC	-	PF9	I/O	FT	(3)	TIM5_CH4, OCTOSPIM_P1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
42	M9	M9	64	64	L5	N8	N8	39	60	H7	L5	L5	N8	PE11	I/O	FT	-	TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, OCTOSPIM_P1_NCS, LCD_G4, FMC_D8, EVENTOUT	-
43	L9	L9	65	65	M5	M8	M8	40	61	M9	M5	M5	M8	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, OCTOSPIM_1_IO0, LCD_G5, FMC_D9, EVENTOUT	-
44	M10	M10	66	66	J5	L8	L8	41	62	J8	J5	J5	L8	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, OCTOSPIM_P1_IO1, LCD_G6, FMC_D10, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	-	-	-	-	-	A2	A2	-	-	-	-	-	A2	PH2	I/O	FT	-	OCTOSPIM_P1_IO4, EVENTOUT	-
-	-	-	-	-	-	B2	B2	-	-	-	-	-	B2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	-	-	-	-	-	B1	B1	-	-	-	-	-	B1	PI9	I/O	FT	-	OCTOSPIM_P2_IO2, CAN1_RX, EVENTOUT	-
-	-	-	-	-	-	A1	A1	-	-	-	-	-	A1	PI10	I/O	FT	-	OCTOSPIM_P2_IO1, EVENTOUT	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0432 reference manual.
3. NC (not-connected) balls must be left unconnected. However, non connected (NC) GPIOS are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low-power modes.
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

5 Memory mapping

Figure 23. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map

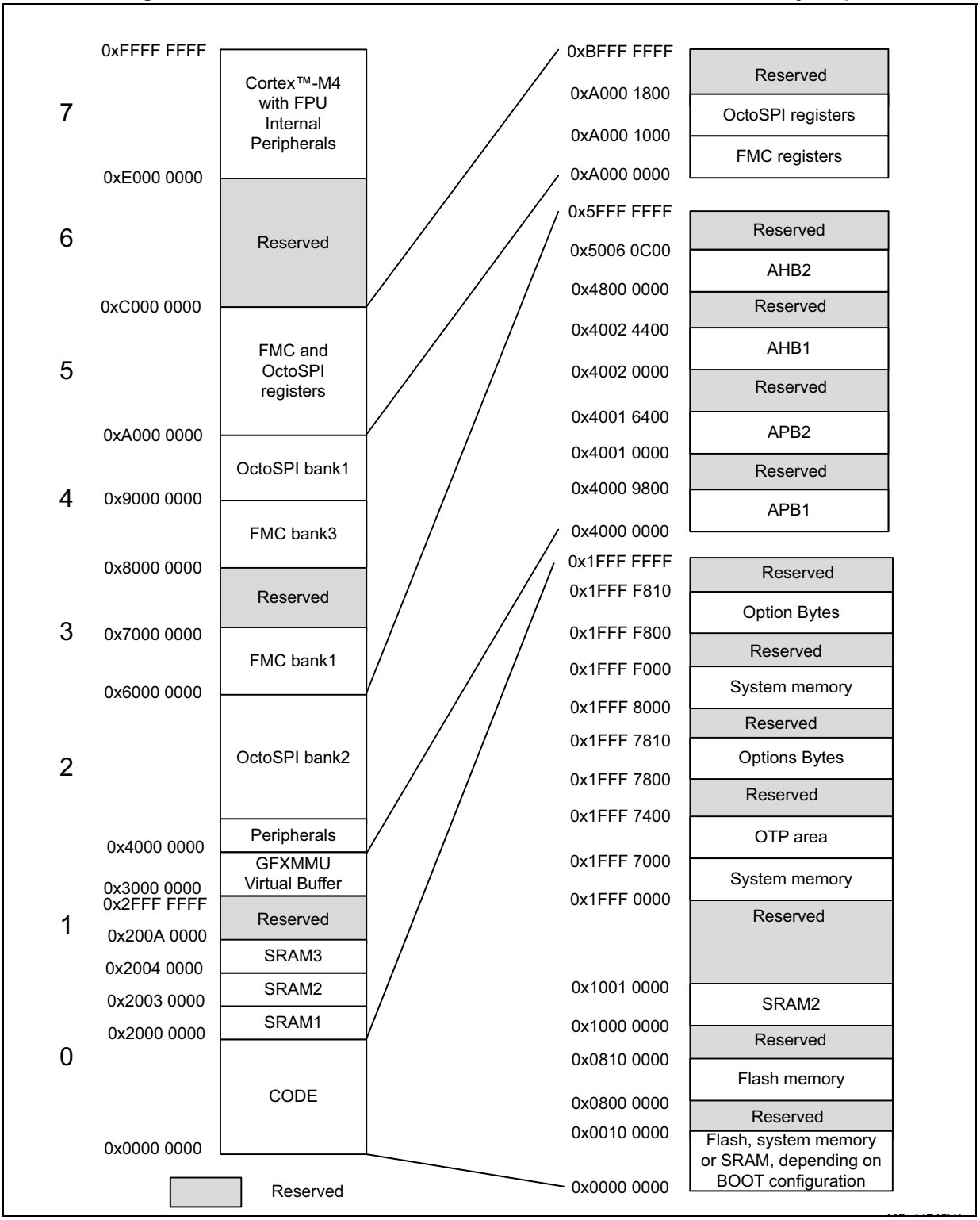


Table 24. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code

The current consumption is measured as described in *Figure 27: Current consumption measurement*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0432 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- The voltage scaling Range 1 is adjusted to f_{HCLK} frequency as follows:
  - Voltage Range 1 Boost mode for 80 MHz < f_{HCLK} <= 120 MHz
  - Voltage Range 1 Normal mode for 26 MHz < f_{HCLK} <= 80 MHz

The parameters given in *Table 26* to *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 37. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	VDD12	f_{HCLK}	Code	25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.05V	f_{HCLK}= 26 MHz	Reduced code	1.34	1.41	mA	51	54	µA/MHz
					Coremark	1.53	1.55		59	60	
					Dhrystone2.1	1.67	1.69		64	65	
					Fibonacci	1.43	1.53		55	59	
					While(1)	1.24	1.24		48	48	
			VDD12=1.10V	f_{HCLK}= 26 MHz	Reduced code	1.47	1.55	mA	56	60	µA/MHz
					Coremark	1.68	1.70		65	66	
					Dhrystone2.1	1.83	1.85		71	71	
					Fibonacci	1.57	1.68		61	65	
					While(1)	1.36	1.36		52	52	
				f_{HCLK}= 80 MHz	Reduced code	4.13	4.49	mA	52	56	µA/MHz
					Coremark	4.85	4.85		61	61	
					Dhrystone2.1	5.21	5.21		65	65	
					Fibonacci	4.49	5.03		56	63	
					While(1)	3.77	3.77		47	47	

Table 47. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	120	430	1400	2750	5050	280	1100	3300	6500	13000	µA
			2.4 V	120	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3.6 V	120	430	1400	2750	5150	280	1100	3300	6600	13000(2)	
IDD (Stop 1 with RTC)	Supply current in STOP 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	120	430	1400	2700	5050	280	1100	3300	6500	13000	
			2.4 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6600	13000	
			3.6 V	125	435	1400	2750	5150	280	1100	3300	6600	13000	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	120	430	1400	2750	5050	300	1100	3500	6900	13000	
			2.4 V	120	435	1400	2750	5100	300	1100	3500	6900	13000	
			3 V	125	435	1400	2750	5100	320	1100	3500	6900	13000	
			3.6 V	125	435	1400	2750	5150	320	1100	3500	6900	13000	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			2.4 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3.6 V	120	425	1350	2700	-	300	1100	3400	6800	-	
IDD (wakeup from Stop 1)	Supply current during wakeup from Stop 1 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(4)	3 V	2.10	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(4)	3 V	0.70	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(4)	3 V	1.50	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 53* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 53. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		7	9	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	9.1	9.8	µs
			Wakeup clock HSI16 = 16 MHz	8.5	9.0	
		Range 2	Wakeup clock MSI = 24 MHz	18.8	19.7	
			Wakeup clock HSI16 = 16 MHz	17.6	18.3	
			Wakeup clock MSI = 4 MHz	23.9	25.7	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	1.9	2.5	
			Wakeup clock HSI16 = 16 MHz	2.6	2.9	
		Range 2	Wakeup clock MSI = 24 MHz	2.6	3.1	
			Wakeup clock HSI16 = 16 MHz	2.6	3.0	
			Wakeup clock MSI = 4 MHz	10.0	11.5	

Table 53. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	30.7	47.8	µs
			Wakeup clock MSI = 4 MHz	40.4	55.6	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	32.1	49.1	
			Wakeup clock MSI = 4 MHz	41.5	55.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	265.0	339.4	

1. Guaranteed by characterization results.

Table 54. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low- power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 55. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by characterization results.

Table 84. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 86. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 92. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

Figure 56. Synchronous non-multiplexed NOR/PSRAM read timings

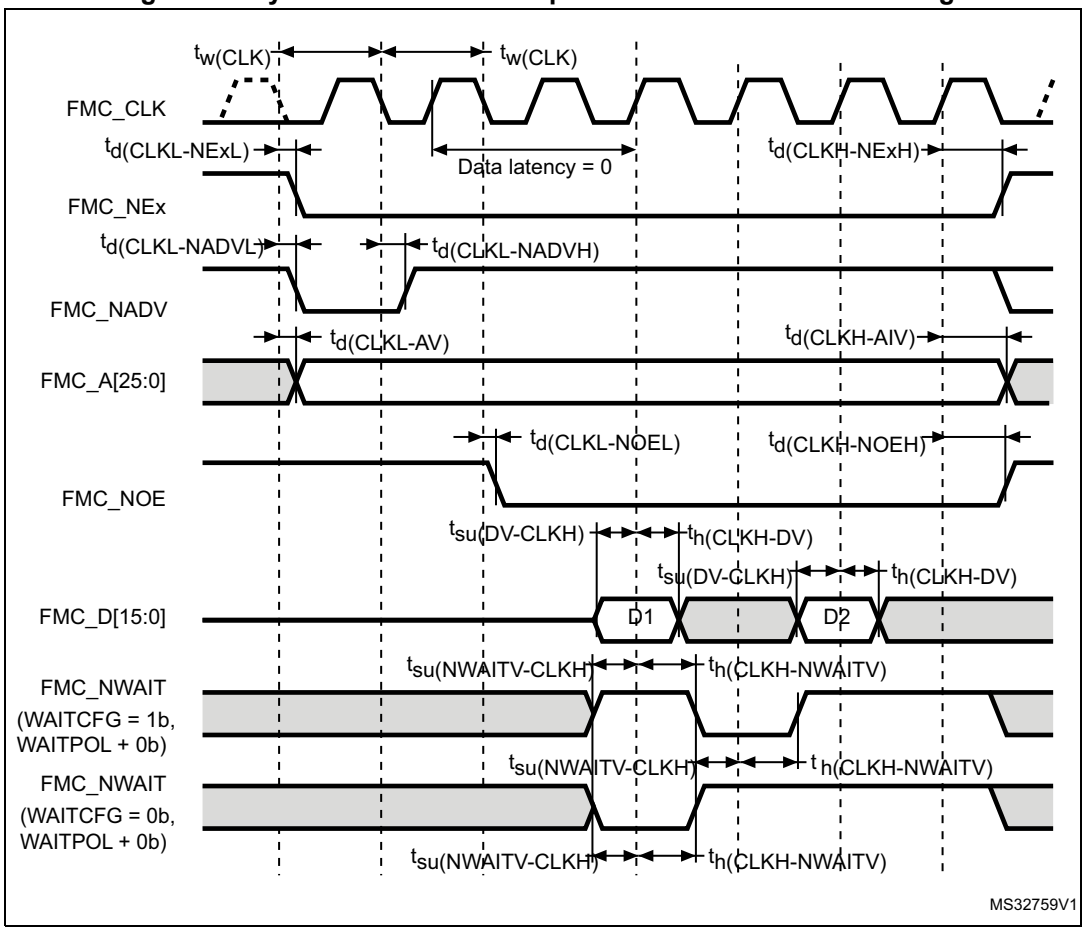


Table 116. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK} -0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +0.5	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	RxT_{HCLK}/2 +1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	4	-	

and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 120. OctoSPI(1) characteristics in SDR mode(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(QCK)	OctoSPI clock frequency	1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	58	MHz
		2.7 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	86	
		1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 15 pF	-	-	66	
		1.71 V < V_{DD}< 3.6 V Voltage Range 2 C_{LOAD} = 20 pF	-	-	26	
$t_{w(CKH)}$	OctoSPI clock high and low time	Prescaler = 0	$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$			$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	0.5	-	-	
		Voltage Range 2	0	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	7.75	-	-	
		Voltage Range 2	10.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	2	3.5	
		Voltage Range 2	-	4	5.5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.

Figure 67. OctoSPI Hyperbus write