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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5vit6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L4Rxxx microcontrollers.

This document should be read in conjunction with the STM32L4Rxxx reference manual (RM0432). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	F9	F9	88	88	F5	J11	J11	-	92	F7	F5	F5	G8	PG3	I/O	FT_s	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	F10	F10	89	89	F6	J10	J10	-	93	F10	F6	F6	G7	PG4	I/O	FT_s	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	E9	E9	90	90	F7	J9	J9	-	94	F8	F7	F7	G9	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	G4	G4	91	91	E5	G11	G11	-	95	F9	E5	E5	G12	PG6	I/O	FT_s	-	OCTOSPIM_P1_DQS, I2C3_SMBA, LPUART1_RTS_DE, LCD_R1, DSI_TE, EVENTOUT	-
-	H4	H4	92	92	E1	H10	H10	-	96	E11	E1	E1	G10	PG7	I/O	FT_fs	-	SAI1_CK1, I2C3_SCL, OCTOSPIM_P2_DQS, DFSDM1_CKOUT, LPUART1_TX, FMC_INT, SAI1_MCLK_A, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
71	A12	A12	104	104	C2	D13	D13	73	106	B11	C2	C2	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT	-
72	A11	A11	105	105	B3	A11	A11	74	107	B10	B3	B3	A11	PA13 (JTMS/ SWDIO)	I/O	FT	- (4)	JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SAI1_SD_B, EVENTOUT	-
73	C11	C11	106	106	B2	E12	E12	75	108	C11	B2	B2	D12	VDDUSB	S	-	-	-	-
74	F11	F11	107	107	A1	C12	C12	76	109	A12	A1	A1	C12	VSS	S	-	-	-	-
75	G11	G11	108	108	B1	C13	C13	77	110	A11	B1	B1	C13	VDD	S	-	-	-	-
-	-	-	-	-	-	E11	E11	-	-	-	-	-	-	PH6	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_CLK, DCMI_D8, EVENTOUT	-
-	-	-	-	-	-	D12	D12	-	-	-	-	-	-	PH7	I/O	FT_f	-	I2C3_SCL, DCMI_D9, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
93	B4	B4	136	137	A9	D5	D5	95	137	C5	A9	A9	D5	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, I2C4_SDA, DFSDM1_CKIN5, USART1_RX, UART4_CTS, TSC_G2_IO4, DCMI_VSYNC, DSI_TE, FMC_NL, TIM17_CH1N, EVENTOUT	COMP2_INM, PVD_IN
94	A4	A4	137	138	B9	E5	E5	96	138	A4	B9	B9	E5	PH3-BOOT0	I/O	FT	-	EVENTOUT	-
95	A3	A3	138	139	C10	C4	C4	97	139	B4	C10	C10	C4	PB8	I/O	FT_fl	-	TIM4_CH3, SAI1_CK1, I2C1_SCL, DFSDM1_CKOUT, DFSDM1_DATIN6, SDMMC1_CKIN, CAN1_RX, DCMI_D6, LCD_B1, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-

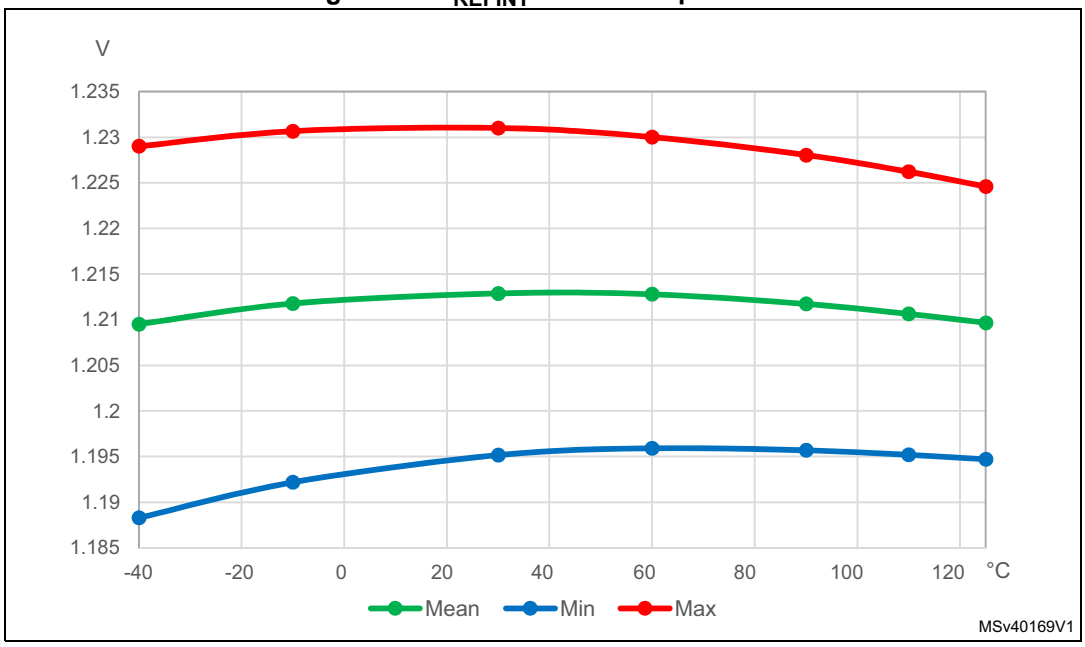
Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	DFSDM1_DATIN4	-
	PC1	TRACED0	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-	DFSDM1_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_CKOUT	-
	PC3	-	LPTIM1_ETR	-	SAI1_D1	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	SAI1_D3	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	TRACED0	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	DCMI_D3	-	I2C3_SDA	-
	PC10	TRACED1	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	DCMI_D2	OCTOSPIM_P1_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	OCTOSPIM_P2_IO0	-	-
	PF1	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_IO1	-	-
	PF2	-	-	-	-	I2C2_SMBA	OCTOSPIM_P2_IO2	-	-
	PF3	-	-	-	-	-	OCTOSPIM_P2_IO3	-	-
	PF4	-	-	-	-	-	OCTOSPIM_P2_CLK	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	OCTOSPIM_P1_CLK	-	-	DFSDM1_CKOUT	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	OCTOSPIM_P2_DQS	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM1_DATIN6	-
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Figure 28. V_{REFINT} versus temperature



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.17*. However, the recommended clock input waveform is shown in *Figure 30*.

Table 57. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 30. Low-speed external clock source AC timing diagram

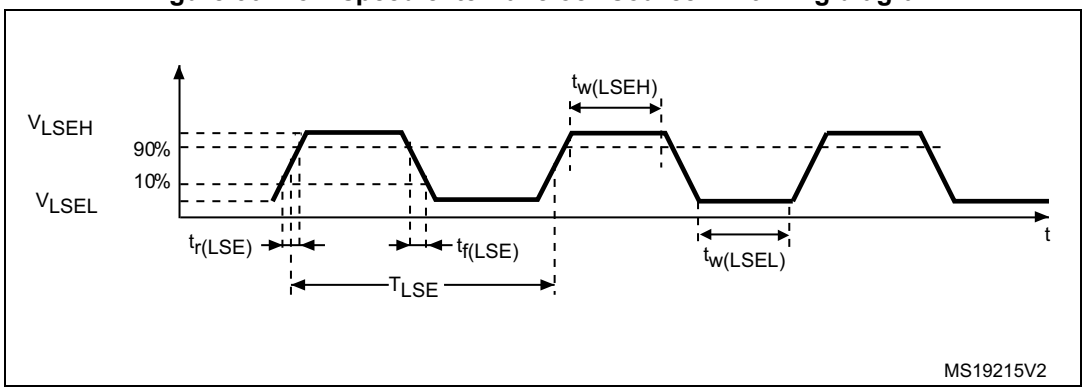


Figure 36. MIPI D-PHY HS/LP clock lane transition timing diagram

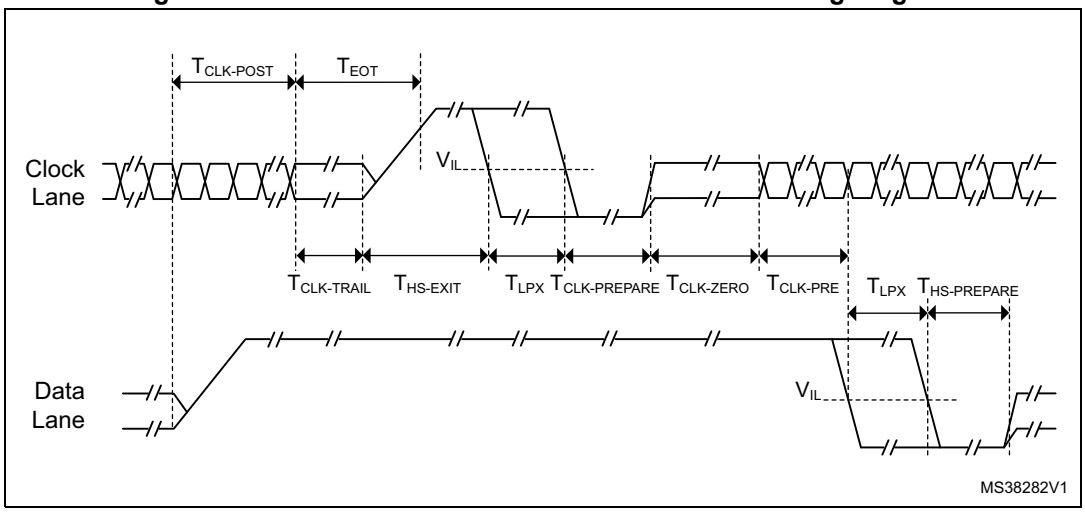
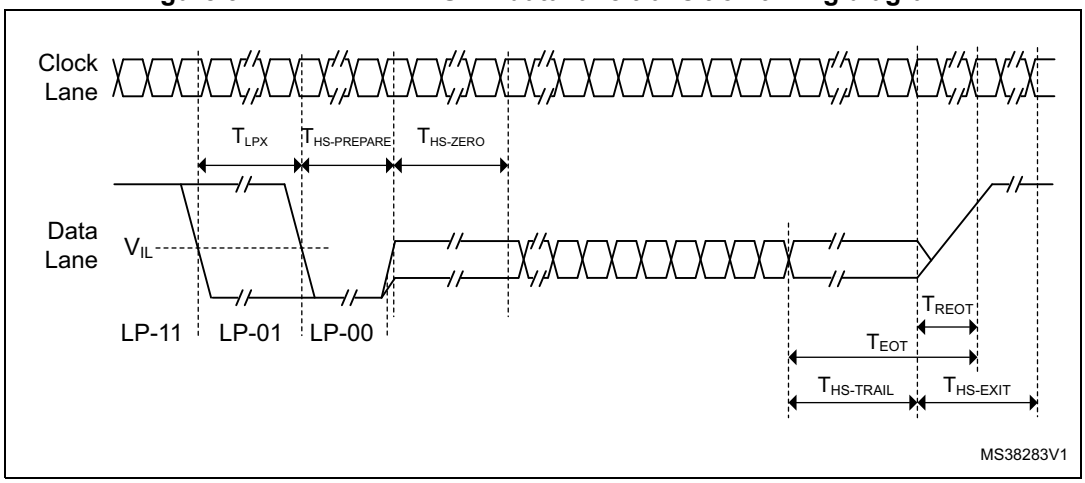


Figure 37. MIPI D-PHY HS/LP data lane transition timing diagram



6.3.11 MIPI D-PHY PLL characteristics

The parameters given in *Table 67* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 67. DSI-PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	4	-	100	MHz
f_{PLL_INFIN}	PFD input clock	-	4	-	25	
f_{PLL_OUT}	PLL multiplier output clock	-	31.25	-	500	
f_{VCO_OUT}	PLL VCO output	-	500	-	1000	
t_{LOCK}	PLL lock time	-	-	-	200	µs

Table 75. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on all pins except PA4, PA5, PB0, PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0, OPAMP1_V1NM, OPAMP2_V1NM	-5	NA	mA
	Injected current on pins PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0	0	NA	
	Injected current on pins OPAMP1_V1NM, OPAMP2_V1NM	0	0	
	Injected current on PA4, PA5, PB0 pins	-5	0	

1. Guaranteed by characterization.

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 76* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 76. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.3xV_{DDIOx}$(2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.39xV_{DDIOx}$-0.06(3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	$0.43xV_{DDIOx}$-0.1(3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.17xV_{DDIOx}$(3)	

The maximum value of R_{AIN} can be found in *Table 83: Maximum ADC RAIN*.

Table 83. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

Table 86. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 92. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

6.3.28 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 96* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINy, DFSDM1_DATINy, DFSDM1_CKOUT for DFSDM).

Table 96. DFSDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 01)	-	-	20	
f_{CKOUT}	Output clock frequency	-	-	-	20	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	-	45	50	55	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2$-0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1.5	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	0	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	(CKOUT DIV+1) x $T_{DFSDMCLK}$	-	(2 x CKOUTDIV) x $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.

conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

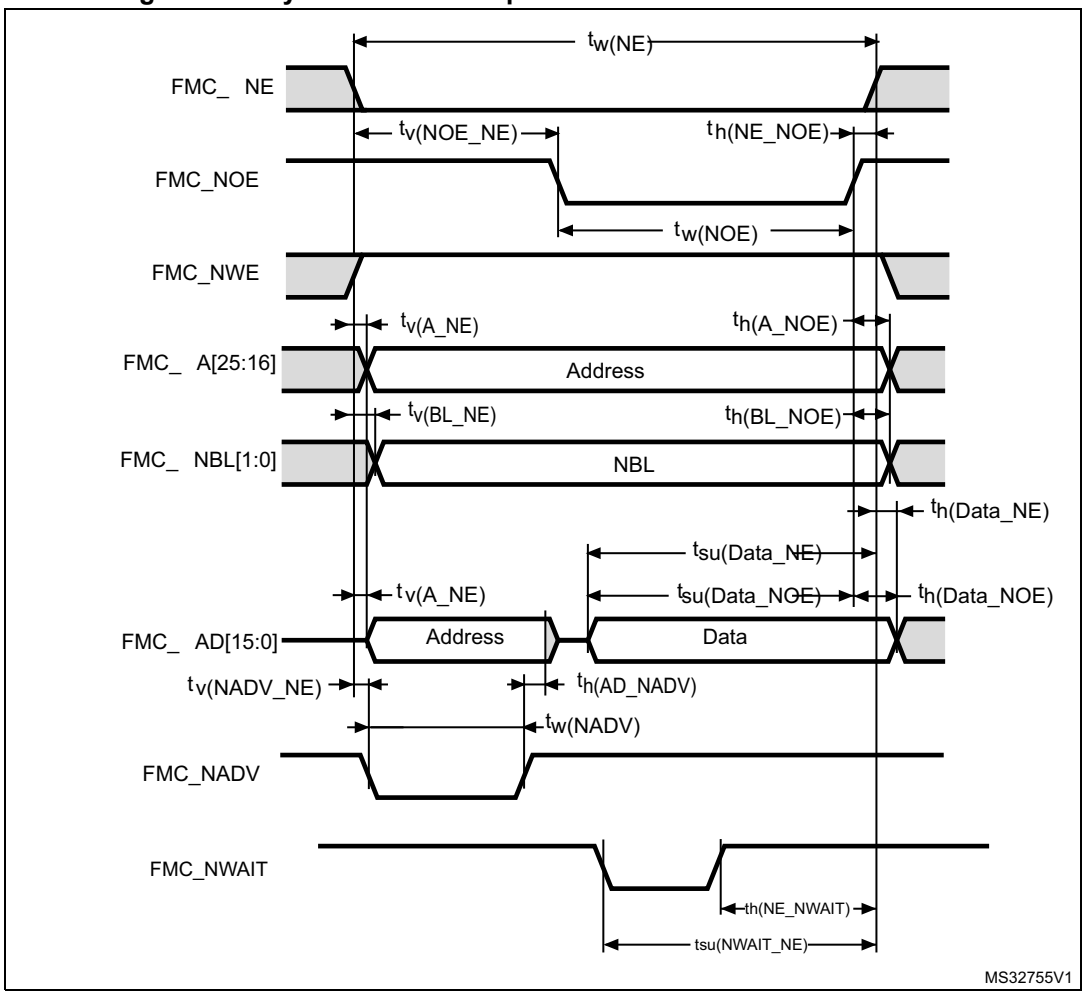
Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 109. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$-0.5	$9T_{HCLK}$+1.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}$-0.5	$6T_{HCLK}$+1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7T_{HCLK}$-13	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5T_{HCLK}$+13	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms



6.3.33 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 123* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 21*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Figure 68. DCMI timing diagram

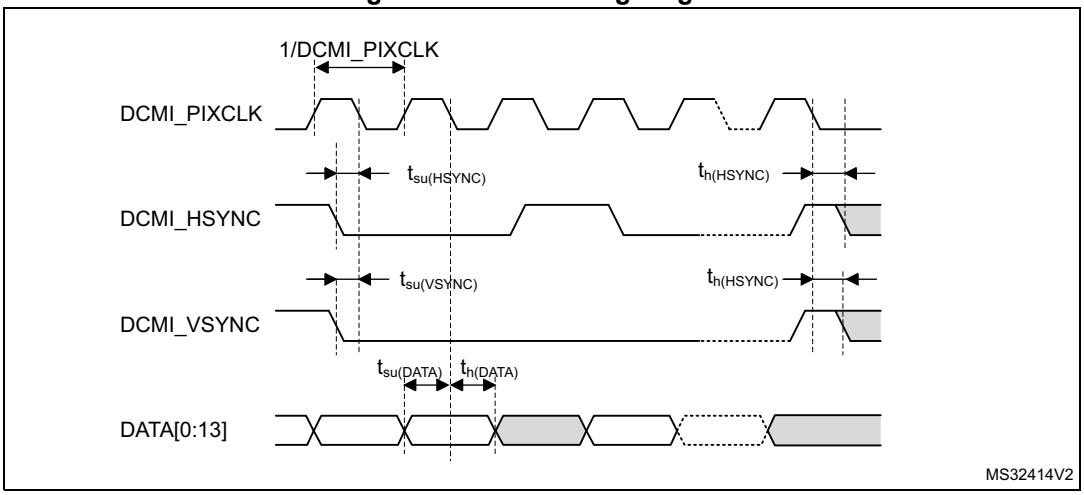
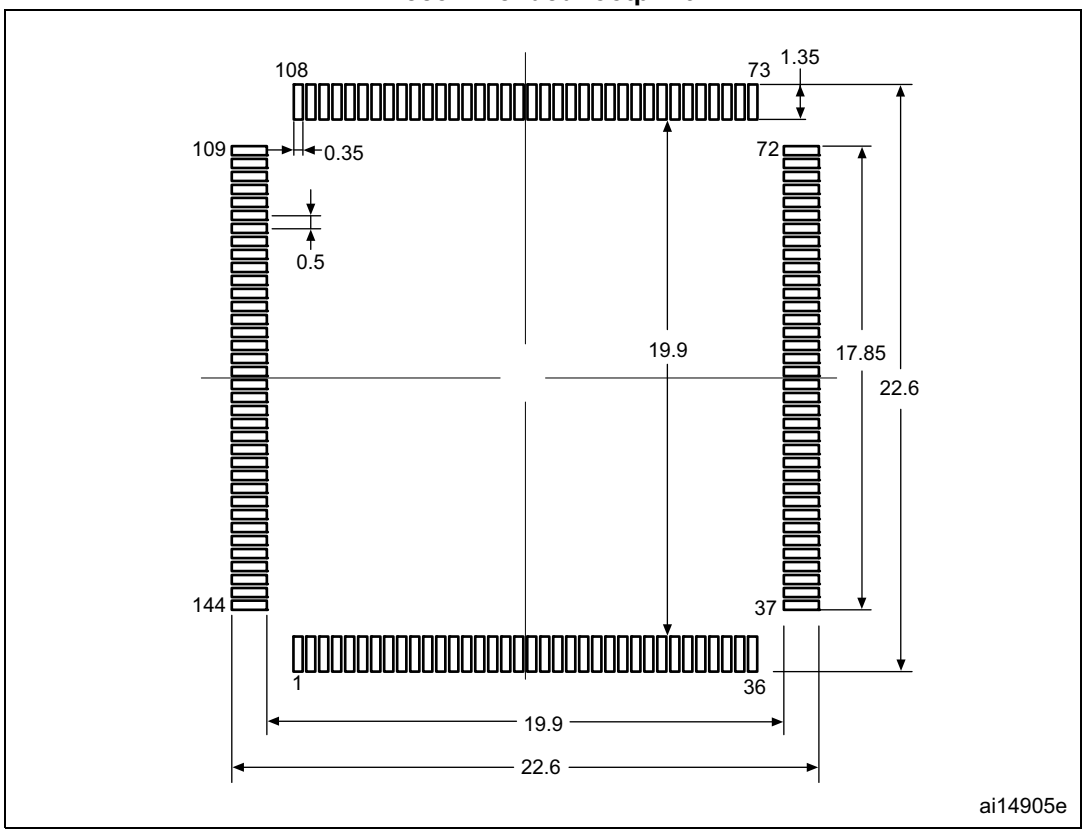


Table 123. DCMI characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	1.71 < VDD < 3.6 Voltage range V1	-	48	MHz
		1.71 < VDD < 3.6 Voltage range V2	-	10	
D_{pixel}	Pixel clock input duty cycle	-	30	70	%

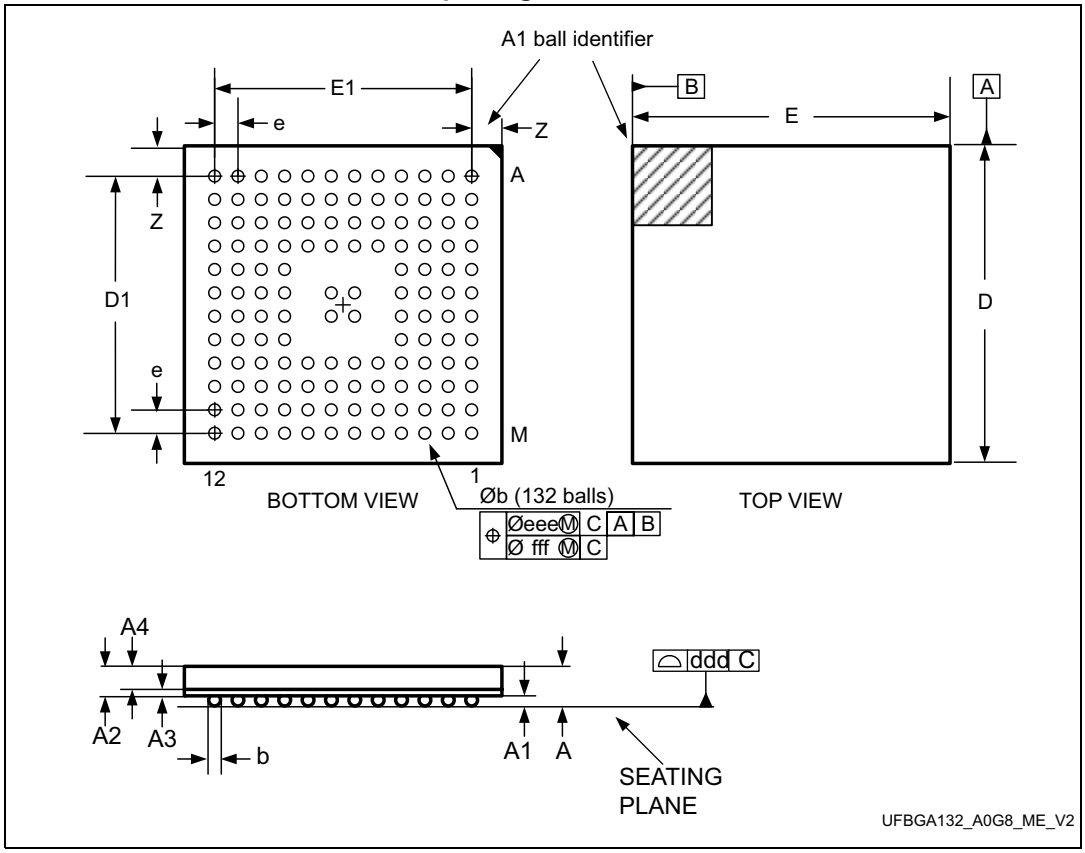
Figure 79. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.5 UFBGA132 package information

Figure 85. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline

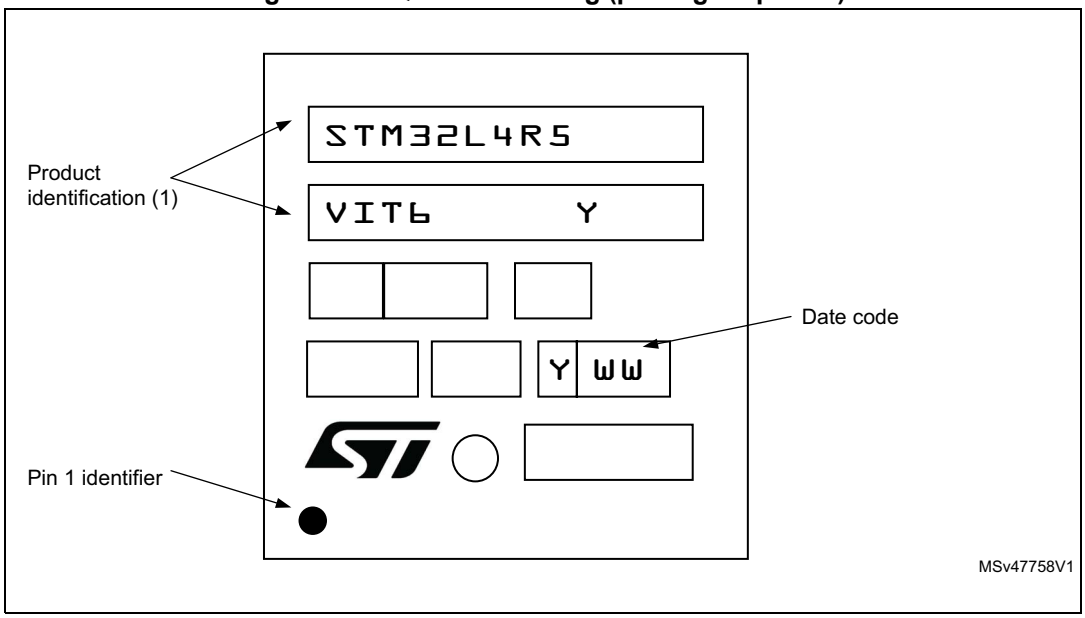


1. Drawing is not to scale.

Table 134. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-

Figure 90. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.