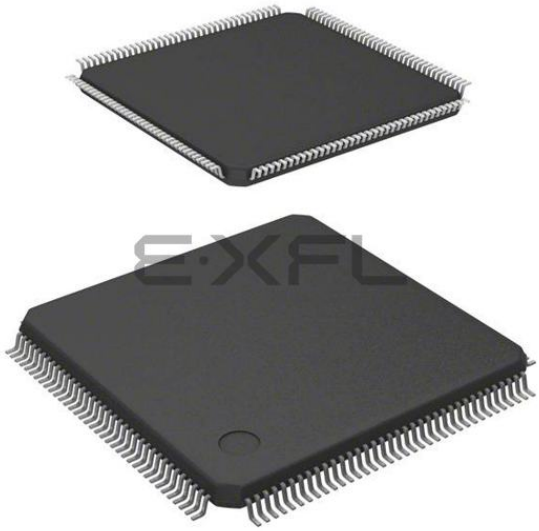


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	115
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5zgt6

3.10.4 Low-power modes

The ultra-low-power STM32L4Rxxx devices support seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wake-up sources. *Table 4* shows the related STM32L4Rxxx modes overview.

Table 4. STM32L4R5xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Run	Range 1 SMPM rage 2 High Range 2 SMPS range 2 Low	Yes	ON[3]	ON	Any	All All except OTG_FS, RNG, LCD-TFT	N/A
LPRun	LPR	Yes	ON[3]	ON	Any except PLL	All except OTG_FS, RNG, LCD-TFT	N/A
Sleep	Range 1 SMPM rage 2 High Range 2 SMPS range 2 Low	No	ON[3]	ON[4]	Any	All All except OTG_FS, RNG, LCD-TFT	Any interrupt or event
LPSleep	LPR	No	ON[3]	ON[4]	Any except PLL	All except OTG_FS, RNG, LCD-TFT	Any interrupt or event

Table 5. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3
Camera interface	O	O	O	O	-	-	-	-	-	-	-	-	-
LCD-TFT	O	O	-	-	-	-	-	-	-	-	-	-	-
GFXMMU	O	O	O	O	-	-	-	-	-	-	-	-	-
DSIHOST	O	O	-	-	-	-	-	-	-	-	-	-	-
USB OTG FS	O[8]	O[8]	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3,4,5)	O	O	O	O	O[6]	O[6]	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O[6]	O[6]	O[6]	O[6]	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O[7]	O[7]	-	-	-	-	-	-	-
I2C3	O	O	O	O	O[7]	O[7]	O[7]	O[7]	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN(x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADC	O	O	O	O	-	-	-	-	-	-	-	-	-
DACx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Gray cells highlight the wakeup capability in each mode.

2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off. In Stop 2 mode, the content of SRAM3 is preserved or not depending on the RRSTP bit in PWR_CR1 register.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.10.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN0	USART3_RTS_DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS_NSS
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	DFSDM1_DATIN5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	DFSDM1_CKIN5	USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	DFSDM1_CKOUT	DFSDM1_DATIN6	-
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	DFSDM1_CKIN6	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	DFSDM1_DATIN7	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C2_SMBA	SPI2_NSS	DFSDM1_DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS_NSS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS_DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	DFSDM1_DATIN4	-
	PC1	TRACED0	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-	DFSDM1_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_CKOUT	-
	PC3	-	LPTIM1_ETR	-	SAI1_D1	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	SAI1_D3	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	TRACED0	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	DCMI_D3	-	I2C3_SDA	-
	PC10	TRACED1	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	DCMI_D2	OCTOSPIM_P1_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
AHB1	0x4002 F000 - 0x47FF FFFF	~127 MB	Reserved
	0x4002 C000 - 0x4002 EFFF	1KB	GFXMMU
	0x4002 BC00 - 0x4002 BBFF	1 KB	Reserved
	0x4002 B000 - 0x4002 BBFF	3 KB	DMA2D
	0x4002 4400 - 0x4002 AFFF	26 KB	Reserved
	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0800 - 0x4002 0BFF	1 KB	DMAMUX1
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
APB2	0x4001 7400 - 0x4001 FFFF	33 KB	Reserved
	0x4001 6C00 - 0x4001 73FF	1 KB	DSIHOST
	0x4001 6800 - 0x4001 6BFF	1 KB	LCD-TFT
	0x4001 6000 - 0x4001 67FF	2 KB	DFSDM1
	0x4001 5C00 - 0x4001 5FFF	1 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	SAI2
	0x4001 5400 - 0x4001 57FF	1 KB	SAI1
	0x4001 4C00 - 0x4001 53FF	2 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2000 - 0x4001 2BFF	3 KB	Reserved

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.60	3.95	5.05	6.65	9.55	4.2	5.0	7.1	11.0	17.0	mA
				16 MHz	2.30	2.65	3.75	5.35	8.20	2.7	3.6	5.6	8.9	15.0	
				8 MHz	1.30	1.65	2.70	4.30	7.15	1.6	2.4	4.4	7.7	14.0	
				4 MHz	0.770	1.10	2.20	3.75	6.60	1.0	1.8	3.8	7.1	14.0	
				2 MHz	0.515	0.865	1.95	3.50	6.35	0.7	1.5	3.5	6.8	13.0	
				1 MHz	0.380	0.735	1.80	3.35	6.20	0.6	1.4	3.4	6.7	13.0	
				100 KHz	0.265	0.620	1.70	3.25	6.10	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	17.0	18.0	19.5	21.5	25.5	19.0	21.0	24.0	28.0	36.0	
			Range 1 Normal Mode	80 MHz	12.5	13.0	14.0	16.0	19.5	14.0	15.0	18.0	22.0	29.0	
				72 MHz	11.0	11.5	13.0	15.0	18.5	13.0	14.0	17.0	21.0	28.0	
				64 MHz	9.90	10.5	12.0	14.0	17.5	12.0	13.0	15.0	19.0	26.0	
				48 MHz	7.85	8.30	9.75	11.5	15.0	8.7	9.9	13.0	17.0	24.0	
				32 MHz	5.35	5.80	7.20	9.20	12.5	6.1	7.1	9.6	14.0	21.0	
				24 MHz	4.10	4.55	5.95	7.90	11.5	4.7	5.7	8.2	13.0	20.0	
				16 MHz	2.80	3.30	4.65	6.60	10.0	3.3	4.3	6.8	11.0	18.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	460	905	2150	3950	7100	660	1700	4100	7700	15000	µA
				1 MHz	355	760	2000	3800	6950	540	1500	3900	7600	14000	
				400 KHz	240	685	1950	3700	6850	410	1400	3800	7500	14000	
				100 KHz	200	635	1900	3650	6800	370	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 31. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable and power supplied by external SMPS

Symbol	Parameter	Conditions(1)			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	7.4	7.8	8.4	9.4	10.8	mA
			VDD12=1.10V	80 MHz	4.7	4.9	5.6	6.3	7.5	
				72 MHz	4.3	4.5	5.0	5.8	7.2	
				64 MHz	3.8	4.0	4.5	5.4	6.7	
				48 MHz	3.1	3.3	4.0	4.7	5.9	
				32 MHz	2.2	2.4	2.9	3.6	5.0	
				26 MHz	1.7	1.9	2.4	3.1	4.3	
				16 MHz	1.1	1.3	1.8	2.5	3.8	
				8 MHz	0.6	0.8	1.3	1.9	3.1	
				4 MHz	0.4	0.5	1.0	1.7	3.0	
				2 MHz	0.2	0.4	0.9	1.6	2.8	
				1 MHz	0.2	0.3	0.8	1.5	2.8	
				100 KHz	0.1	0.3	0.8	1.4	2.7	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

Table 38. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	4.00	4.10	mA	154	158	µA/MHz
				Coremark	4.15	3.80		160	146	
				Dhrystone2.1	4.40	4.00		169	154	
				Fibonacci	3.80	3.60		146	138	
				While(1)	3.15	3.15		121.2	121.2	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	13.0	13.0	mA	163	163	µA/MHz
				Coremark	13.0	12.0		163	150	
				Dhrystone2.1	14.0	12.5		175	156	
				Fibonacci	11.5	11.0		144	138	
				While(1)	10.5	10.5		131	131	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.5	17.0	mA	154	142	µA/MHz
				Coremark	18.0	16.0		150	133	
				Dhrystone2.1	19.0	16.5		158	138	
				Fibonacci	16.0	15.0		133	125	
				While(1)	16.5	16.5		138	138	
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	595	590	µA	298	295	µA/MHz
				Coremark	620	580		310	290	
				Dhrystone2.1	645	655		323	328	
				Fibonacci	670	580		335	290	
				While(1)	470	685		235	343	

1. Reduced code used for characterization results provided in *Table 26*, *Table 30*, *Table 34*.

Table 43. Current consumption in Sleep and Low-power sleep modes, Flash ON and power supplied by external SMPS

Symbol	Parameter	Conditions(1)			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	1.68	1.89	2.51	3.37	4.81	mA
			VDD12=1.10V	80 MHz	1.01	1.17	1.67	2.37	3.59	
				72 MHz	0.92	1.08	1.58	2.30	3.54	
				64 MHz	0.83	0.99	1.51	2.21	3.45	
				48 MHz	0.77	0.93	1.44	2.16	3.40	
				32 MHz	0.56	0.72	1.22	1.92	3.16	
				26 MHz	0.47	0.63	1.10	1.79	3.02	
				16 MHz	0.33	0.50	0.97	1.64	2.87	
				8 MHz	0.22	0.38	0.84	1.53	2.74	
				4 MHz	0.16	0.32	0.80	1.47	2.70	
				2 MHz	0.14	0.27	0.75	1.45	2.65	
				1 MHz	0.12	0.26	0.75	1.42	2.63	
				100 KHz	0.11	0.25	0.73	1.40	2.63	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

Table 46. Current consumption in Stop 2 mode, SRAM3 enabled

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	3.90	15.0	59.5	140	310	13.0	52.0	210	480	1100	µA
			2.4 V	3.95	15.0	60.0	140	310	14.0	53.0	210	480	1100	
			3 V	3.95	15.0	60.5	145	315	14.0	53.0	210	480	1100	
			3.6 V	3.95	15.0	61.5	145	320	14.0	54.0	210	490	1100	
IDD(Stop 2 with RTC)	Supply current in STOP 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	4.10	15.0	60.5	140	310	11.0	53.0	210	480	1100	
			2.4 V	4.25	15.5	60.5	145	315	12.0	54.0	210	480	1100	
			3 V	4.50	15.5	61.5	145	320	12.0	54.0	210	480	1100	
			3.6 V	4.70	16.0	62.5	145	325	12.0	56.0	220	490	1100(2)	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	4.35	15.5	61.0	140	310	9.50	39.0	160	350	780	
			2.4 V	4.50	15.5	61.0	145	315	9.60	39.0	160	370	790	
			3 V	4.70	16.0	62.0	145	320	9.90	40.0	160	370	800	
			3.6 V	4.80	16.5	63.0	145	325	10.0	42.0	160	370	820	
		RTC clocked by LSE quartz in low drive mode	1.8 V	4.30	15.5	63.5	150	-	9.40	39.0	160	380	-	
			2.4 V	4.40	16.0	64.0	150	-	9.50	40.0	160	380	-	
			3 V	4.45	16.0	64.5	150	-	9.60	40.0	170	380	-	
			3.6 V	4.85	16.5	65.5	155	-	11.0	42.0	170	390	-	
IDD(wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(3)	3 V	3.80	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(3)	3 V	1.30	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(3)	3 V	2.95	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 71*. They are based on the EMS levels and classes defined in application note AN1709.

Table 71. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 120 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 120 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 75. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on all pins except PA4, PA5, PB0, PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0, OPAMP1_V1NM, OPAMP2_V1NM	-5	NA	mA
	Injected current on pins PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0	0	NA	
	Injected current on pins OPAMP1_V1NM, OPAMP2_V1NM	0	0	
	Injected current on PA4, PA5, PB0 pins	-5	0	

1. Guaranteed by characterization.

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 76* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 76. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.3xV_{DDIOx}$(2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.39xV_{DDIOx}$-0.06(3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	$0.43xV_{DDIOx}$-0.1(3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.17xV_{DDIOx}$(3)	

Figure 54. Synchronous multiplexed NOR/PSRAM read timings

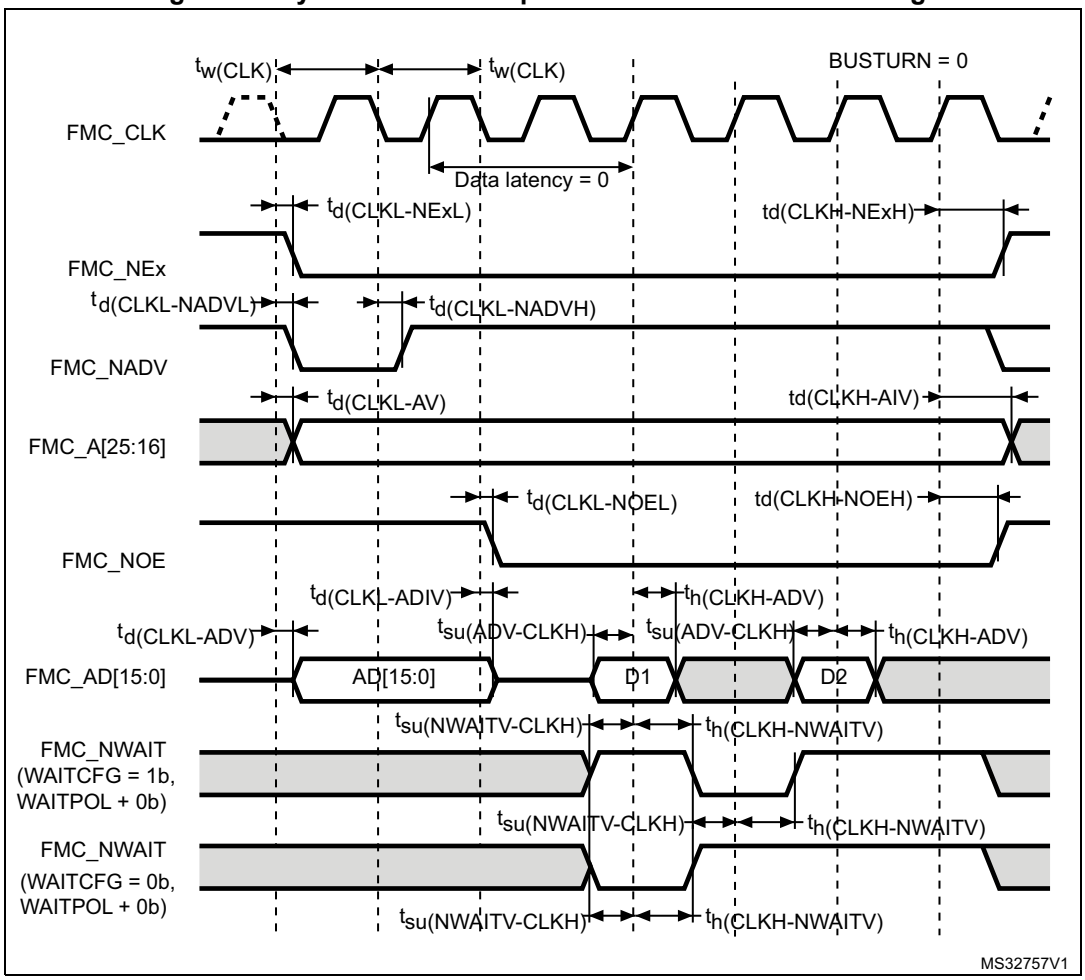


Figure 55. Synchronous multiplexed PSRAM write timings

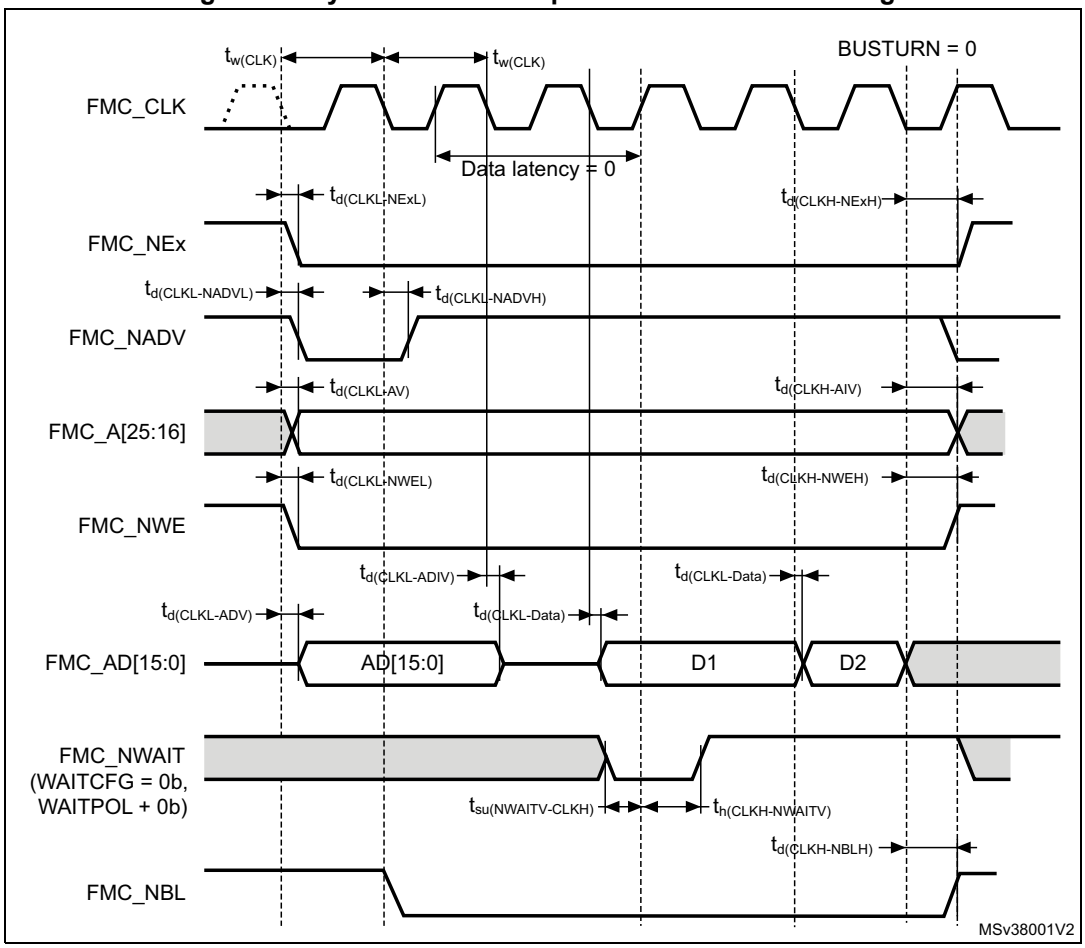


Figure 58. NAND controller waveforms for read access

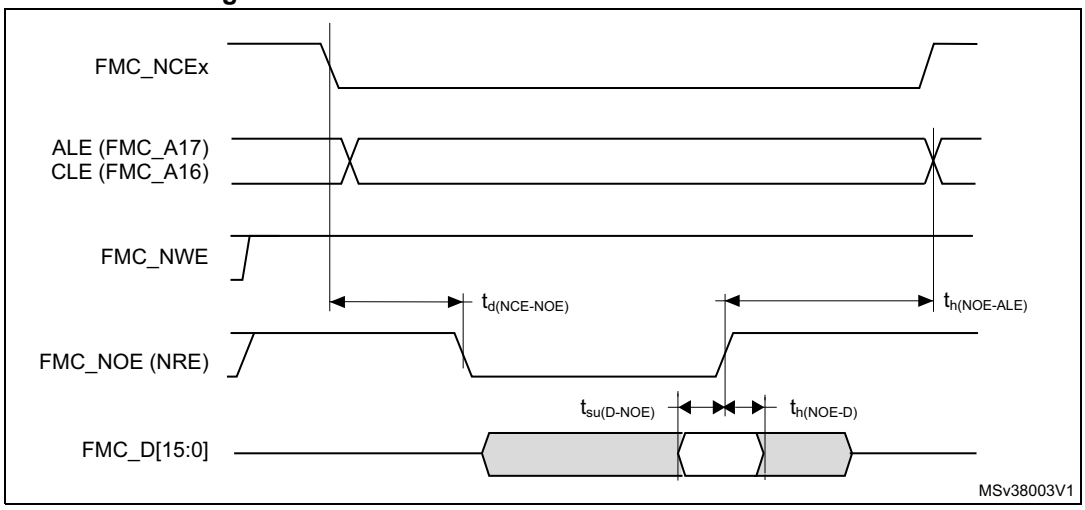


Figure 59. NAND controller waveforms for write access

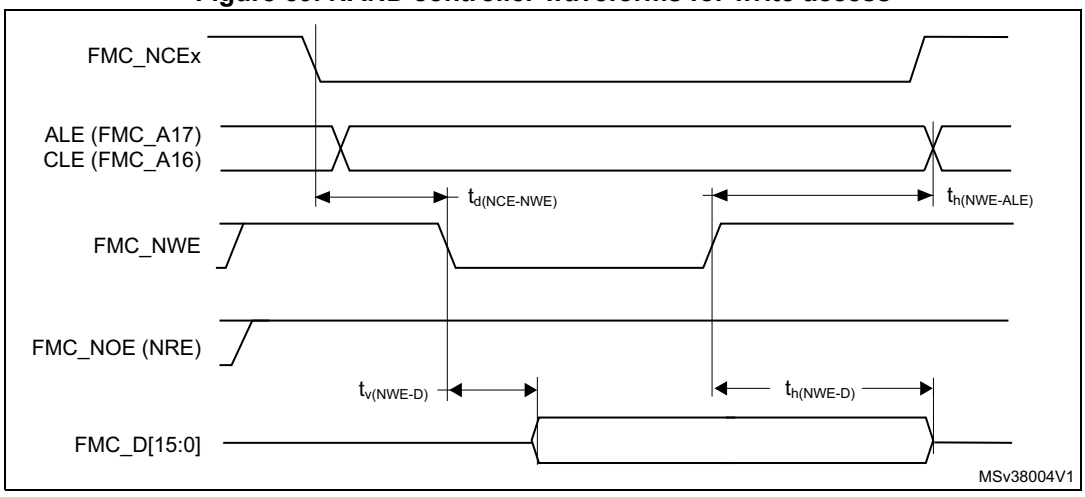


Figure 60. NAND controller waveforms for common memory read access

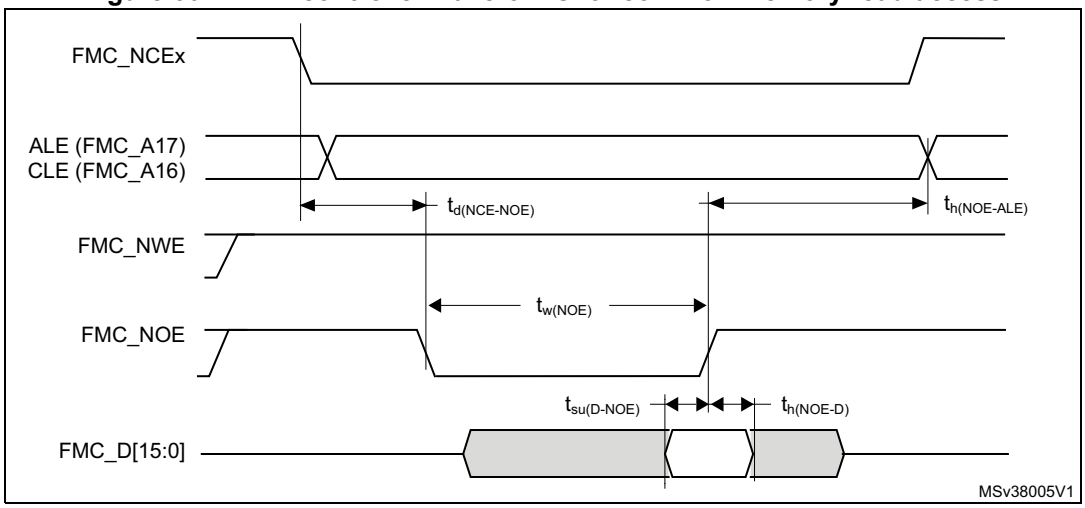


Figure 61. NAND controller waveforms for common memory write access

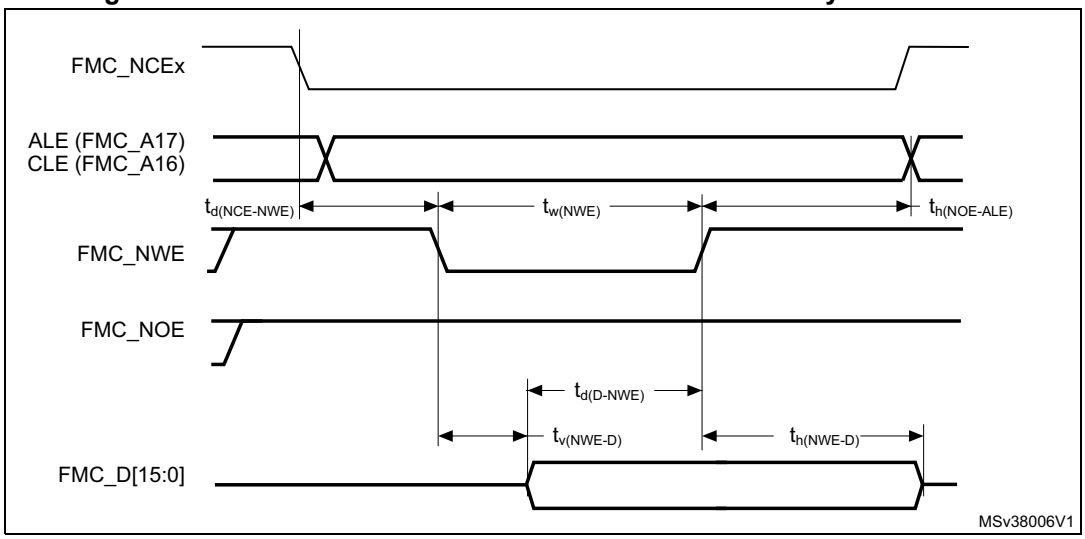


Table 118. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	14	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 119. Switching characteristics for NAND Flash write cycles(1)(2)

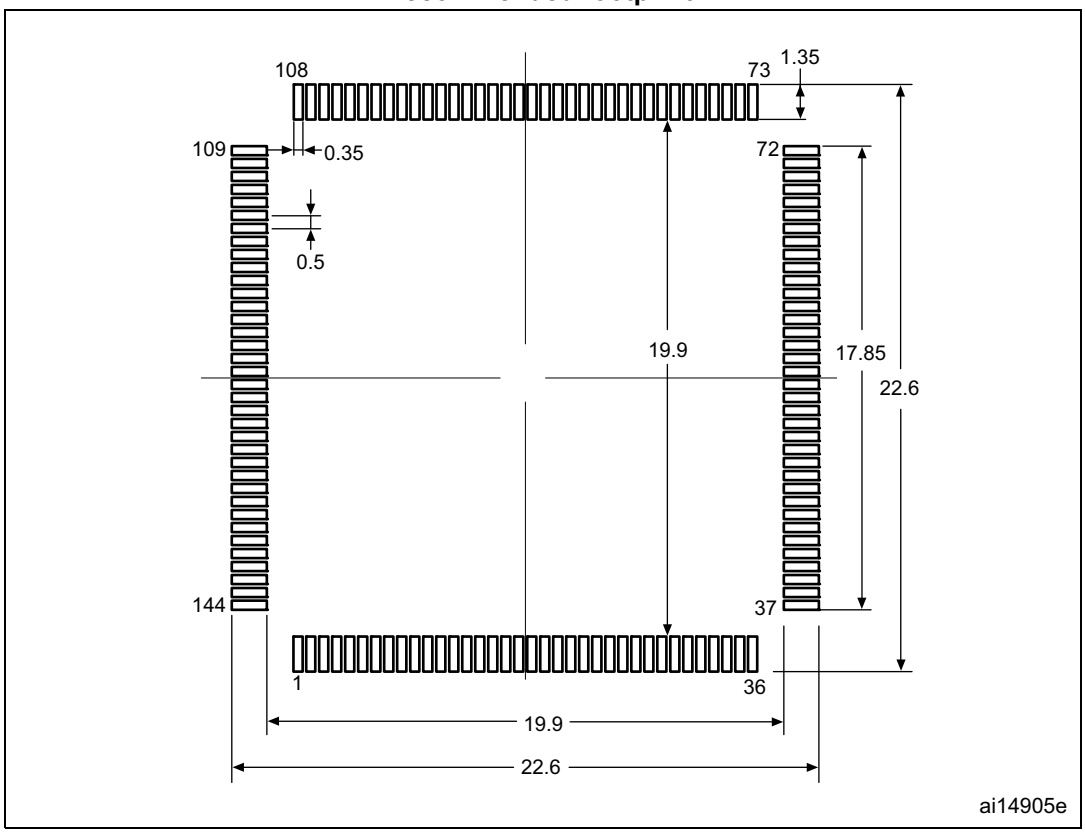
Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$2T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$-1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.32 OctoSPI characteristics

Unless otherwise specified, the parameters given in *Table 120*, *Table 121* and *Table 122* for OctoSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency

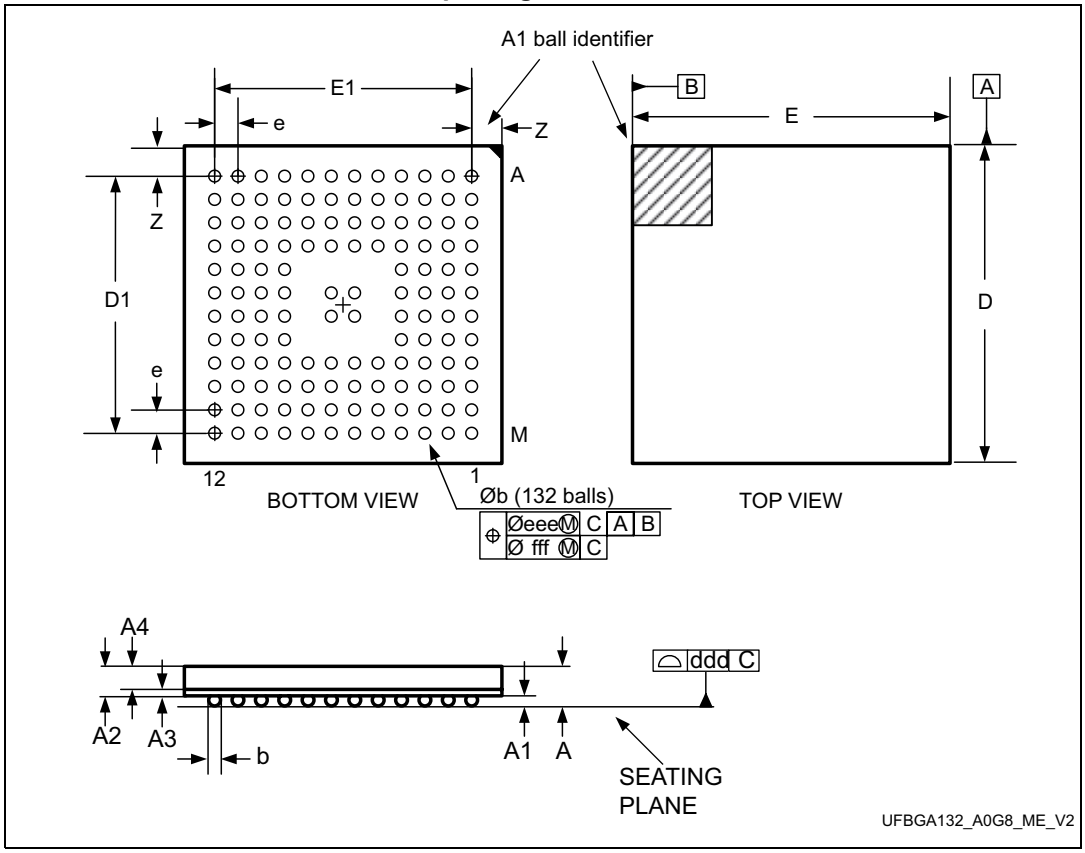
Figure 79. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.5 UFBGA132 package information

Figure 85. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 134. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-