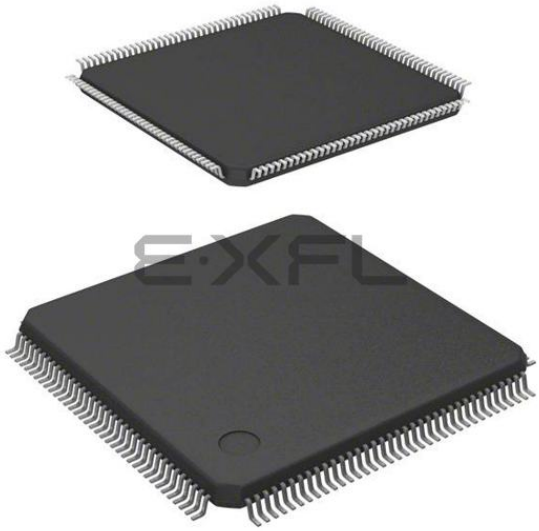

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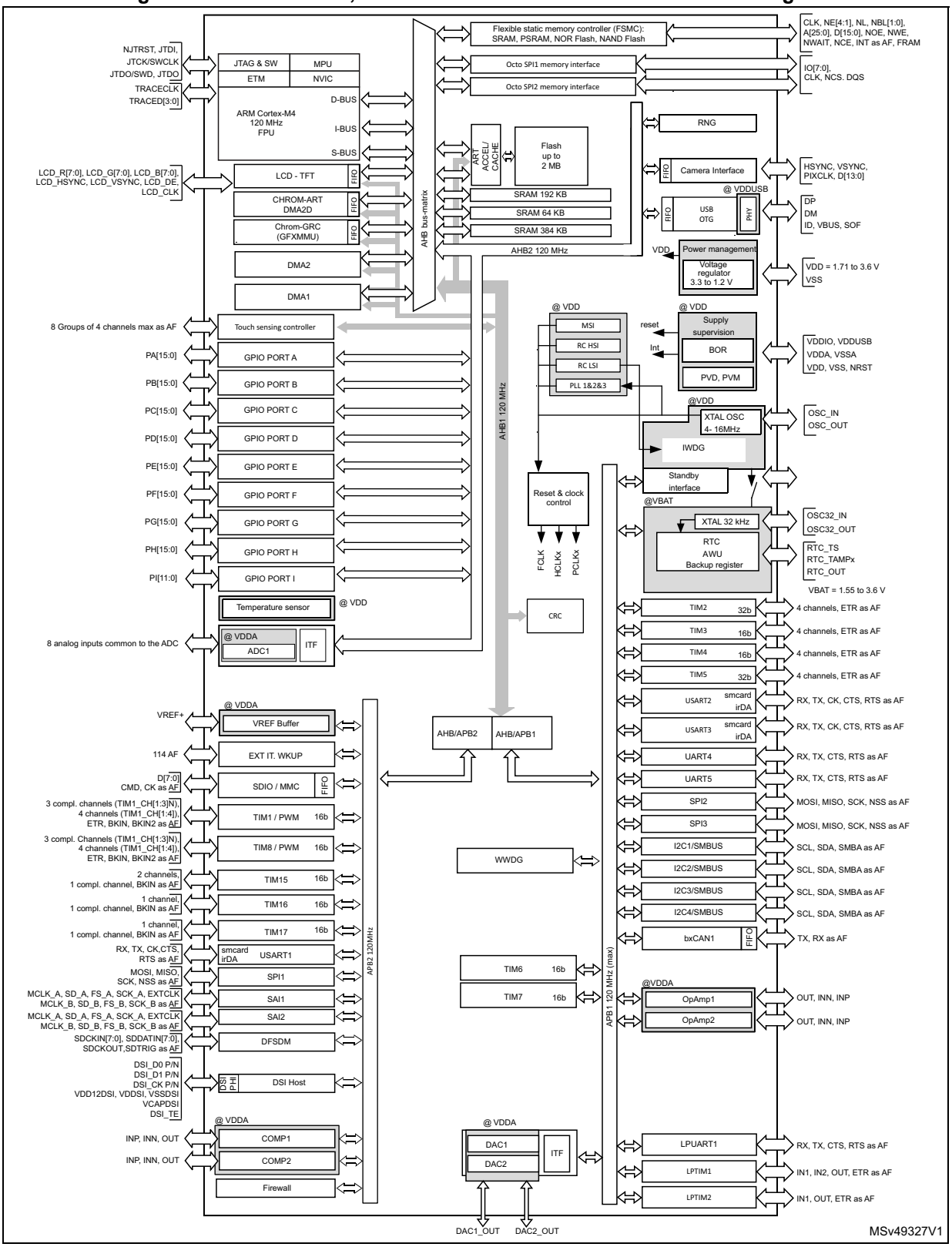
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

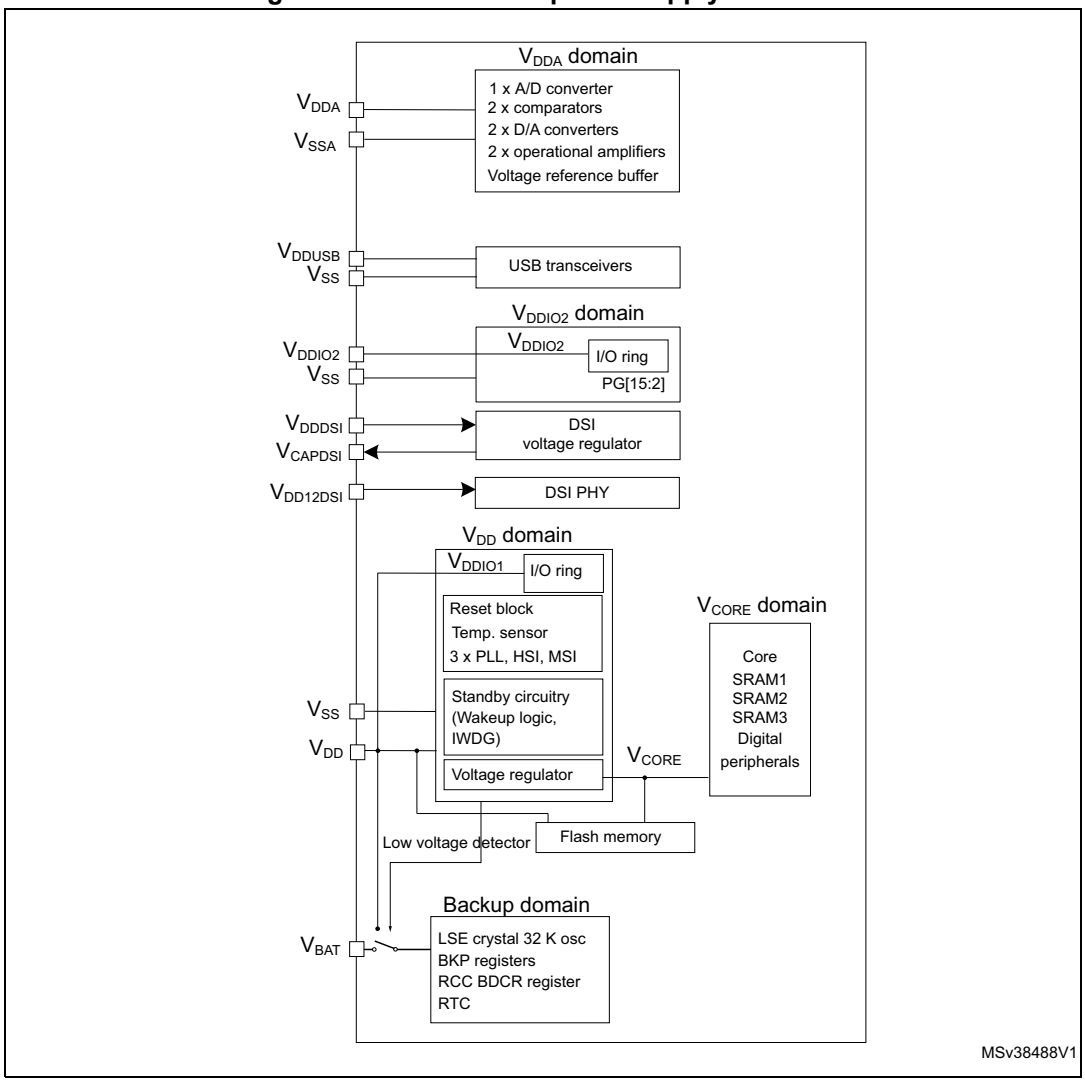
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	115
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5zit6

Figure 1. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx block diagram



Note: AF: alternate function on I/O pins.

Figure 5. STM32L4R9xx power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}) must remain below VDD +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Hyperbus™ support
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.43 OctoSPI IO manager (OctoSPIIOM)

The OctoSPI IO Manager is a low level interface allowing:

- Efficient OctoSPI pin assignment with a full IO Matrix (before alternate function map)
- Multiplexing single/dual/quad/octal SPI interface over the same bus

The OctoSPI IO Manager has the following features:

- Support up to two single/dual/quad/octal SPI Interface
- Support up to eight ports for pin assignment
- Fully programmable IO matrix for pin assignment by function (data/control/clock)
- Muxer for Single/Dual/Quad/Octal SPI interface multiplexing over the same bus

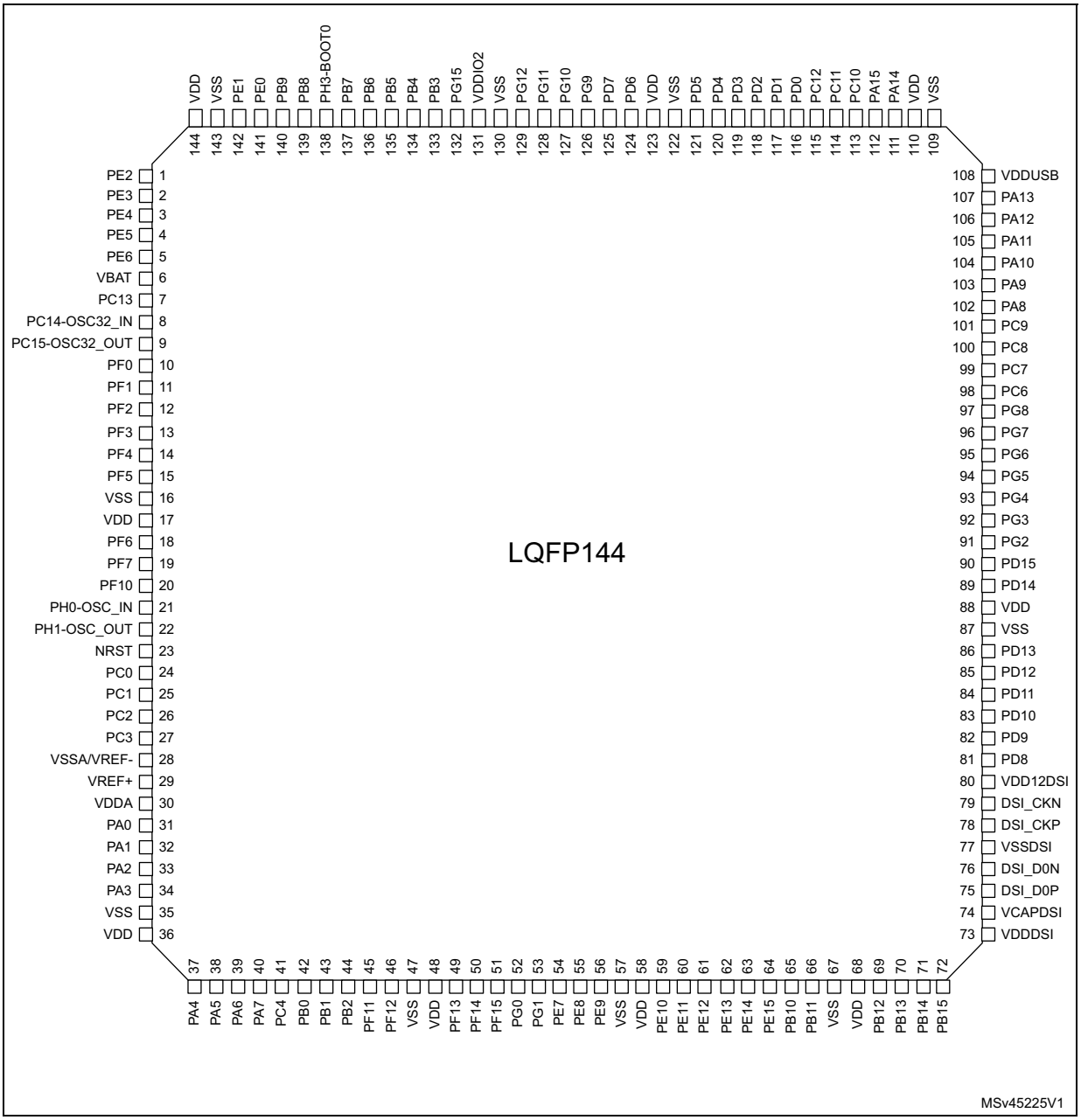
3.44 Development support

3.44.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins could be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 13. STM32L4R9xx LQFP144 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
52	K12	K12	74	74	H4	N13	N13	49	70	M11	H4	H4	N13	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, DFSDM1_CKIN1, USART3_CTS_NSS, LPUART1_CTS, TSC_G1_IO2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
53	K11	K11	75	75	H3	M13	M13	50	71	K10	H3	H3	M12	PB14	I/O	FT_fl	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS_DE, TSC_G1_IO3, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPIM_P1_DQS	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-	DFSDM1_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-	DFSDM1_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM1_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM1_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM1_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM1_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN	-	SPI1_MOSI	-	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port I	PI0	-	-	DCMI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	EVENTOUT

1. Refer to *Table 16* for AF0 to AF7.

Table 29. Consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS

Symbol	Parameter	Conditions(1)			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	6.82	7.22	7.82	8.62	10.23	mA
			VDD12=1.10V	80 MHz	4.49	4.67	5.03	5.75	7.01	
				72 MHz	3.95	4.13	4.67	5.39	6.65	
				64 MHz	3.56	3.77	4.31	5.03	6.29	
				48 MHz	2.82	2.98	3.50	4.13	5.39	
				32 MHz	1.92	2.08	2.59	3.31	4.49	
				26 MHz	1.55	1.70	2.18	2.87	4.12	
				16 MHz	0.99	1.14	1.62	2.31	3.54	
				8 MHz	0.56	0.71	1.16	1.85	3.08	
				4 MHz	0.33	0.47	0.95	1.62	2.85	
				2 MHz	0.22	0.37	0.84	1.51	2.74	
				1 MHz	0.16	0.32	0.78	1.45	2.67	
				100 KHz	0.11	0.27	0.73	1.40	2.63	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

Table 39. Typical current consumption in Run and Low-power run modes with different codes running from Flash, ART disable and power supplied by external SMPS

Symbol	Parameter	Conditions[1]				TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	VDD12	f_{HCLK}	Code	25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12= 1.05V	f_{HCLK}= 26 MHz	Reduced code	1.57	1.61	mA	60	62	µA/MHz
					Coremark	1.63	1.49		63	57	
					Dhrystone2.1	1.73	1.57		67	60	
					Fibonacci	1.49	1.41		57	54	
					While(1)	1.24	1.24		48	48	
			VDD12= 1.10V	f_{HCLK}= 26 MHz	Reduced code	1.73	1.77	mA	66	68	µA/MHz
					Coremark	1.79	1.64		69	63	
					Dhrystone2.1	1.90	1.73		73	66	
					Fibonacci	1.64	1.55		63	60	
					While(1)	1.36	1.36		52	52	
				f_{HCLK}= 80 MHz	Reduced code	4.67	4.67	mA	58	58	µA/MHz
					Coremark	4.67	4.31		58	54	
					Dhrystone2.1	5.03	4.49		63	56	
					Fibonacci	4.13	3.95		52	49	
					While(1)	3.77	3.77		47	47	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12= 1.20V	f_{HCLK}= 120 MHz	Reduced code	7.4	6.8	mA	62	57	µA/MHz
					Coremark	7.2	6.4		60	53	
					Dhrystone 2.1	7.6	6.6		64	55	
					Fibonacci	6.4	6.0		53	50	
					While(1)	6.6	6.6		55	55	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.10 V.

Table 44. Current consumption in Low-power sleep mode, Flash in power-down

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (LPSleep)	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	255	645	1950	3700	6850	430	1400	3700	7400	14000	µA
				1 MHz	195	620	1900	3700	6850	370	1300	3700	7400	14000	
				400 KHz	180	600	1900	3700	6800	350	1300	3700	7400	14000	
				100 KHz	175	595	1900	3650	6800	340	1300	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 52. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	I2C1 APB clock domain	1.4	1.4	1.25	2	µA/MHz
	I2C2 independent clock domain	3.5	3.4	2.5	3.5	
	I2C2 APB clock domain	1.4	1.25	1.25	1	
	I2C3 independent clock domain	3.25	3.15	2.9	3	
	I2C3 APB clock domain	1.15	1	0.835	1	
	I2C4 independent clock domain	3.5	3.25	2.75	3	
	I2C4 APB clock domain	1.35	1.25	1	1.5	
	LPUART1 independent clock domain	3.15	3	2.45	3	
	LPUART1 APB clock domain	1.65	1.5	1.3	1.5	
	LPTIM1 independent clock domain	3.6	3.5	2.9	3	
	LPTIM1 APB clock domain	1	0.875	0.835	1	
	LPTIM2 independent clock domain	3.4	3.25	2.55	3.5	
	LPTIM2 APB clock domain	1.1	1	0.79	1	
	OPAMP	0.415	0.375	0.415	0.5	
	PWR	0.5	0.375	0.415	0.5	
	RTCAPB	1.25	1.15	1.25	1	
	SPI2	2.6	2.4	2.1	2.5	
	SPI3	3	2.75	2.5	3	
	TIM2	6.15	5.75	4.65	4.5	
	TIM3	5.25	4.9	4.15	5	
	TIM4	5.15	4.75	4.15	5	
	TIM5	6.5	6	5	6	
	TIM6	1.35	1.15	1.25	1	
	TIM7	1.25	1.15	0.835	1	

Figure 33. HSI16 frequency versus temperature

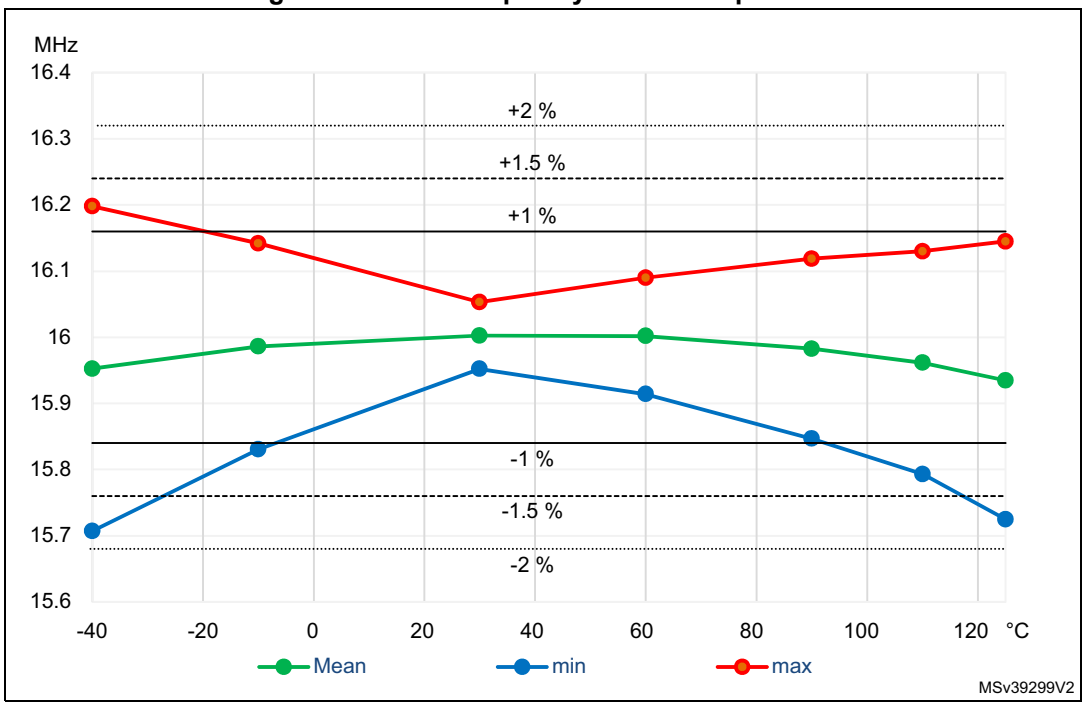


Table 67. DSI-PLL characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLL)}$	PLL power consumption on V_{DD12}	f_{VCO_OUT} = 500 MHz	-	0.55	0.70	mA
		f_{VCO_OUT} = 600 MHz	-	0.65	0.80	
		f_{VCO_OUT} = 1000 MHz	-	0.95	1.20	

1. Guaranteed by characterization results.

6.3.12 MIPI D-PHY regulator characteristics

The parameters given in *Table 68* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 68. DSI regulator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD12DSI}$	1.2 V internal voltage on $V_{DD12DSI}$	-	1.15	1.20	1.30	V
C_{EXT}	External capacitor on V_{CAPDSI}	-	1.1	2.2	3.3	µF
ESR	External Serial Resistor	-	0	25	600	mΩ
$I_{DDDSIREG}$	Regulator power consumption	-	100	120	125	µA
I_{DDDSI}	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI}	Ultra Low Power Mode (Reg. ON + PLL OFF)	-	290	600	µA
		Stop State (Reg. ON + PLL OFF)	-	290	600	
$I_{DDDSILP}$	DSI system current consumption on V_{DDDSI} in LP mode communication(2)	10 MHz escape clock (Reg. ON + PLL OFF)	-	4.3	5.0	mA
		20 MHz escape clock (Reg. ON + PLL OFF)	-	4.3	5.0	
$I_{DDDSIHS}$	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI} in HS mode communication(3)	300 Mbps - 1 data lane (Reg. ON + PLL ON)	-	8.0	8.8	mA
		300 Mbps - 2data lane (Reg. ON + PLL ON)	-	11.4	12.5	
		500 Mbps - 1 data lane (Reg. ON + PLL ON)	-	13.5	14.7	
		500 Mbps - 2data lane (Reg. ON + PLL ON)	-	18.0	19.6	
	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI} in HS mode with CLK like payload	500 Mbps - 2data lane (Reg. ON + PLL ON)	-	21.4	23.3	
t_{WAKEUP}	Startup delay	C_{EXT} = 2.2 µF	-	110	-	µs
		C_{EXT} = 3.3 µF	-	-	160	
I_{INRUSH}	Inrush current on V_{DDDSI}	External capacitor load at start	-	60	200	mA

1. Guaranteed by characterization results.
2. Values based on an average traffic in LP Command Mode.
3. Values based on an average traffic (3/4 HS traffic & 1/4 LP) in Video Mode.

Table 84. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 87. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 49. USB OTG timings – definition of data signal rise and fall time

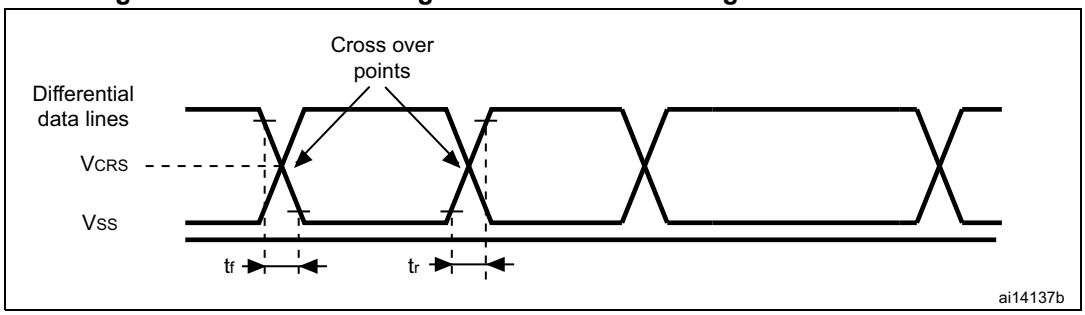


Table 104. USB OTG electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(2)				
t_{rfmLS}	Rise/ fall time matching in LS	t_r / t_f	80	125	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF			
t_{rfmFS}	Rise/ fall time matching in FS	t_r / t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 105. USB BCD DC electrical characteristics(1)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-		
RDAT_LKG	Data line leakage resistance	-	300	-	-	kΩ
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	V

Table 105. USB BCD DC electrical characteristics(1) (continued)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
VLGC	Logic threshold	-	0.8	-	2.0	V
VDAT_REF	Data detect voltage	-	0.25	-	0.4	V
VDP_SRC	D+ source voltage	-	0.5	-	0.7	V
VDM_SRC	D- source voltage	-	0.5	-	0.7	V
IDP_SINK	D+ sink current	-	25	-	175	µA
IDM_SINK	D- sink current	-	25	-	175	µA

1. Guaranteed by design

CAN (controller area network) interface

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.31 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 106* to *Table 119* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 50 through *Figure 53* represent asynchronous waveforms and *Table 106* through *Table 113* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataHoldTime = 0x1
- ByteLaneSetup = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.

Table 117. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK}-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +0.5	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	RxT_{HCLK}/2 +1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

NAND controller waveforms and timings

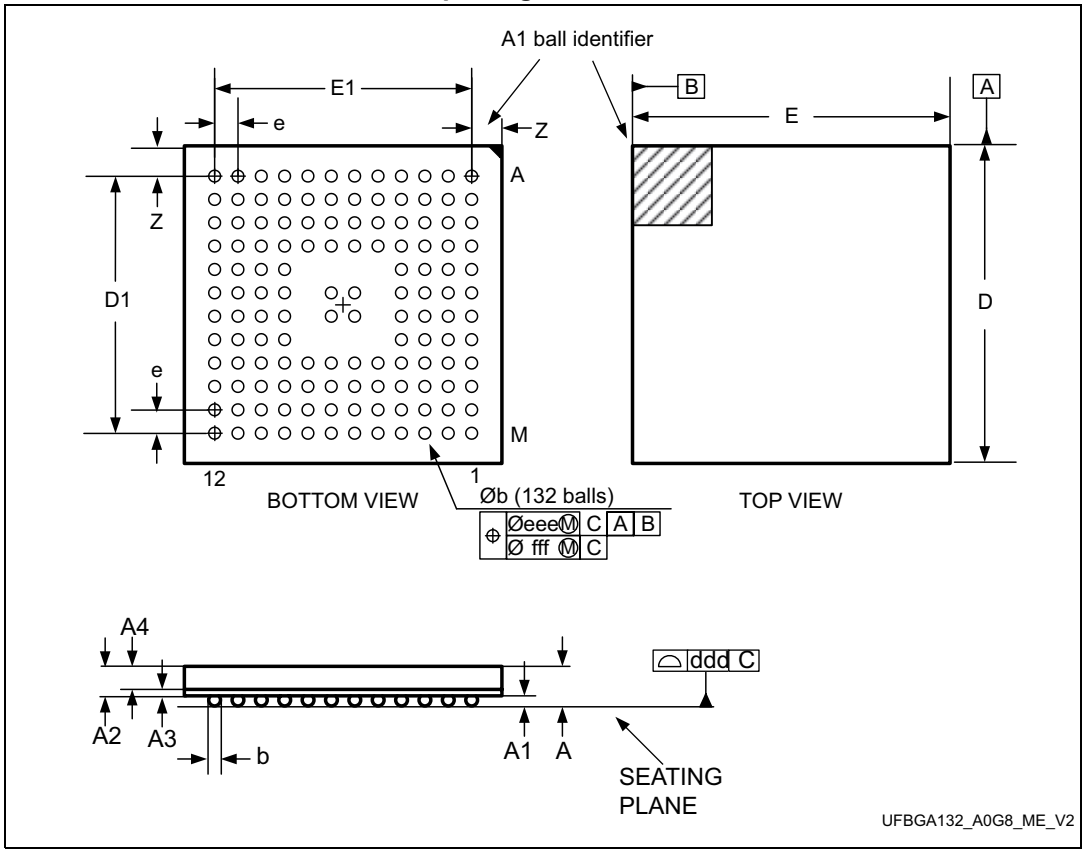
Figure 58 through *Figure 61* represent synchronous waveforms, and *Table 118* and *Table 119* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

7.5 UFBGA132 package information

Figure 85. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 134. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-