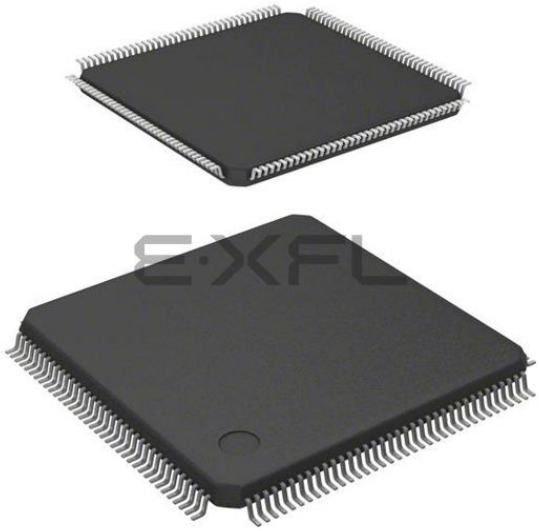

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	115
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r5zit6p

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.21 Voltage reference buffer (VREFBUF)

The STM32L4Rxxx devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

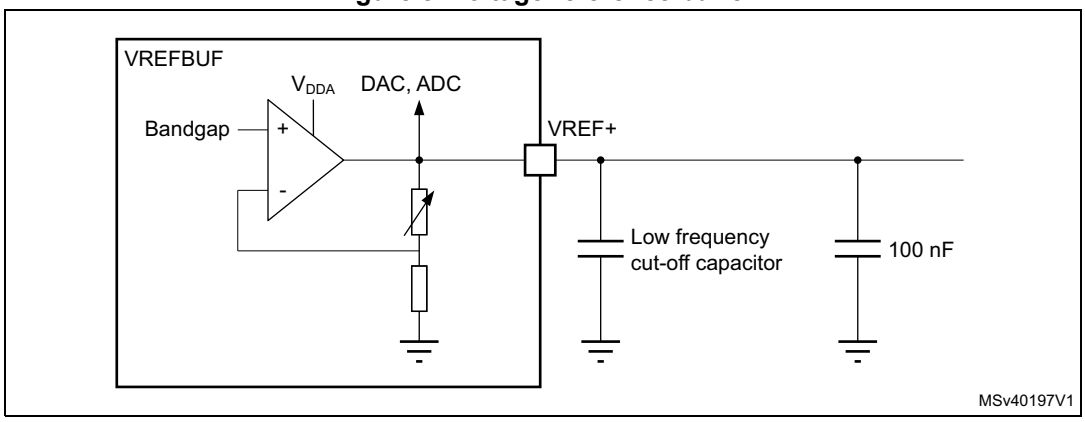
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 8. Voltage reference buffer



3.22 Comparators (COMP)

The STM32L4Rxxx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
54	K10	K10	76	76	J3	M12	M12	51	72	J9	J3	J3	L10	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	M2	L12	L12	-	-	-	M2	M2	-	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	52	73	-	-	-	M13	VDDDSI	S	-	-	-	-
-	-	-	-	-	-	L13	L13	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	53	74	L12	L3	L3	L13	VCAPDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	54	75	K11	L1	L1	L11	DSI_D0P	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	55	76	K12	L2	L2	L12	DSI_D0N	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	56	77	-	-	-	J13	VSSDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	57	78	J11	K1	K1	K11	DSI_CKP	I/O	-	(3)	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
86	A6	A6	119	119	A5	D7	D7	88	121	D7	A5	A5	D7	PD5	I/O	FT	-	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	-	120	120	B6	M3	M3	-	122	-	B6	B6	M3	VSS	S	-	-	-	-
-	-	-	121	121	A6	A8	A8	-	123	-	A6	A6	A8	VDD	S	-	-	-	-
87	B6	B6	122	122	E7	E7	E7	89	124	B7	E7	E7	E7	PD6	I/O	FT	-	SAI1_D1, DCMI_D10, SPI3_MOSI, DFSDM1_DATIN1, USART2_RX, OCTOSPIM_P1_IO6, LCD_DE, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
88	A5	A5	123	123	D7	F7	F7	90	125	E7	D7	D7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, OCTOSPIM_P1_IO7, FMC_NCE/FMC_NE1, EVENTOUT	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port C	PC0	LPUART1_RX	-	-	-	-	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	-	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	TSC_G4_IO1	DCMI_D0	LCD_R0	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_ D123DIR	TSC_G4_IO2	DCMI_D1	LCD_R1	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800- 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF	1 KB	VREFBUF
	0x4001 0000 - 0x4001 002F	1 KB	SYSCFG
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	3 KB	Reserved
	0x4000 8400 - 0x4000 87FF	1 KB	I2C4
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	2 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 1800 - 0x4000 23FF	4 KB	Reserved

Table 47. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	120	430	1400	2750	5050	280	1100	3300	6500	13000	µA
			2.4 V	120	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3.6 V	120	430	1400	2750	5150	280	1100	3300	6600	13000(2)	
IDD (Stop 1 with RTC)	Supply current in STOP 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	120	430	1400	2700	5050	280	1100	3300	6500	13000	
			2.4 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6600	13000	
			3.6 V	125	435	1400	2750	5150	280	1100	3300	6600	13000	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	120	430	1400	2750	5050	300	1100	3500	6900	13000	
			2.4 V	120	435	1400	2750	5100	300	1100	3500	6900	13000	
			3 V	125	435	1400	2750	5100	320	1100	3500	6900	13000	
			3.6 V	125	435	1400	2750	5150	320	1100	3500	6900	13000	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			2.4 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3.6 V	120	425	1350	2700	-	300	1100	3400	6800	-	
IDD (wakeup from Stop 1)	Supply current during wakeup from Stop 1 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(4)	3 V	2.10	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(4)	3 V	0.70	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(4)	3 V	1.50	-	-	-	-	-	-	-	-	-	

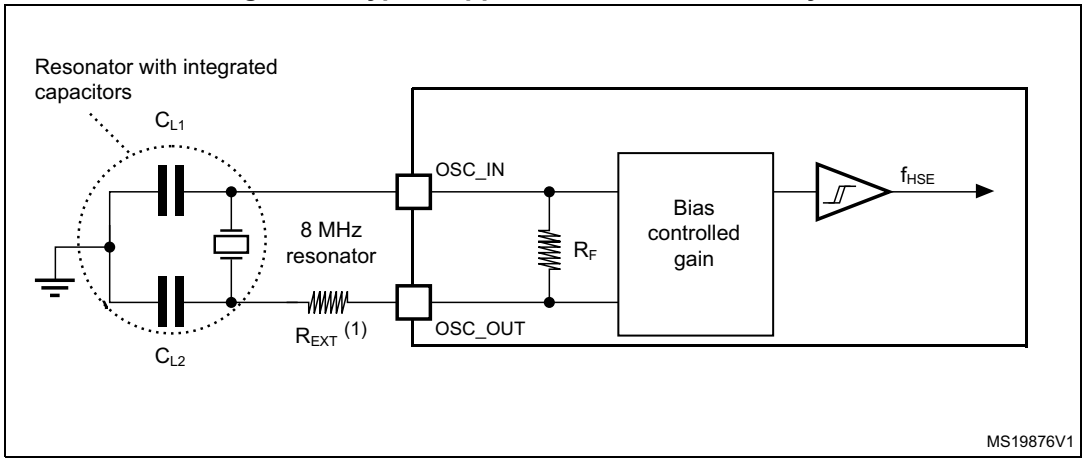
1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*

Table 52. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	USART2 independent clock domain	5.35	5	4.15	4.5	µA/MHz
	USART2 APB clock domain	3	2.75	2.5	2.5	
	USART3 independent clock domain	6.35	6	5	5.5	
	USART3 APB clock domain	2.6	2.4	2.1	2.5	
	UART4 independent clock domain	5.15	4.9	3.75	4.5	
	UART4 APB clock domain	2.5	2.25	2.1	2.5	
	UART5 independent clock domain	5.4	5	4.15	5	
	UART5 APB clock domain	2.4	2.25	2.1	2	
	WWDG	0.75	0.625	0.835	0.5	
	All APB1 on	110	100	84	97	
APB2	AHB to APB2 bridge	0.185	0.15	0.125	0.5	µA/MHz
	DFSDM	9.5	9	7.5	8.5	
	DSI independent clock domain	33	34.5	29.5	NA	
	DSI APB clock domain	13	7.15	29	NA	
	FW	0.665	0.625	0.5	0.5	
	LTDC independent clock domain	35.5	34.5	40	NA	
	LTDC APB clock domain	18	17	14	NA	
	SAI1 independent clock domain	3.1	2.9	2.5	3	
	SAI1 APB clock domain	2.6	2.4	1.9	2	
	SAI2 independent clock domain	3.15	3	2.55	3	
	SAI2 APB clock domain	2.6	2.4	1.9	2.5	
	SPI1	2.25	2.15	1.75	1	
	SYSCFG/VREFBUF/COMP	0.565	0.6	0.5	0.5	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 59*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

6.3.13 Flash memory characteristics

Table 69. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4	
t_{prog_page}	One page (4 Kbytes) programming time	Normal programming	41.8	43	
		Fast programming	30.4	31	
t_{ERASE}	Page (4 Kbytes) erase time	-	22	24.5	
t_{prog_bank}	One bank (1 Mbyte) programming time	Normal programming	10.7	11	s
		Fast programming	7.7	8	
t_{ME}	Mass erase time (one or two banks)	-	22.1	25	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 6 µs)	-	
		Erase mode	7 (for 67 µs)	-	

1. Guaranteed by design.

Table 70. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 74. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A(1)

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

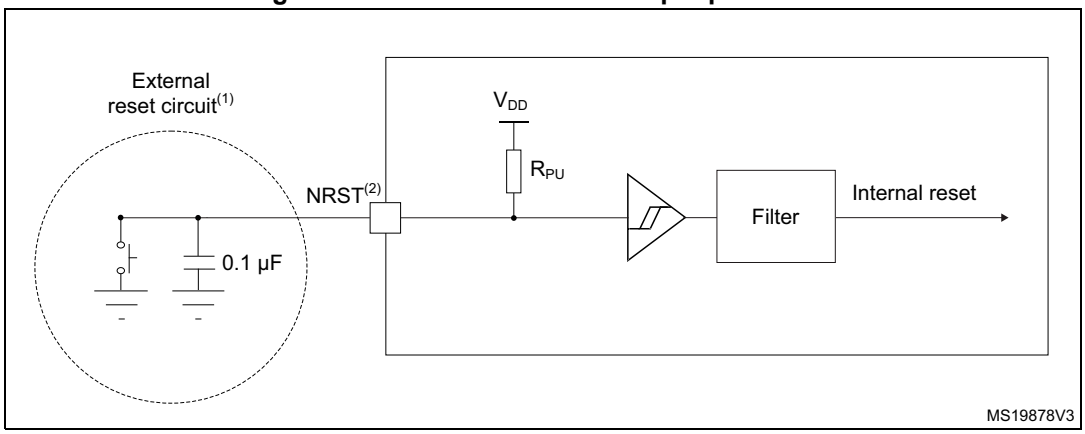
While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 75*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Figure 40. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 79: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.19 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 80. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

6.3.20 Analog switches booster

Table 81. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

Table 85. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 88. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

6.3.24 Comparator characteristics

Table 91. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Figure 65. OctoSPI Hyperbus read

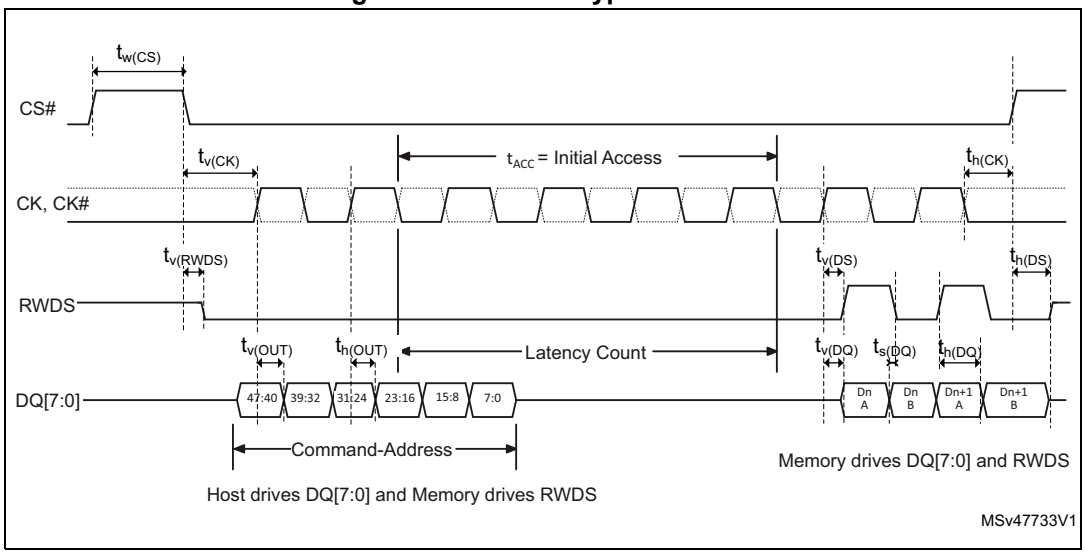


Figure 66. OctoSPI Hyperbus read with double latency

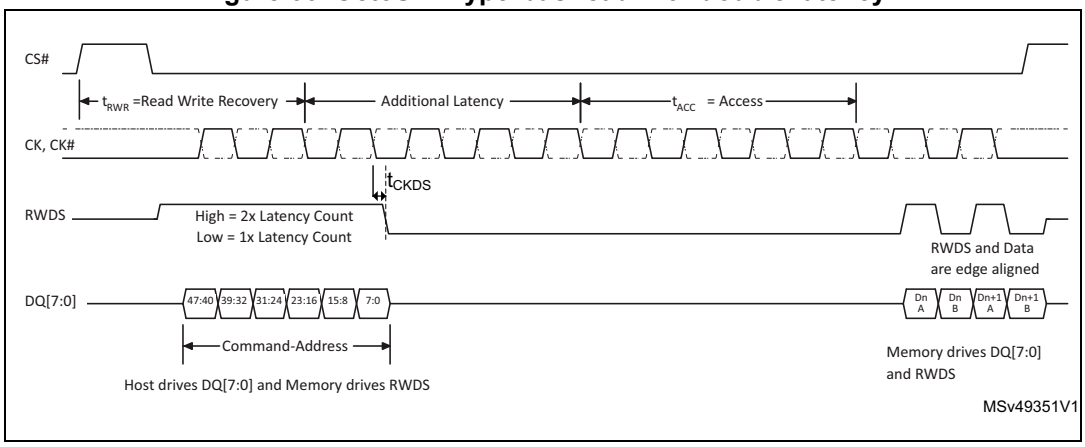
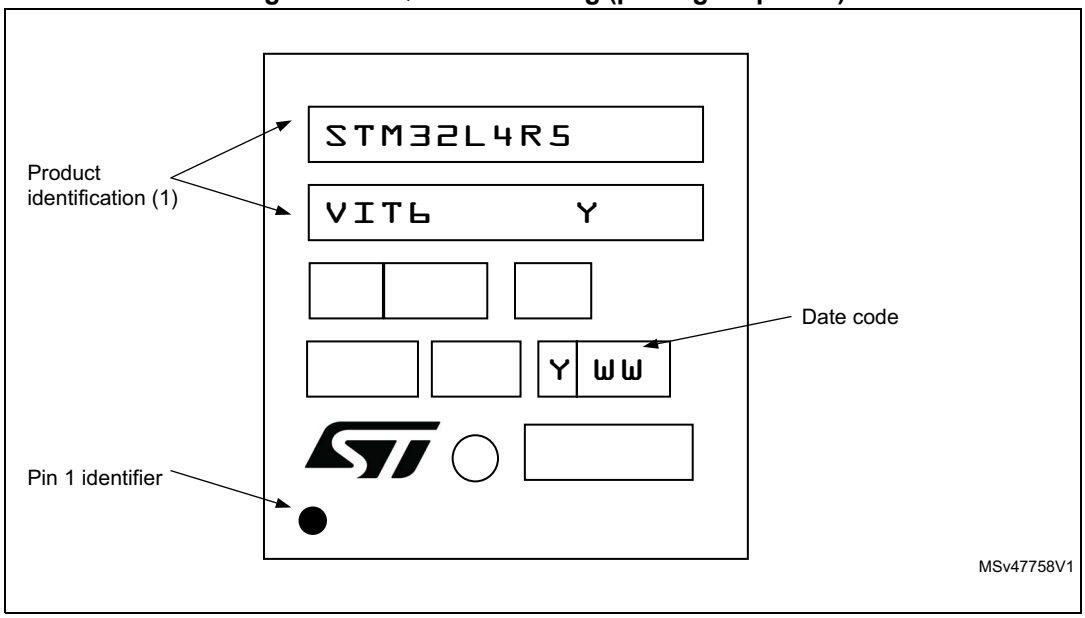


Figure 90. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

8 Ordering information

Table 138. STM32L4Rxxx ordering information scheme

Example: STM32 L 4Rx V I T 6 P TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

4R5 = STM32L4R5xx
4R7 = STM32L4R7xx, LCD-TFT, Chrom-GRC™
4R9 = STM32L4R9xx, LCD-TFT Chrom-GRC™ and DSI Host

Pin count

V = 100 pins
Q = 132 balls
Z = 144 pins/balls
A = 169 balls

Flash memory size

I = 2 Mbytes of Flash memory
G = 1 Mbyte of Flash memory

Package

T = LQFP
I = UFBGA (7 x 7 mm)
J = UFBGA (10 x 10 mm)
Y = WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)
3 = Industrial temperature range, -40 to 125 °C (130°C junction)

Option

P = Dedicated pinout supporting external SMPS

Packing

TR = tape and reel
xxx = programmed parts

9 Revision history

Table 139. Document revision history

Date	Revision	Changes
10-Oct-2017	1	Initial release.
24-Nov-2017	2	Added: – *Section 6.3.10: MIPI D-PHY characteristics* – *Section 6.3.11: MIPI D-PHY PLL characteristics* – *Section 6.3.12: MIPI D-PHY regulator characteristics* Updated: – Cover page *Features* (Performance benchmark and Energy benchmark) – *Table 4: STM32L4R5xx modes overview* – *Section 3.12: Clocks and startup* – *Figure 18: STM32L4R5xx WLCSP144 ballout*(1) – *Figure 19: STM32L4R5xx UFBGA132 ballout*(1) – *Table 22: General operating conditions*
19-Jan-2018	3	Added: – *Figure 4: STM32L4R5xxxP and STM32L4R7xxxP with external SMPS power supply overview* – *Figure 11: STM32L4R5xxxP UFBGA169 external SMPS ballout*(1) – *Figure 14: STM32L4R5ZxxxP external SMPS LQFP144 pinout*(1) – *Figure 17: STM32L4R9ZxxxP WLCSP144 external SMPS ballout*(1) – *Figure 20: STM32L4R5xxxP UFBGA132 external SMPS ballout*(1) Updated: – Footnotes of *Table 2: STM32L4R5xx, STM32L4R7xx and STM32L4R9xx features and peripheral counts* – *Table 15: STM32L4Rxxx pin definitions* – *Figure 1: STM32L4R5xx, STM32L4R7xx and STM32L4R9xx block diagram* – *Figure 3: STM32L4R5xx and STM32L4R7xx power supply overview* – *Figure 5: STM32L4R9xx power supply overview* – *Section 3.10.1: Power supply schemes* – *Section 3.12: Clocks and startup*

Table 139. Document revision history (continued)

Date	Revision	Changes
25-Apr-2018	4	Added: – *Figure 6: Power-up/down sequence* – *Figure 66: OctoSPI Hyperbus read with double latency* Updated: – *Section 1: Introduction* – *Section 3.10.1: Power supply schemes* – *Table 8: Temperature sensor calibration values* – Updated maximum value for V_{DD12}-V_{SS} on *Table 19: Voltage characteristics* – Updated maximum value for V_{DD12} on *Table 22: General operating conditions* – Title of *Table 41: Typical consumption in Run and Low-power run modes, with different codes running from SRAM1 and power supplied by external SMPS* – Values on column “Parameter”’ on *Table 42: Current consumption in Sleep and Low-power sleep mode, Flash ON* – Values on column “Parameter”’ on *Table 43: Current consumption in Sleep and Low-power sleep modes, Flash ON and power supplied by external SMPS* – Title of *Table 44: Current consumption in Low-power sleep mode, Flash in power-down* – FCK 1/t(CK) rows on *Table 122: OctoSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus*