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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA
Supplier Device Package	169-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r7aii6

retained in Standby mode, supplied by the low-power regulator (standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2, SRAM3 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

The CAN peripheral supports:

- CAN protocol version 2.0 A, B Active
- Bit rates of up to 1 Mbit/s
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - Scalable filter banks: 28 filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.38 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The SD/SDIO, MultiMediaCard (MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD Memory Card Specifications Version 4.1. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Full compliance with SDIO Card Specification Version 4.0: card support for two different databus modes: 1-bit (default) and 4-bit. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Data transfer up to 104 Mbyte/s for the 8-bit mode (depending maximum allowed IO speed)
- Data and command output enable signals to control external bidirectional drivers.

- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Hyperbus™ support
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.43 OctoSPI IO manager (OctoSPIIOM)

The OctoSPI IO Manager is a low level interface allowing:

- Efficient OctoSPI pin assignment with a full IO Matrix (before alternate function map)
- Multiplexing single/dual/quad/octal SPI interface over the same bus

The OctoSPI IO Manager has the following features:

- Support up to two single/dual/quad/octal SPI Interface
- Support up to eight ports for pin assignment
- Fully programmable IO matrix for pin assignment by function (data/control/clock)
- Muxer for Single/Dual/Quad/Octal SPI interface multiplexing over the same bus

3.44 Development support

3.44.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins could be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 17. STM32L4R9ZxxxP WLCSP144 external SMPS ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PA14	PA15	PD0	PD5	VDD	PG12	VDDIO2	PB7	PE0	VDD12	VSS_3
B	VDD	VDDBUS	PA13	PC12	PD2	VSS	PG10	PB3	PH3-BOOT0	PB9	PE2	VDD_3
C	PA11	PA12	PC10	PC11	PD1	PD4	PG9	PB4	PB6	PB8	PE3	PE4
D	PC8	PC9	PA8	PA9	PA10	PD3	PD7	PE1	PE5	PE6	PC13	VSS
E	PG7	PG8	VDDIO2	PC6	PG6	PC7	PD6	PB5	PF0	VBAT	PC14-OSC32_IN	PC15-OSC32_OUT
F	PD15	PG2	PD14	PD12	PG3	PG4	PG5	PF1	PF5	PF4	PF3	PF2
G	VSS	VDD	PD13	PD11	PD10	PE9	PF14	PA5	PF7	PF6	VSS	VDD
H	PD9	PD8	PB14	PB13	PE14	PE8	PB1	PA2	PC2	PF10	NRST	PH0-OSC_IN
J	DSI_D1N	DSI_D1P	PB15	PB12	PE13	PF15	PB2	PA6	PA0	PC3	PC0	PH1-OSC_OUT
K	DSI_CKP	DSI_CKN	VSSDSI	PE15	PE10	PG0	PF11	PC5	PA4	PA1	VSSA/VREF-	PC1
L	DSI_D0P	DSI_D0N	VCAPDSI	PB10	PE11	PG1	VDD	PF12	PC4	PA3	VREF+	VDDA
M	VDD	VDD	VDD12	VSS	PE12	PE7	PF13	VSS	PB0	PA7	VDD	VSS

MSv49307V1

1. The above figure shows the package top view.

Figure 18. STM32L4R5xx WLCSP144 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PA14	PA15	PD0	PD5	VDD	PG12	VDDIO2	PB7	PE0	PE1	VSS
B	VDD	VDDUSB	PA13	PC12	PD2	VSS	PG10	PB3	PH3-BOOT0	PB9	PE2	VDD
C	PA11	PA12	PC10	PC11	PD1	PD4	PG9	PB4	PB6	PB8	PE3	PE4
D	PC8	PC9	PA8	PA9	PA10	PD3	PD7	PG13	PE5	PE6	PC13	VSS
E	PG7	PG8	VDDIO2	PC6	PG6	PC7	PD6	PB5	PF0	VBAT	PC14-OSC32_IN	PC15-OSC32_OUT
F	PD15	PG2	PD14	PD12	PG3	PG4	PG5	PF1	PF5	PF4	PF3	PF2
G	VSS	VDD	PD13	PD11	PD10	PE9	PF14	PA5	PF7	PF6	VSS	VDD
H	PD9	PD8	PB14	PB13	PE14	PE8	PB1	PA2	PC2	PF10	NRST	PH0-OSC_IN
J	NC	NC	PB15	PB12	PE13	PF15	PB2	PA6	PA0	PC3	PC0	PH1-OSC_OUT
K	NC	NC	VSS	PE15	PE10	PG0	PF11	PC5	PA4	PA1	VSSA/VREF-	PC1
L	NC	NC	NC	PB10	PE11	PG1	VDD	PF12	PC4	PA3	VREF+	VDDA
M	VDD	VDD	VSS	PB11	PE12	PE7	PF13	VSS	PB0	PA7	VDD	VSS

MSv43442V1

1. The above figure shows the package top view.
   NC (not-connected) balls must be left unconnected.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
3	B1	B1	3	3	C12	D1	D1	3	3	D3	C12	C12	D1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, SAI1_D2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4, LCD_B0, FMC_A20, SAI1_FS_A, EVENTOUT	-
4	C2	C2	4	4	D9	E4	E4	4	4	C2	D9	D9	E4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, SAI1_CK2, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6, LCD_G0, FMC_A21, SAI1_SCK_A, EVENTOUT	-
5	D2	D2	5	5	D10	E3	E3	5	5	D4	D10	D10	E3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_D1, DCMI_D7, LCD_G1, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3,WKUP3
6	E2	E2	6	6	E10	E2	E2	6	6	B1	E10	E10	E2	VBAT	S	-	-	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
21	L1	L1	32	32	L11	L1	L1	-	29	K2	L11	L11	L1	VREF+	S	-	-	-	VREFBUF_OUT
22	M1	M1	33	33	L12	L2	L2	-	30	L1	L12	L12	L2	VDDA	S	-	-	-	-
-	-	-	-	-	-	-	-	20	-	-	-	-	-	VDDA/ VREF+	S	-	-	-	-
23	L2	L2	34	34	J9	K3	K3	21	31	K3	J9	J9	K3	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS_NSS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC1_IN5, RTC_TAMP2,WKUP1
-	M3	M3	-	-	-	M1	M1	-	-	-	-	-	-	OPAMP 1_VINM	I	TT	-	-	-
24	M2	M2	35	35	K10	N2	N2	22	32	L2	K10	K10	M1	PA1	I/O	FT_la	-	TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, OCTOSPIM_P1_DQS, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC1_IN6

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
54	K10	K10	76	76	J3	M12	M12	51	72	J9	J3	J3	L10	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	M2	L12	L12	-	-	-	M2	M2	-	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	52	73	-	-	-	M13	VDDDSI	S	-	-	-	-
-	-	-	-	-	-	L13	L13	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	53	74	L12	L3	L3	L13	VCAPDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	54	75	K11	L1	L1	L11	DSI_D0P	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	55	76	K12	L2	L2	L12	DSI_D0N	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	56	77	-	-	-	J13	VSSDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	57	78	J11	K1	K1	K11	DSI_CKP	I/O	-	(3)	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	-	-	-	-	-	D11	D11	-	-	-	-	-	C11	PH9	I/O	FT	-	I2C3_SMBA, OCTOSPIM_P2_IO4, DCMI_D0, EVENTOUT	-
-	-	-	-	-	-	B13	B13	-	-	-	-	-	B13	PH12	I/O	FT	-	TIM5_CH3, OCTOSPIM_P2_IO7, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	A13	A13	-	-	-	-	-	A13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-
-	-	-	-	-	-	B12	B12	-	-	-	-	-	B12	PH15	I/O	FT	-	TIM8_CH3N, OCTOSPIM_P2_IO6, DCMI_D11, EVENTOUT	-
-	-	-	-	-	-	A12	A12	-	-	-	-	-	A12	PI0	I/O	FT	-	TIM5_CH4, OCTOSPIM_P1_IO5, SPI2_NSS, DCMI_D13, EVENTOUT	-
-	-	-	-	-	-	C11	C11	-	-	-	-	-	-	PI8	I/O	FT	-	OCTOSPIM_P2_NCS, DCMI_D12, EVENTOUT	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port C	PC0	LPUART1_RX	-	-	-	-	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	-	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	TSC_G4_IO1	DCMI_D0	LCD_R0	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_ D123DIR	TSC_G4_IO2	DCMI_D1	LCD_R1	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 24*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 25*.

Figure 24. Pin loading conditions

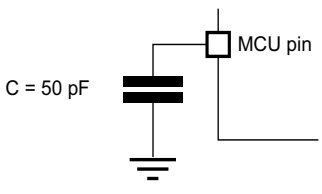


Figure 25. Pin input voltage

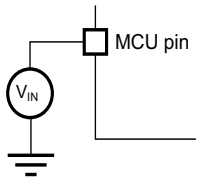


Table 36. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26MHz	Reduced code(1)	3.40	3.60	mA	131	138	µA/MHz
				Coremark	3.90	3.95		150	152	
				Dhrystone2.1	4.25	4.30		163	165	
				Fibonacci	3.65	3.90		140	150	
				While(1)	3.15	3.15		121	121	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	11.5	12.5	mA	144	156	µA/MHz
				Coremark	13.5	13.5		169	169	
				Dhrystone2.1	14.5	14.5		181	181	
				Fibonacci	12.5	14.0		156	175	
				While(1)	10.5	10.5		131	131	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.5	17.0	mA	154	142	µA/MHz
				Coremark	21.5	21.5		179	179	
				Dhrystone2.1	22.5	22.5		188	188	
				Fibonacci	20.0	21.0		167	175	
				While(1)	16.5	16.5		138	138	

Table 50. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	245	420	1450	3850	10500	-	-	-	-	-	nA
			2.4 V	340	555	1750	4600	12500	-	-	-	-	-	
			3 V	465	730	2250	5900	15500	-	-	-	-	-	
			3.6 V	615	945	2850	7250	19000	-	-	-	-	-	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	335	520	1550	4000	-	-	-	-	-	-	
			2.4 V	435	650	1850	4750	-	-	-	-	-	-	
			3 V	560	830	2350	6050	-	-	-	-	-	-	
			3.6 V	730	1050	2950	7400	-	-	-	-	-	-	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz(3)	3 V	0.5	-	-	-	-	-	-	-	-	-	mA

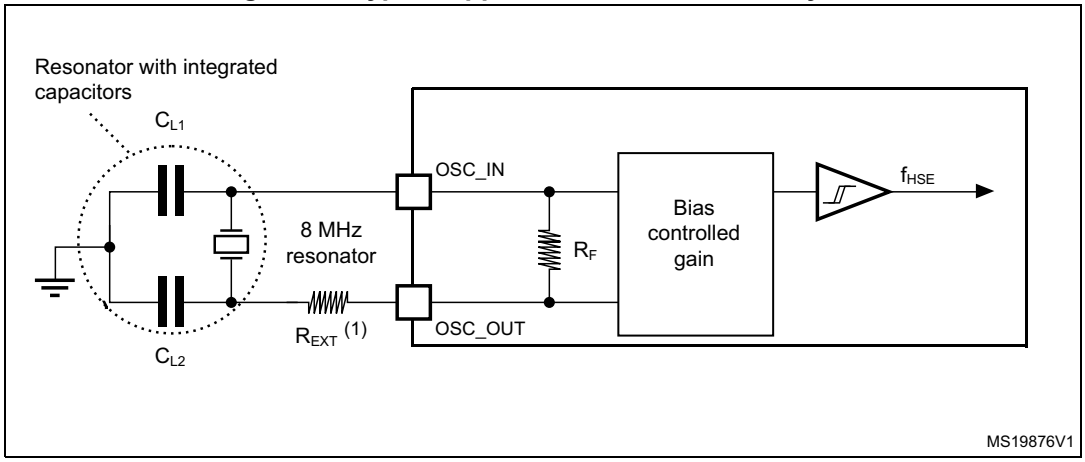
1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*.

Table 52. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	USART2 independent clock domain	5.35	5	4.15	4.5	µA/MHz
	USART2 APB clock domain	3	2.75	2.5	2.5	
	USART3 independent clock domain	6.35	6	5	5.5	
	USART3 APB clock domain	2.6	2.4	2.1	2.5	
	UART4 independent clock domain	5.15	4.9	3.75	4.5	
	UART4 APB clock domain	2.5	2.25	2.1	2.5	
	UART5 independent clock domain	5.4	5	4.15	5	
	UART5 APB clock domain	2.4	2.25	2.1	2	
	WWDG	0.75	0.625	0.835	0.5	
	All APB1 on	110	100	84	97	
APB2	AHB to APB2 bridge	0.185	0.15	0.125	0.5	µA/MHz
	DFSDM	9.5	9	7.5	8.5	
	DSI independent clock domain	33	34.5	29.5	NA	
	DSI APB clock domain	13	7.15	29	NA	
	FW	0.665	0.625	0.5	0.5	
	LTDC independent clock domain	35.5	34.5	40	NA	
	LTDC APB clock domain	18	17	14	NA	
	SAI1 independent clock domain	3.1	2.9	2.5	3	
	SAI1 APB clock domain	2.6	2.4	1.9	2	
	SAI2 independent clock domain	3.15	3	2.55	3	
	SAI2 APB clock domain	2.6	2.4	1.9	2.5	
	SPI1	2.25	2.15	1.75	1	
	SYSCFG/VREFBUF/COMP	0.565	0.6	0.5	0.5	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with an 8 MHz crystal

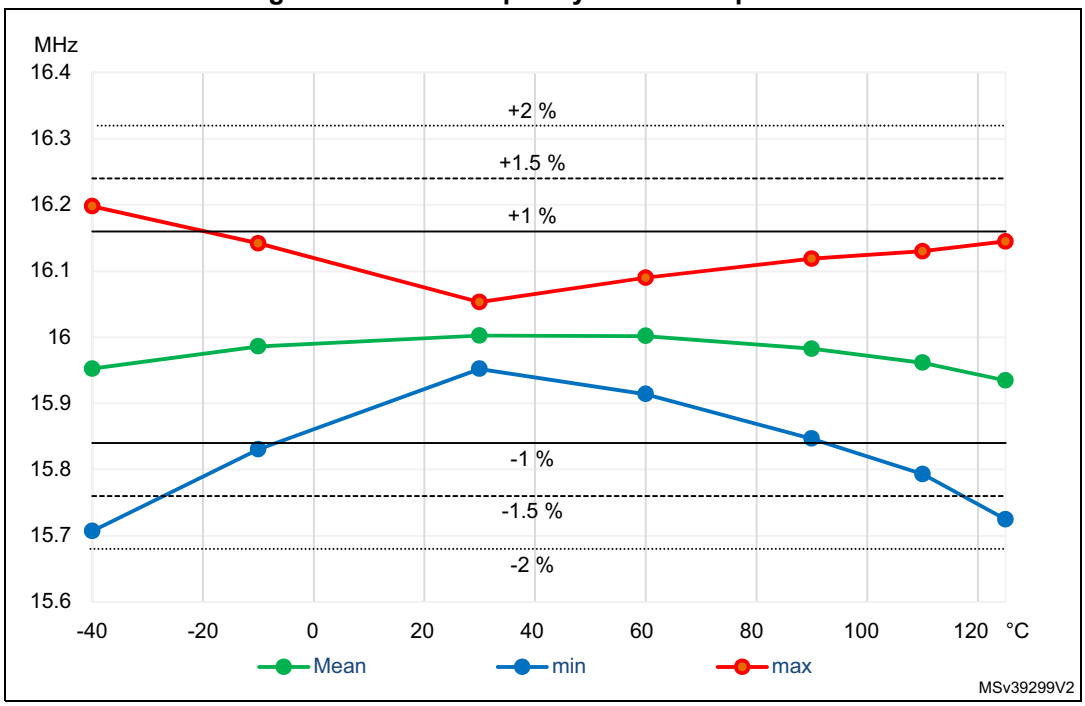


1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 59*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Figure 33. HSI16 frequency versus temperature



6.3.26 Temperature sensor characteristics

Table 93. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.27 V_{BAT} monitoring characteristics

Table 94. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 95. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.33 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 123* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 21*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Figure 68. DCMI timing diagram

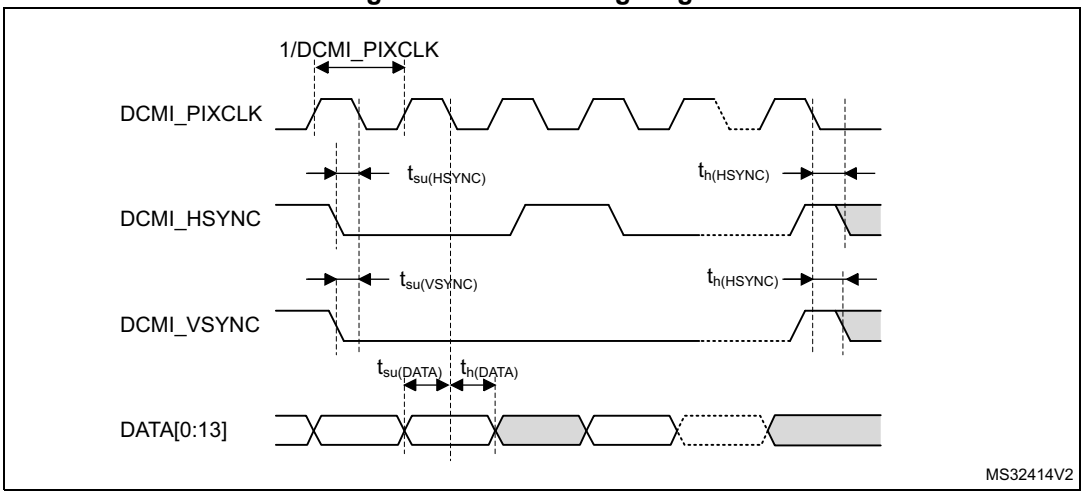


Table 123. DCMI characteristics(1)

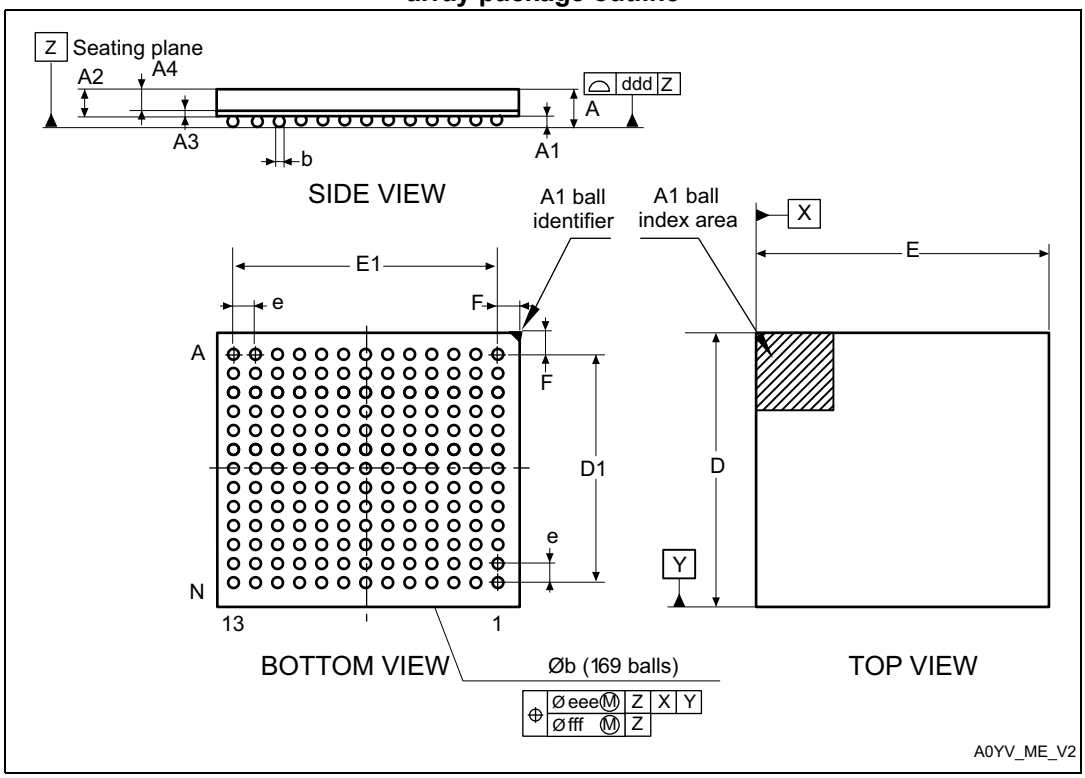
Symbol	Parameter	Condition	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	1.71 < VDD < 3.6 Voltage range V1	-	48	MHz
		1.71 < VDD < 3.6 Voltage range V2	-	10	
D_{pixel}	Pixel clock input duty cycle	-	30	70	%

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA169 package information

Figure 72. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 127. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

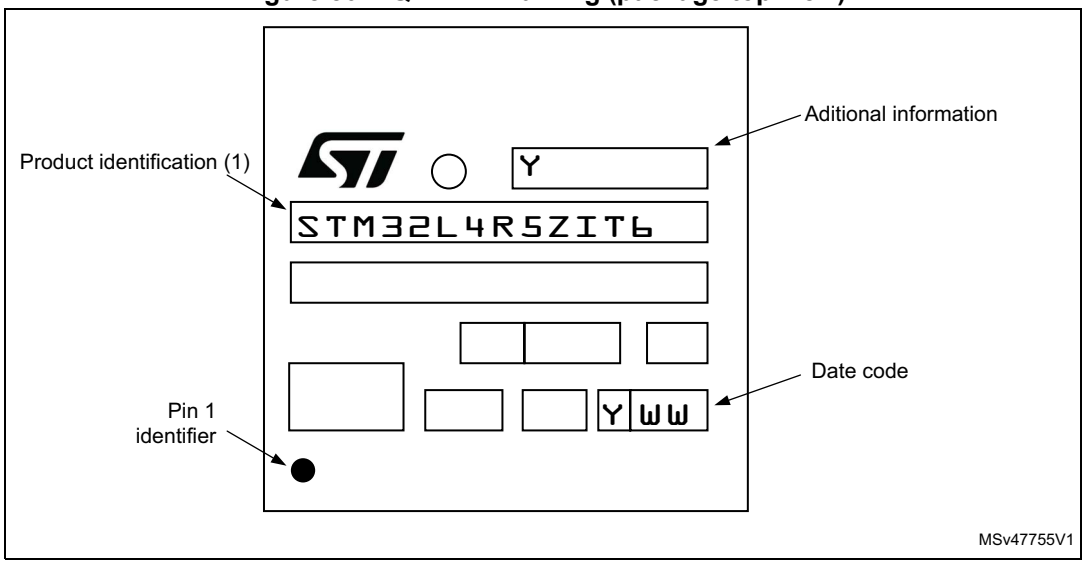
Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146

LQFP144 device marking

The following figures gives an example of topside marking orientation versus pin 1 identifier location.

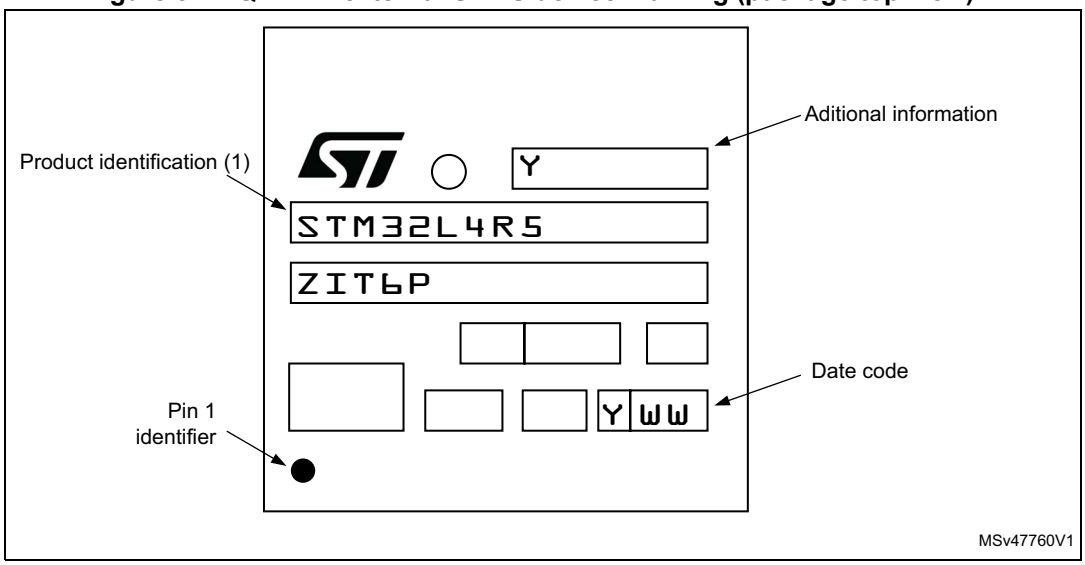
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 80. LQFP144 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 81. LQFP144 external SMPS device marking (package top view)(2)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering

9 Revision history

Table 139. Document revision history

Date	Revision	Changes
10-Oct-2017	1	Initial release.
24-Nov-2017	2	Added: – *Section 6.3.10: MIPI D-PHY characteristics* – *Section 6.3.11: MIPI D-PHY PLL characteristics* – *Section 6.3.12: MIPI D-PHY regulator characteristics* Updated: – Cover page *Features* (Performance benchmark and Energy benchmark) – *Table 4: STM32L4R5xx modes overview* – *Section 3.12: Clocks and startup* – *Figure 18: STM32L4R5xx WLCSP144 ballout*(1) – *Figure 19: STM32L4R5xx UFBGA132 ballout*(1) – *Table 22: General operating conditions*
19-Jan-2018	3	Added: – *Figure 4: STM32L4R5xxxP and STM32L4R7xxxP with external SMPS power supply overview* – *Figure 11: STM32L4R5xxxP UFBGA169 external SMPS ballout*(1) – *Figure 14: STM32L4R5ZxxxP external SMPS LQFP144 pinout*(1) – *Figure 17: STM32L4R9ZxxxP WLCSP144 external SMPS ballout*(1) – *Figure 20: STM32L4R5xxxP UFBGA132 external SMPS ballout*(1) Updated: – Footnotes of *Table 2: STM32L4R5xx, STM32L4R7xx and STM32L4R9xx features and peripheral counts* – *Table 15: STM32L4Rxxx pin definitions* – *Figure 1: STM32L4R5xx, STM32L4R7xx and STM32L4R9xx block diagram* – *Figure 3: STM32L4R5xx and STM32L4R7xx power supply overview* – *Figure 5: STM32L4R9xx power supply overview* – *Section 3.10.1: Power supply schemes* – *Section 3.12: Clocks and startup*