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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r7vit6

3.12 Clocks and startup

The clock controller (see *Figure 7*) distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock. The HSE must be available when the DSI-HOST peripheral is used.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 120 MHz.
- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG, the two SAIs, LCD-TFT and DSI-HOST. When using DSI-HOST peripheral, the high-speed external crystal (HSE) must be available.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

The DSI Host main features are:

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video Mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for end of transmission packet (EoTp)
- Fault recovery schemes
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for generic and DCS commands
  - Video Mode interface through LTDC
  - Adapted command mode interface through LTDC
- Independently programmable virtual channel ID in
  - Video mode
  - Adapted command mode
  - APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2 and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps

Adapted interface features:

- Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2 and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (four memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

3.42 OctoSPI interface (OctoSPI)

The OctoSPI is a specialized communication interface targetting single, dual, quad or octal SPI memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the OctoSPI registers
- Status polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation

The OctoSPI supports two frame formats:

- Classical frame format with command, address, alternate byte, dummy cycles and data phase over 1, 2, 4 or 8 data pins
- Hyperbus^{TM} frame format

The OctoSPI offers the following features:

- Three functional modes: indirect, status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where 8 bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR and DTR support
- Data strobe support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
7	C1	C1	7	7	D11	E1	E1	7	7	E4	D11	D11	E1	PC13	I/O	FT	- (1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/RTC_OUT,WKUP2
8	D1	D1	8	8	E11	F1	F1	8	8	D1	E11	E11	F1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
9	E1	E1	9	9	E12	G1	G1	9	9	D2	E12	E12	G1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	D6	D6	10	10	E9	F5	F5	-	10	E3	E9	E9	F5	PF0	I/O	FT_f	-	I2C2_SDA, OCTOSPIM_P2_IO0, FMC_A0, EVENTOUT	-
-	D5	D5	11	11	F8	F4	F4	-	11	E2	F8	F8	F4	PF1	I/O	FT_f	-	I2C2_SCL, OCTOSPIM_P2_IO1, FMC_A1, EVENTOUT	-
-	D4	D4	12	12	F12	F3	F3	-	12	E1	F12	F12	F3	PF2	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_IO2, FMC_A2, EVENTOUT	-
-	E4	E4	13	13	F11	G3	G3	-	13	E5	F11	F11	G3	PF3	I/O	FT	-	OCTOSPIM_P2_IO3, FMC_A3, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	-	-	22	22	H10	H4	H4	-	20	G3	H10	H10	H4	PF10	I/O	FT	-	OCTOSPIM_P1_CLK, DFSDM1_CKOUT, DCMI_D11, SAI1_D3, TIM15_CH2, EVENTOUT	-
12	F1	F1	23	23	H12	H1	H1	12	21	H1	H12	H12	H1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
13	G1	G1	24	24	J12	J1	J1	13	22	H2	J12	J12	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
14	H2	H2	25	25	H11	H3	H3	14	23	J1	H11	H11	H3	NRST	I-O	RST	-	-	-
15	H1	H1	26	26	J11	J2	J2	15	24	H3	J11	J11	J2	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, DFSDM1_DATIN4, LPUART1_RX, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	ADC1_IN1

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	M4	M4	-	-	-	N4	N4	-	-	-	-	-	-	OPAMP2_VINM	I	TT	-	-	-
32	J5	J5	43	43	M10	L4	L4	30	40	M4	M10	M10	M4	PA7	I/O	FT_fla	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, OCTOSPIM_P1_IO2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC1_IN12
33	K5	K5	44	44	L9	H5	H5	31	41	L5	L9	L9	K4	PC4	I/O	FT_a	-	USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT	COMP1_INM, ADC1_IN13
34	L5	L5	45	45	K8	J5	J5	-	-	K5	K8	K8	-	PC5	I/O	FT_a	-	SAI1_D3, USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
35	M5	M5	46	46	M9	K5	K5	32	42	M5	M9	M9	N4	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC1_IN15

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
38	M7	M7	58	58	M6	L7	L7	35	54	G6	M6	M6	L7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, LCD_B6, FMC_D4, SAI1_SD_B, EVENTOUT	-
39	L7	L7	59	59	H6	K7	K7	36	55	K7	H6	H6	K6	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, LCD_B7, FMC_D5, SAI1_SCK_B, EVENTOUT	-
40	M8	M8	60	60	G6	J7	J7	37	56	J7	G6	G6	J6	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, LCD_G2, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	F6	F6	61	61	-	M7	M7	-	57	C1	-	-	M7	VSS	S	-	-	-	-
-	G6	G6	62	62	-	-	-	-	58	-	-	-	-	VDD	S	-	-	-	-
41	L8	L8	63	63	K5	H7	H7	38	59	L8	K5	K5	H6	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, TSC_G5_IO1, OCTOSPIM_P1_CLK, LCD_G3, FMC_D7, SAI1_MCLK_B, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
86	A6	A6	119	119	A5	D7	D7	88	121	D7	A5	A5	D7	PD5	I/O	FT	-	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	-	120	120	B6	M3	M3	-	122	-	B6	B6	M3	VSS	S	-	-	-	-
-	-	-	121	121	A6	A8	A8	-	123	-	A6	A6	A8	VDD	S	-	-	-	-
87	B6	B6	122	122	E7	E7	E7	89	124	B7	E7	E7	E7	PD6	I/O	FT	-	SAI1_D1, DCMI_D10, SPI3_MOSI, DFSDM1_DATIN1, USART2_RX, OCTOSPIM_P1_IO6, LCD_DE, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
88	A5	A5	123	123	D7	F7	F7	90	125	E7	D7	D7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, OCTOSPIM_P1_IO7, FMC_NCE/FMC_NE1, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

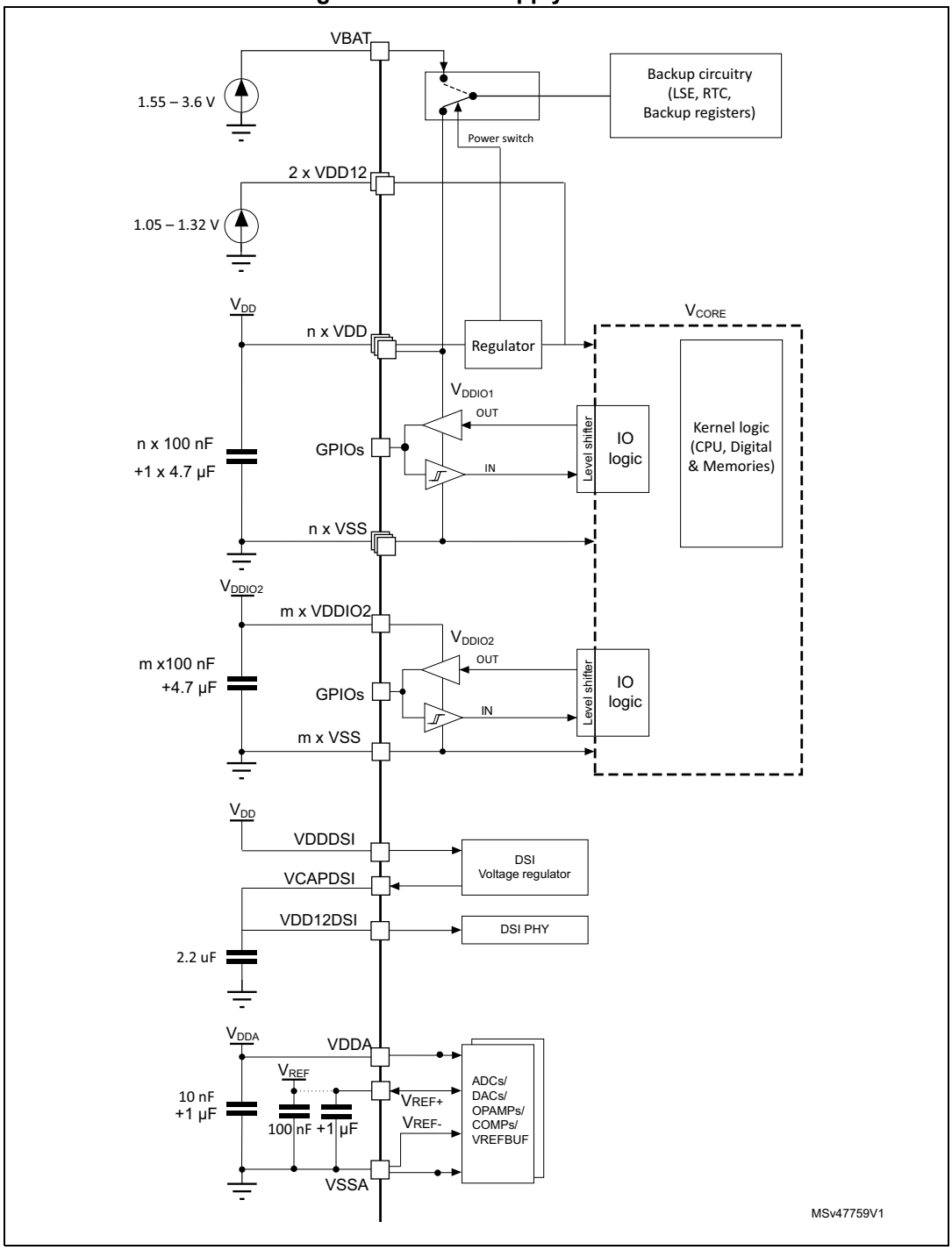
Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	D9	D9	124	124	C7	B7	B7	-	126	F6	C7	C7	B7	PG9	I/O	FT_s	-	OCTOSPIM_P2_IO6, SPI3_SCK, USART1_TX, FMC_NCE/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
-	D8	D8	125	125	B7	D6	D6	-	127	E6	B7	B7	D6	PG10	I/O	FT_s	-	LPTIM1_IN1, OCTOSPIM_P2_IO7, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	G3	G3	126	126	-	E6	E6	-	128	-	-	-	E6	PG11	I/O	FT_s	-	LPTIM1_IN2, OCTOSPIM_P1_IO5, SPI3_MOSI, USART1_CTS_NSS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-

Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses(1)

Bus	Boundary address	Size (bytes)	Peripheral
-	0xA000 1800 - 0xDFFF FFFF	1 KB	Reserved
	0xA000 1400 - 0xA000 17FF	1 KB	OCTOSPI2 registers
	0xA000 1000 - 0xA000 13FF	1 KB	OCTOSPI1 registers
	0xA000 0400 - 0xA000 0FFF	1 KB	Reserved
	0xA000 0000 - 0xA000 03FF	1 KB	FSMC registers
AHB2	0x5006 2000 - 0x5FFF FFFF	~260 MB	Reserved
	0x5006 2400 - 0x5006 27FF	1 KB	SDMMC1
	0x5006 2000 - 0x5006 23FF	1 KB	Reserved
	0x5006 1C00 - 0x5006 1FFF	1 KB	OCTOSPIIOM
	0x5006 0C00 - 0x5006 1BFF	4 KB	Reserved
	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5005 0800 - 0x5006 07FF	61 KB	Reserved
	0x5005 0400 - 0x5005 07FF	1 KB	Reserved
	0x5005 0000 - 0x5005 03FF	1 KB	DCMI
	0x5004 0400 - 0x5004 FFFF	62 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	OTG_FS
	0x4800 2400 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 2000 - 0x4800 23FF	1 KB	GPIOI
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA

6.1.6 Power supply scheme

Figure 26. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Figure 28. V_{REFINT} versus temperature

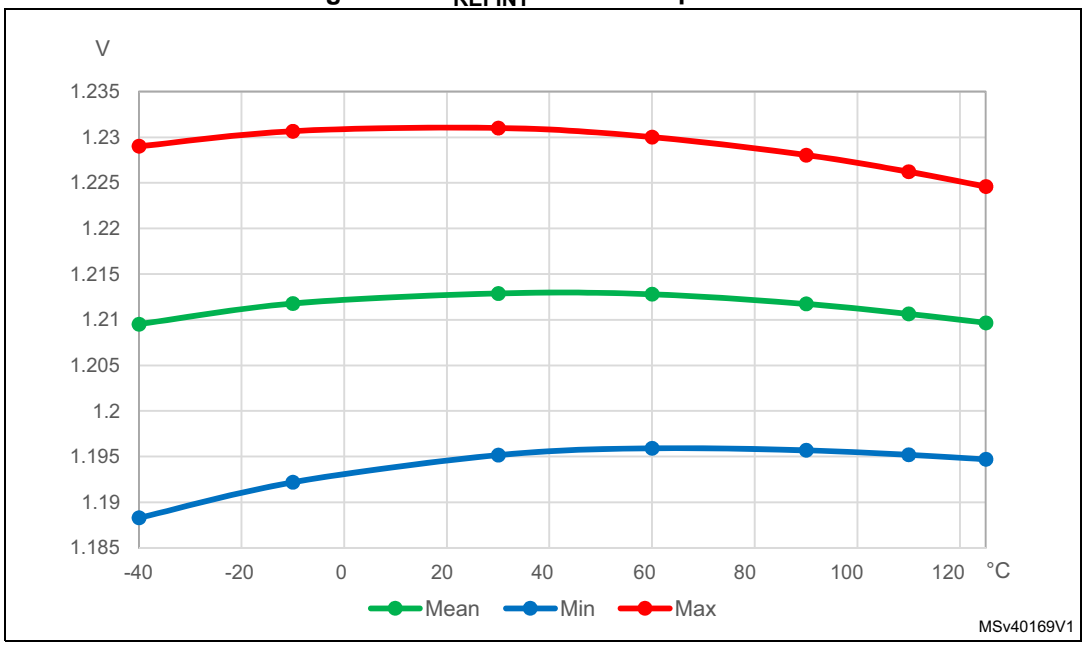


Table 37. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	VDD12	f_{HCLK}	Code	25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.05V	f_{HCLK}= 26 MHz	Reduced code	1.34	1.41	mA	51	54	µA/MHz
					Coremark	1.53	1.55		59	60	
					Dhrystone2.1	1.67	1.69		64	65	
					Fibonacci	1.43	1.53		55	59	
					While(1)	1.24	1.24		48	48	
			VDD12=1.10V	f_{HCLK}= 26 MHz	Reduced code	1.47	1.55	mA	56	60	µA/MHz
					Coremark	1.68	1.70		65	66	
					Dhrystone2.1	1.83	1.85		71	71	
					Fibonacci	1.57	1.68		61	65	
					While(1)	1.36	1.36		52	52	
				f_{HCLK}= 80 MHz	Reduced code	4.13	4.49	mA	52	56	µA/MHz
					Coremark	4.85	4.85		61	61	
					Dhrystone2.1	5.21	5.21		65	65	
					Fibonacci	4.49	5.03		56	63	
					While(1)	3.77	3.77		47	47	

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 53*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 19: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 53*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 52. Peripheral current consumption

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix	10.5	9.65	7.7	9	µA/MHz
	ADC independent clock domain	0.25	0.25	0.125	0.5	
	ADC AHB clock domain	3	2.75	2.6	3.5	
	CRC	0.835	0.875	0.835	0.5	
	DCMI	7.15	6.65	5.5	7	
	DMA1	3.15	2.9	2.5	2.5	
	DMA2	2.85	2.65	2.5	2.5	
	DMA2D	29.5	27.5	22.5	26	
	DMAMUX	5.35	5.15	4.15	4.5	
	FLASH	7.75	7.25	6.25	6.5	
	FMC	10.5	9.65	8.35	9.5	
	GFXMMU	5.6	5.25	4.6	4.5	
	GPIOA	1.85	1.75	1.4	1	
	GPIOB	1.75	1.65	1.35	1.5	
	GPIOC	2.4	2.25	1.9	2.5	
	GPIOD	1.85	1.75	1.45	2	
	GPIOE	1.85	1.75	1.45	1.5	
	GPIOF	2	1.75	1.55	2	
	GPIOG	2.25	2.15	1.8	2.5	
	GPIOH	2.35	2.15	1.8	2.5	

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 53* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 53. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		7	9	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	9.1	9.8	µs
			Wakeup clock HSI16 = 16 MHz	8.5	9.0	
		Range 2	Wakeup clock MSI = 24 MHz	18.8	19.7	
			Wakeup clock HSI16 = 16 MHz	17.6	18.3	
			Wakeup clock MSI = 4 MHz	23.9	25.7	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	1.9	2.5	
			Wakeup clock HSI16 = 16 MHz	2.6	2.9	
		Range 2	Wakeup clock MSI = 24 MHz	2.6	3.1	
			Wakeup clock HSI16 = 16 MHz	2.6	3.0	
			Wakeup clock MSI = 4 MHz	10.0	11.5	

Table 53. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	30.7	47.8	µs
			Wakeup clock MSI = 4 MHz	40.4	55.6	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	32.1	49.1	
			Wakeup clock MSI = 4 MHz	41.5	55.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	265.0	339.4	

1. Guaranteed by characterization results.

Table 54. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low- power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 55. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by characterization results.

Table 86. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 120. OctoSPI(1) characteristics in SDR mode(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(QCK)	OctoSPI clock frequency	1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	58	MHz
		2.7 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	86	
		1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 15 pF	-	-	66	
		1.71 V < V_{DD}< 3.6 V Voltage Range 2 C_{LOAD} = 20 pF	-	-	26	
$t_{w(CKH)}$	OctoSPI clock high and low time	Prescaler = 0	$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$			$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	0.5	-	-	
		Voltage Range 2	0	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	7.75	-	-	
		Voltage Range 2	10.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	2	3.5	
		Voltage Range 2	-	4	5.5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.