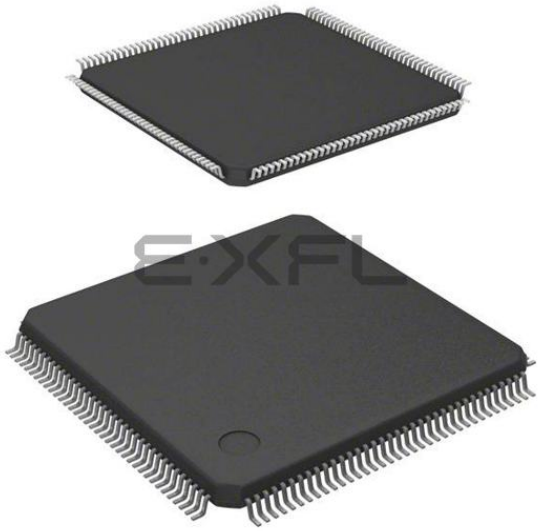

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	115
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r7zit6

3.4 Embedded Flash memory

The STM32L4Rxxx devices feature 2 Mbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 4 or 8 Kbytes (depending on the read access width).

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming:
  - In single bank mode, four areas can be selected with 8-Kbyte granularity.
  - In dual bank mode, two areas per bank can be selected with 4-Kbyte granularity.

Table 4. STM32L4R5xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Stop 0[5]	Range 1 Range 2	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]

3.25 LCD-TFT controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (red, green, blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels with the following features:

- Two displays layers with dedicated FIFO (64 x 32-bit)
- Color look-up table (CLUT) up to 256 colors (256 x 24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to four programmable interrupt events

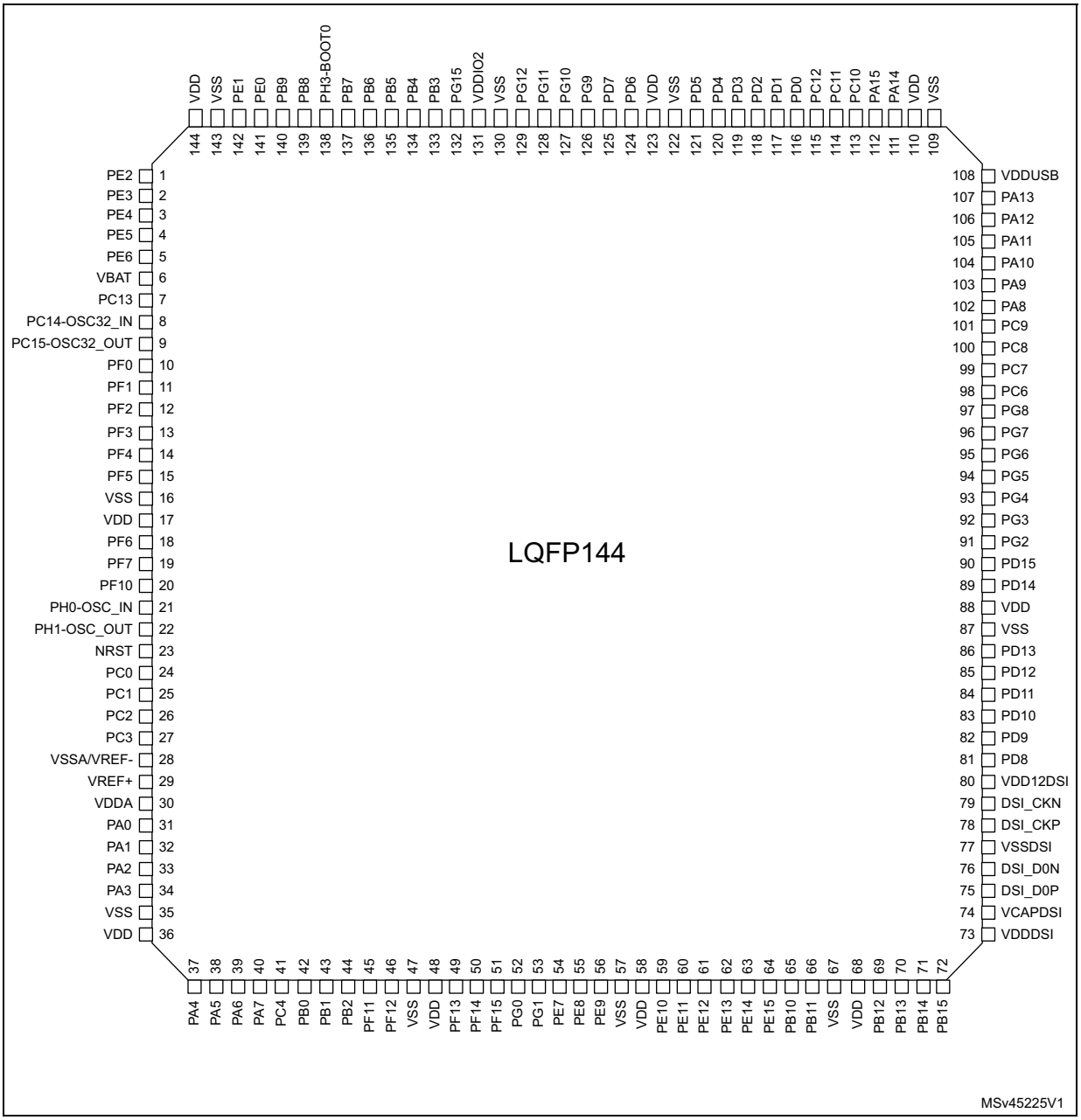
3.26 DSI Host (DSIHOST)

The DSI Host is a dedicated IP that interfaces with the MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

The interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI)
  - Used to transmit information in full bandwidth in the Adapted Command Mode (DBI) through a custom mode
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface
  - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli

Figure 13. STM32L4R9xx LQFP144 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L4Rxxx pin definitions

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	-	-	-	-	-	M11	M11	-	-	-	-	-	M11	VSS	S	-	-	-	-
-	-	-	-	-	-	C1	C1	-	-	-	-	-	C1	VDD	S	-	-	-	-
-	-	-	-	-	-	C3	C3	-	-	-	-	-	C3	PI11	I/O	FT	-	OCTOSPIM_P2_IO0, EVENTOUT	-
1	B2	B2	1	1	B11	D3	D3	1	1	C3	B11	B11	D3	PE2	I/O	FT_l	-	TRACECK, TIM3_ETR, SAI1_CK1, TSC_G7_IO1, LCD_R0, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
2	A1	A1	2	2	C11	D2	D2	2	2	B3	C11	C11	D2	PE3	I/O	FT_l	-	TRACED0, TIM3_CH1, OCTOSPIM_P1_DQS, TSC_G7_IO2, LCD_R1, FMC_A19, SAI1_SD_B, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
29	J4	J4	40	40	K9	L3	L3	27	37	K4	K9	K9	N2	PA4	I/O	TT_a	-	OCTOSPIM_P1_NCS, SPI1_NSS, SPI3_NSS, USART2_CK, DCMI_HSYNC, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC1_IN9, DAC1_OUT1
30	K4	K4	41	41	G8	K4	K4	28	38	L4	G8	G8	L3	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT	ADC1_IN10, DAC1_OUT2
31	L4	L4	42	42	J8	M4	M4	29	39	J4	J8	J8	L4	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, DCMI_PIXCLK, SPI1_MISO, USART3_CTS_NSS, LPUART1_CTS, OCTOSPIM_P1_IO3, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC1_IN11

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
54	K10	K10	76	76	J3	M12	M12	51	72	J9	J3	J3	L10	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	M2	L12	L12	-	-	-	M2	M2	-	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	52	73	-	-	-	M13	VDDDSI	S	-	-	-	-
-	-	-	-	-	-	L13	L13	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	53	74	L12	L3	L3	L13	VCAPDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	54	75	K11	L1	L1	L11	DSI_D0P	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	55	76	K12	L2	L2	L12	DSI_D0N	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	56	77	-	-	-	J13	VSSDSI	S	-	-	-	-
-	-	-	-	-	-	-	-	57	78	J11	K1	K1	K11	DSI_CKP	I/O	-	(3)	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
59	J10	J10	81	81	F4	K11	K11	-	85	G9	F4	F4	J8	PD12	I/O	FT_fl	-	TIM4_CH1, I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, LCD_R7, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
60	H12	H12	82	82	G3	K13	K13	-	86	G10	G3	G3	H8	PD13	I/O	FT_fl	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	83	83	G1	H12	H12	-	87	-	G1	G1	H12	VSS	S	-	-	-	-
-	-	-	84	84	G2	G13	G13	-	88	G12	G2	G2	H13	VDD	S	-	-	-	-
61	H11	H11	85	85	F3	K10	K10	63	89	G8	F3	F3	H11	PD14	I/O	FT	-	TIM4_CH3, LCD_B2, FMC_D0, EVENTOUT	-
62	H10	H10	86	86	F1	H11	H11	64	90	G7	F1	F1	H10	PD15	I/O	FT	-	TIM4_CH4, LCD_B3, FMC_D1, EVENTOUT	-
-	G10	G10	87	87	F2	J12	J12	-	91	F12	F2	F2	H9	PG2	I/O	FT_s	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT
	PH4	-	-	-	-	-	-	-	EVENTOUT
	PH5	-	-	DCMI_PIXCLK	-	-	-	-	EVENTOUT
	PH6	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PH7	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PH8	-	-	DCMI_HSYNC	-	-	-	-	EVENTOUT
	PH9	-	-	DCMI_D0	-	-	-	-	EVENTOUT
	PH10	-	-	DCMI_D1	-	-	-	-	EVENTOUT
	PH11	-	-	DCMI_D2	-	-	-	-	EVENTOUT
	PH12	-	-	DCMI_D3	-	-	-	-	EVENTOUT
	PH13	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-	DCMI_D4	-	-	-	-	EVENTOUT
	PH15	-	-	DCMI_D11	-	-	-	-	EVENTOUT

5 Memory mapping

Figure 23. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map

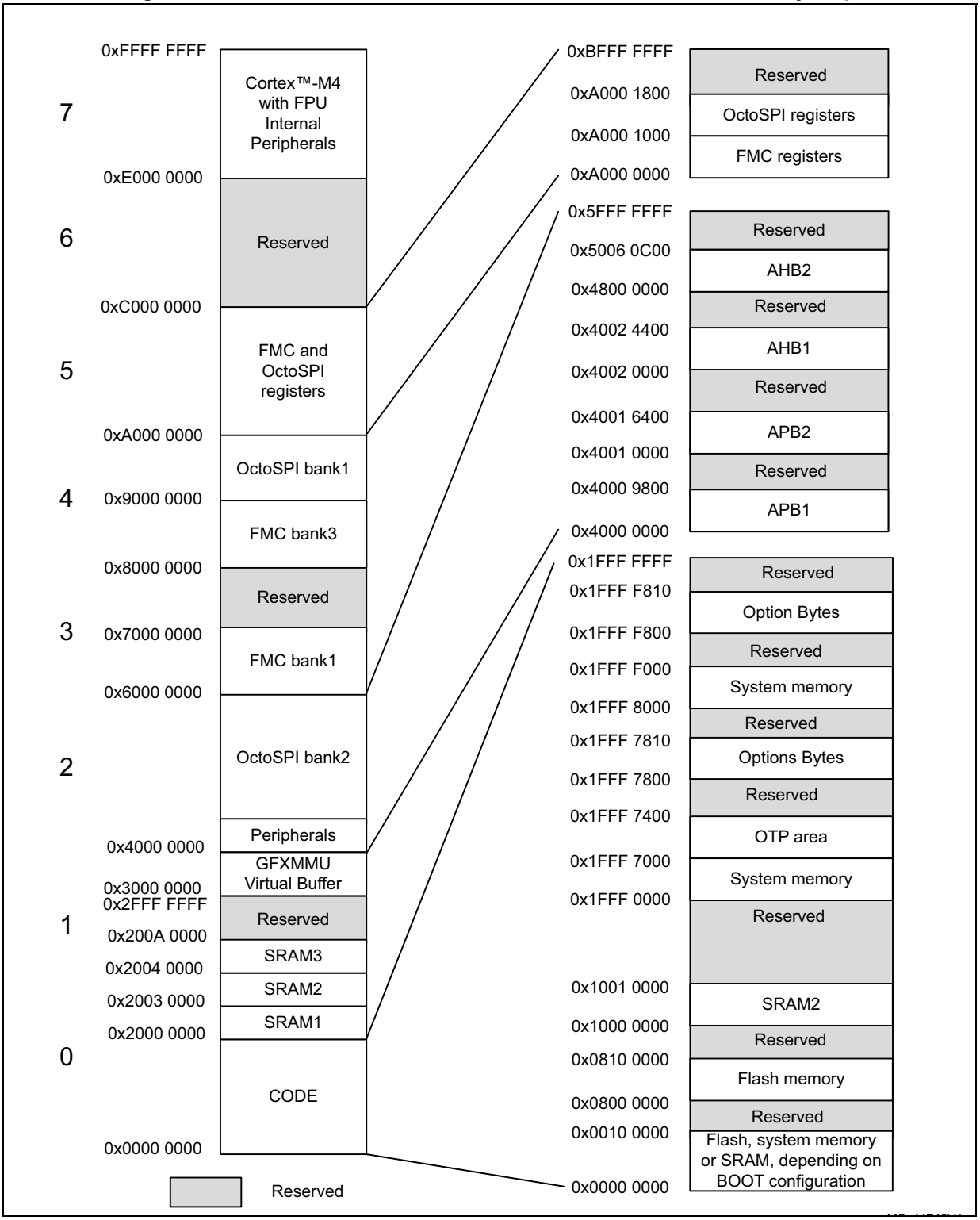


Table 30. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	4.00	4.40	5.55	7.20	10.0	4.60	5.5	7.5	11.0	17.0	mA
				16 MHz	2.65	3.05	4.15	5.80	8.75	3.10	4.0	6.0	9.3	16.0	
				8 MHz	1.50	1.85	2.90	4.45	7.25	1.80	2.6	4.6	7.9	14.0	
				4 MHz	0.875	1.25	2.35	3.95	6.90	1.20	1.9	3.9	7.2	14.0	
				2 MHz	0.565	0.925	2.05	3.65	6.55	0.77	1.6	3.6	6.8	13.0	
				1 MHz	0.405	0.770	1.90	3.50	6.40	0.60	1.4	3.4	6.7	13.0	
				100 KHz	0.265	0.635	1.75	3.35	6.25	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.5	19.5	21.0	23.5	27.0	21.00	23.0	26.0	30.0	38.0	
			Range 1 Normal Mode	80 MHz	13.0	13.5	15.5	17.5	21.0	15.00	17.0	19.0	23.0	30.0	
				72 MHz	12.0	12.5	14.0	16.0	20.0	14.00	15.0	18.0	22.0	29.0	
				64 MHz	10.5	11.0	12.5	15.0	18.5	12.00	14.0	16.0	20.0	28.0	
				48 MHz	8.75	9.30	11.0	13.0	16.5	9.80	12.0	14.0	18.0	25.0	
				32 MHz	6.20	6.70	8.20	10.0	14.0	7.00	8.2	11.0	15.0	22.0	
				24 MHz	4.70	5.20	6.70	10.5	12.5	5.40	6.5	9.0	13.0	20.0	
				16 MHz	3.35	3.85	5.25	7.30	11.0	3.90	4.9	7.4	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	595	1000	2300	4150	7350	810.00	1700	4100	7800	15000	µA
				1 MHz	370	800	2100	3950	7150	560.00	1500	3900	7600	14000	
				400 KHz	245	705	2000	3850	7050	420.00	1400	3800	7500	14000	
				100 KHz	230	655	1950	3800	7000	400.00	1400	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 34. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.75	4.85	6.45	9.30	4.70	5.6	7.6	11.0	17.0	mA
				16 MHz	2.20	2.55	3.65	5.20	8.10	3.20	4.1	6.1	9.4	16.0	
				8 MHz	1.20	1.55	2.65	4.25	7.10	1.70	2.7	4.7	8.0	14.0	
				4 MHz	0.74	1.10	2.15	3.75	6.60	1.20	2.0	4.0	7.3	14.0	
				2 MHz	0.49	0.85	1.95	3.50	6.35	0.79	1.6	3.6	6.9	13.0	
				1 MHz	0.37	0.73	1.80	3.40	6.20	0.61	1.4	3.4	6.7	13.0	
				100 KHz	0.26	0.62	1.70	3.25	6.10	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.00	18.50	20.00	22.50	26.50	19.00	21.0	24.0	28.0	36.0(2)	
			Range 1 Normal Mode	80 MHz	11.00	11.50	13.50	15.50	19.00	15.00	16.0	19.0	23.0	30.0(2)	
				72 MHz	10.00	10.50	12.00	14.00	18.00	13.00	15.0	18.0	22.0	29.0	
				64 MHz	9.10	9.60	11.00	13.00	16.50	12.00	13.0	16.0	20.0	27.0	
				48 MHz	7.20	7.70	9.20	11.00	14.50	11.00	12.0	15.0	19.0	26.0	
				32 MHz	4.90	5.40	6.85	8.80	12.50	7.30	8.5	12.0	16.0	23.0	
				24 MHz	3.75	4.25	5.65	7.65	11.00	5.60	6.7	9.3	14.0	21.0	
				16 MHz	2.60	3.10	4.50	6.45	9.90	4.10	5.2	7.7	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable FLASH in power-down		2 MHz	435	885	2150	3950	7100	800	1800	4200	7800	15000	µA
				1 MHz	300	745	2000	3800	6950	580	1600	4000	7600	14000	
				400 KHz	225	655	1900	3700	6850	420	1400	3800	7500	14000	
				100 KHz	180	620	1900	3650	6800	370	1400	3700	7500	14000	

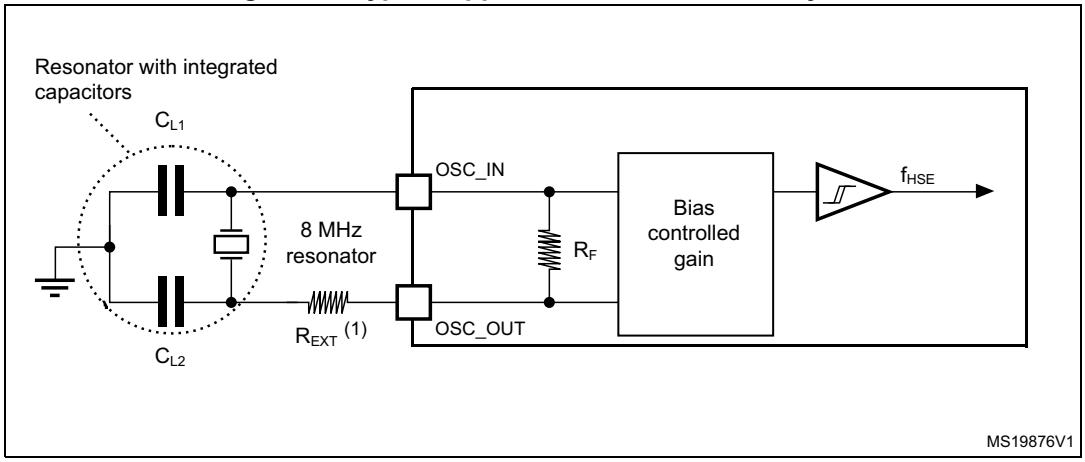
1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 53. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	12.6	14.5	µs
			Wakeup clock HSI16 = 16 MHz	12.2	14.0	
		Range 2	Wakeup clock MSI = 24 MHz	22.1	24.1	
			Wakeup clock HSI16 = 16 MHz	21.3	23.3	
			Wakeup clock MSI = 4 MHz	25.1	27.1	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.3	7.0	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
		Range 2	Wakeup clock MSI = 24 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
			Wakeup clock MSI = 4 MHz	10.9	12.6	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	20.4	22.4	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			16.8	19.0	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	13.1	14.8	µs
			Wakeup clock HSI16 = 16 MHz	12.6	14.4	
		Range 2	Wakeup clock MSI = 24 MHz	22.6	24.6	
			Wakeup clock HSI16 = 16 MHz	21.7	23.7	
			Wakeup clock MSI = 4 MHz	25.8	27.9	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
		Range 2	Wakeup clock MSI = 24 MHz	6.4	8.0	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
			Wakeup clock MSI = 4 MHz	11.9	13.6	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

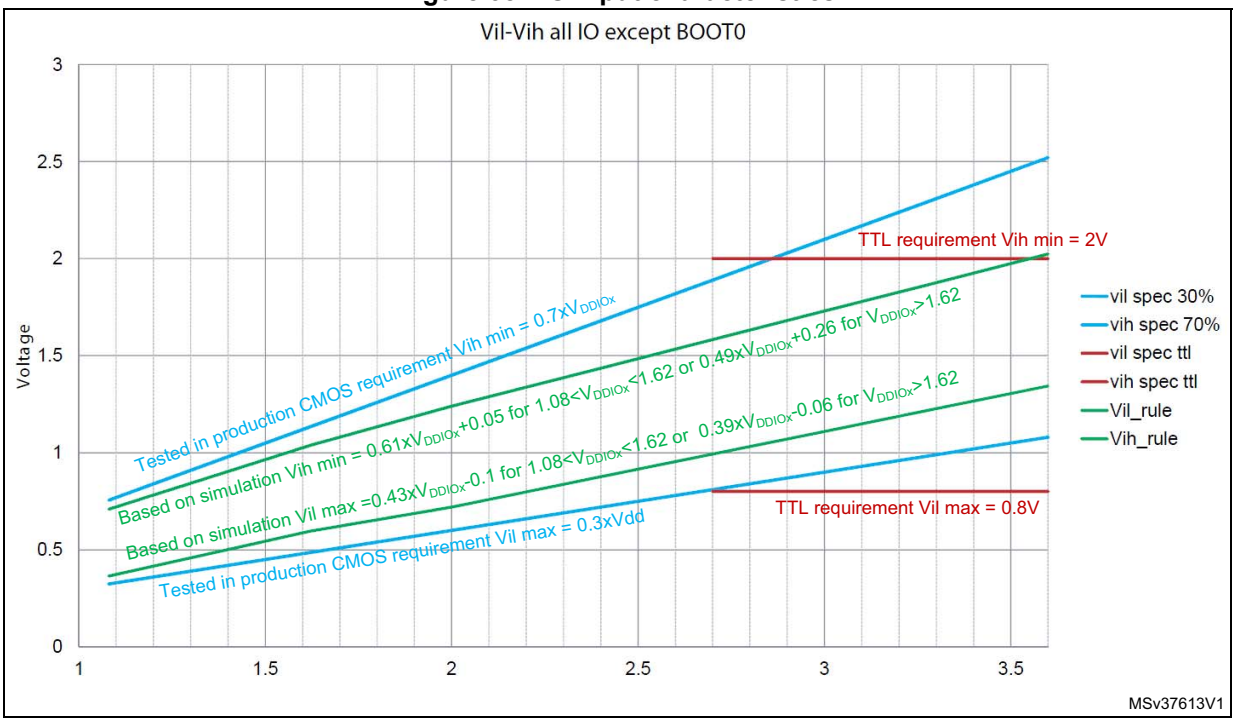
Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 59*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

1. Refer to *Figure 38: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. Max(V_{DDXXX}) is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table*.
5. All TX_xx IO except FT_lu, FT_u, PB2 and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:
   $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to I_{bias} in *Table 92: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 38* for standard I/Os, and in *Figure 38* for 5 V tolerant I/Os.

Figure 38. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

6.3.26 Temperature sensor characteristics

Table 93. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.27 V_{BAT} monitoring characteristics

Table 94. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 95. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

Table 101. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	13	15	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1	-	10	23	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V2	-	13	25	
		Slave mode 1.08 V < V_{DD} < 1.32 V(3)	-	29	39	
$t_{v(MO)}$		Master mode	-	2	4	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7	-	-	
		Slave mode 1.08 < V_{DD} < 1.32 V(3)	26	-	-	
$t_{h(MO)}$		Master mode	1	-	-	

1. Guaranteed by characterization results.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high-phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.
3. SPI mapped on Port G.

Figure 44. SPI timing diagram - slave mode and CPHA = 0

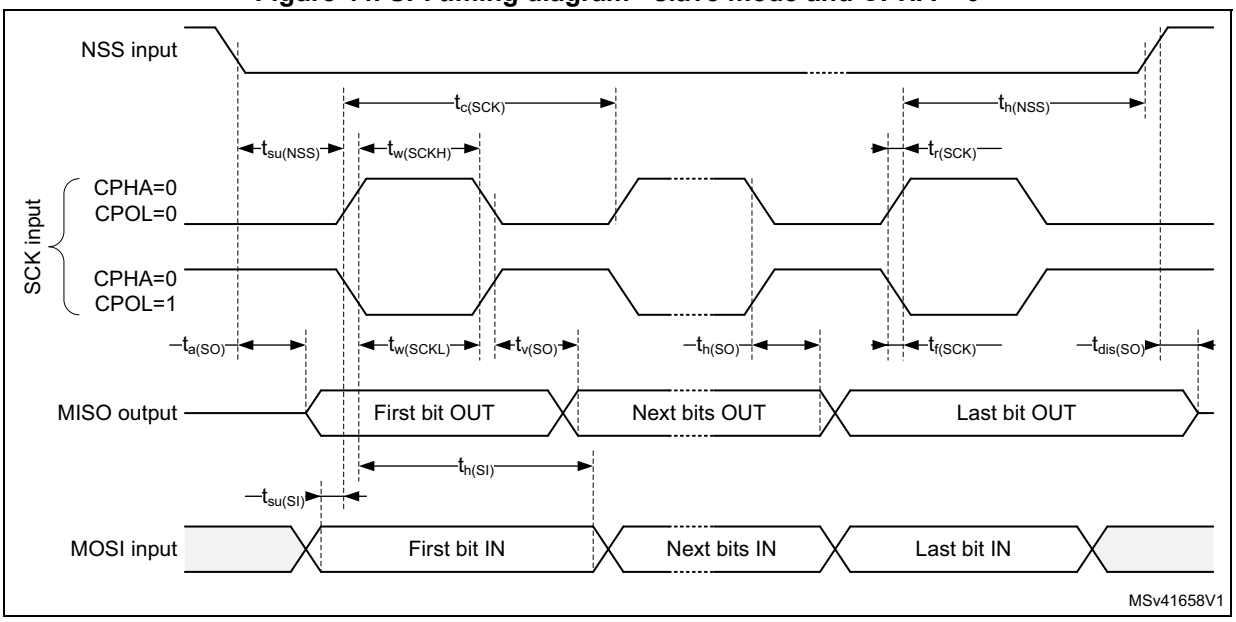


Table 122. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and Hyperbus (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
$t_{w(CKH)}$	OctoSPI clock high and low time	-		$t_{(CK)}/2-1$	-	$t_{(CK)}/2+0.5$	ns
$t_{w(CKL)}$				$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2+0.5$	
$t_{v(CK)}$	Clock valid time	-		-	-	$t_{(CK)}+1$	
$t_{h(CK)}$	Clock hold time	-		$t_{(CK)}/2-0.5$	-	-	
$t_{w(CS)}$	Chip select high time	-		3 x $t_{(CK)}$	-	-	
$t_{v(DQ)}$	Data input vallid time	-		0	-	-	
$t_{v(DS)}$	Data storbe input valid time	-		0	-	-	
$t_{h(DS)}$	Data storbe input hold time	-		0	-	-	
$t_{v(RWDS)}$	Data storbe output valid time	-		-	-	3 x $t_{(CK)}$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	Voltage Range 1		-3.5	-	$t_{(CK)}/2-5.75$(3)	
		Voltage Range 2		-5.5	-	$t_{(CK)}/2-9$(3)	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	Voltage Range 1		5.75	-	-	
		Voltage Range 2		9	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	-	4.5	6	ns
			DHQC = 1 Pres=1,2 ...		tpclk/4+1.5	tpclk/4+2.25	
		Voltage Range 2	DHQC = 0		8	11	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	0.5	-	-	
			DHQC = 1 Pres=1,2 ...	tpclk/4-1.75	-	-	
		Voltage Range 2	DHQC = 0	0.75	-	-	

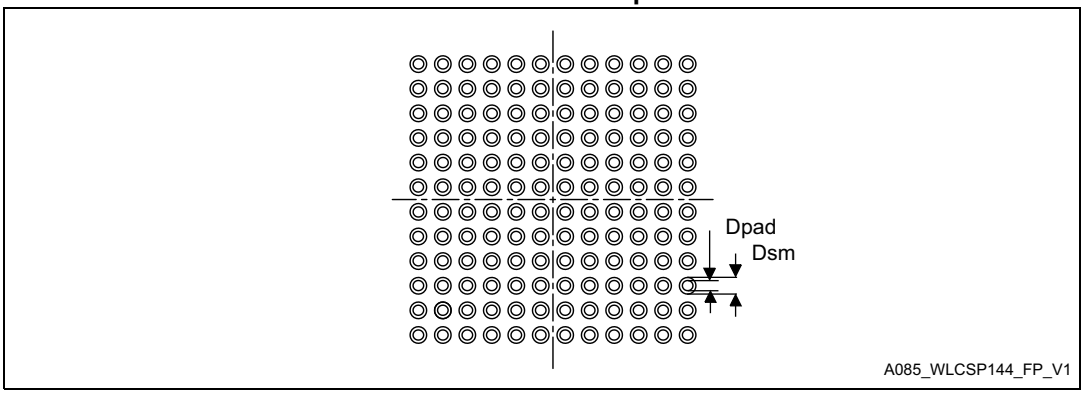
1. Guaranteed by characterization results.
2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.
3. Data input setup time maximum does not take into account Data level switching duration.

Table 132. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[2]	-	-	0.0010	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	5.22	5.24	5.26	0.205	0.206	0.207
E	5.22	5.24	5.26	0.205	0.206	0.207
e	-	0.40	-	-	0.016	-
e1	-	4.40	-	-	0.173	-
e2	-	4.40	-	-	0.173	-
F	-	0.420[3]	-	-	0.0165	-
G	-	0.420[4]	-	-	0.0165	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. A3 value is guaranteed by technology design value.
3. This value is calculated from over value D and e1.
4. This value is calculated from over value E and e2.

Figure 83. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, recommended footprint



1. Dimensions are expressed in millimeters.