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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r9vgt6

Table 2. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx features and peripheral counts (continued)

Peripheral	R5VI R5VG	R7VI	R9VI R9VG	R5QI R5QG	R5ZI R5ZG	R7ZI	R9ZI R9ZG	R5AI R5AG	R7AI	R9AI R9AG
LCD - TFT	No	Yes		No		Yes		No	Yes	
MIPI DSI Host(2)	No		Yes	No			Yes	No		Yes
Random number generator	Yes									
GPIOs(3) Wakeup pins Nb of I/Os down to 1.08 V	83 5 0		77 4 0	110 5 14	115 5 14		112 5 11	140 5 14		131 4 13
Capacitive sensing Number of channels	21		18	24						
12-bit ADCs Number of channels	1									
	16		14	16						14
12-bit DAC Number of channels	2 2									
Internal voltage reference buffer	Yes									
Analog comparator	2									
Operational amplifiers	2									
Max. CPU frequency	120 MHz									
Operating voltage (V_{DD})	1.71 to 3.6 V									
Operating voltage (V_{DD12})	1.05 to 1.32 V									
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C									
Packages	LQFP100			UFBGA132	LQFP144 WLCSP144	LQFP144	LQFP144, UFBGA144 WLCSP144	UFBGA169		

1. For the LQFP100 package, only FMC bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The DSI Host interface is only available on the STM32L4R9xx sales types.
3. In the case of an external SMPS package type is used, 2 GPIOs are replaced by V_{DD12} pins to connect the SMPS power supplies hence reducing the number of available GPIOs by 2.

3.25 LCD-TFT controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (red, green, blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels with the following features:

- Two displays layers with dedicated FIFO (64 x 32-bit)
- Color look-up table (CLUT) up to 256 colors (256 x 24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to four programmable interrupt events

3.26 DSI Host (DSIHOST)

The DSI Host is a dedicated IP that interfaces with the MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

The interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI)
  - Used to transmit information in full bandwidth in the Adapted Command Mode (DBI) through a custom mode
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface
  - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli

- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - Storage of minimum and maximum values of final conversion data
  - Refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “Regular” or “injected” conversions:
  - “Regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “Injected” conversions for precise timing and with high conversion priority

3.28 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.29 Digital camera interface (DCMI)

The STM32L4Rxxx devices embed a camera interface that can connect with any camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface in order to receive video data.

The camera interface can sustain a data transfer rate up to 54 Mbytes/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication of 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image.

3.30 Timers and watchdogs

The STM32L4Rxxx devices include two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer.

The *Table 10* below compares the features of the advanced control, general-purpose and basic timers.

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 7: Clock tree*
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 11. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop 0, Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

Figure 15. STM32L4R9xx UFBGA144 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PE0	PB9	PH3-BOOT0	PB4	VDDIO2	VSS	PD3	PC11	PA14	VDD	VSS
B	VBAT	VDD	PE3	PB8	PB5	PB3	PD6	PD1	PA15	PA13	PA12	PA11
C	VSS	PE5	PE2	PE1	PB7	PG13	PD4	PD0	PC10	PA10	VDDUSB	PC9
D	PC14-OSC32_IN	PC15-OSC32_OUT	PE4	PE6	PB6	PG12	PD5	PD2	PC12	PA9	PA8	PC6
E	PF2	PF1	PF0	PC13	PF3	PG10	PD7	PG8	PC7	PC8	PG7	VDDIO2
F	PF8	PF6	PF4	PF5	PF7	PG9	PG3	PG5	PG6	PG4	VSS	PG2
G	VDD	VSS	PF10	PF9	PF12	PE7	PD15	PD14	PD12	PD13	PD11	VDD
H	PH0-OSC_IN	PH1-OSC_OUT	PC0	PC2	PB2	PF15	PE11	PD10	PD9	PD8	DSI_D1P	DSI_D1N
J	NRST	PC1	PC3	PA6	PB1	PF13	PE9	PE13	PB15	VSSDSI	DSI_CKP	DSI_CKN
K	VSSA/VREF-	VREF+	PA0	PA4	PC5	PF11	PE8	PE15	PB11	PB14	DSI_D0P	DSI_D0N
L	VDDA	PA1	PA2	PA5	PC4	VSS	PG0	PE10	PB10	PB12	VDD	VCAPDSI
M	VSS	VDD	PA3	PA7	PB0	VDD	PF14	PG1	PE12	PE14	PB13	VSS

MSv38491V4

1. The above figure shows the package top view.

Figure 16. STM32L4R9xx WLCSP144 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PA14	PA15	PD0	PD5	VDD	PG12	VDDIO2	PB7	PE0	PE1	VSS
B	VDD	VDDUSB	PA13	PC12	PD2	VSS	PG10	PB3	PH3-BOOT0	PB9	PE2	VDD
C	PA11	PA12	PC10	PC11	PD1	PD4	PG9	PB4	PB6	PB8	PE3	PE4
D	PC8	PC9	PA8	PA9	PA10	PD3	PD7	PG13	PE5	PE6	PC13	VSS
E	PG7	PG8	VDDIO2	PC6	PG6	PC7	PD6	PB5	PF0	VBAT	PC14-OSC32_IN	PC15-OSC32_OUT
F	PD15	PG2	PD14	PD12	PG3	PG4	PG5	PF1	PF5	PF4	PF3	PF2
G	VSS	VDD	PD13	PD11	PD10	PE9	PF14	PA5	PF7	PF6	VSS	VDD
H	PD9	PD8	PB14	PB13	PE14	PE8	PB1	PA2	PC2	PF10	NRST	PH0-OSC_IN
J	DSI_D1N	DSI_D1P	PB15	PB12	PE13	PF15	PB2	PA6	PA0	PC3	PC0	PH1-OSC_OUT
K	DSI_CKP	DSI_CKN	VSSDSI	PE15	PE10	PG0	PF11	PC5	PA4	PA1	VSSA/VREF-	PC1
L	DSI_D0P	DSI_D0N	VCAPDSI	PB10	PE11	PG1	VDD	PF12	PC4	PA3	VREF+	VDDA
M	VDD	VDD	VSS	PB11	PE12	PE7	PF13	VSS	PB0	PA7	VDD	VSS

MSv42219V2

1. The above figure shows the package top view

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
45	M11	M11	67	67	H5	K8	K8	42	63	M10	H5	H5	K7	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, OCTOSPIM_P1_IO2, LCD_G7, FMC_D11, EVENTOUT	-
46	M12	M12	68	68	K4	J8	J8	43	64	K8	K4	K4	J7	PE15	I/O	FT	-	TIM1_BKIN, SPI1_MOSI, OCTOSPIM_P1_IO3, LCD_R2, FMC_D12, EVENTOUT	-
47	L10	L10	69	69	L4	N9	N9	44	65	L9	L4	L4	N9	PB10	I/O	FT_fl	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, DFSDM1_DATIN7, USART3_TX, LPUART1_RX, TSC_SYNC, OCTOSPIM_P1_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
76	A10	A10	109	109	A2	A10	A10	78	111	A10	A2	A2	A10	PA14 (JTCK/ SWCLK)	I/O	FT	(4)	JTCK/SWCLK, LPTIM1_OUT, I2C1_SMBA, I2C4_SMBA, OTG_FS_SOF, SAI1_FS_B, EVENTOUT	-
77	A9	A9	110	110	A3	A9	A9	79	112	B9	A3	A3	A9	PA15 (JTDI)	I/O	FT	(4)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, UART4_RTS_DE, TSC_G3_IO1, SAI2_FS_B, EVENTOUT	-
78	B11	B11	111	111	C3	D9	D9	80	113	C9	C3	C3	D9	PC10	I/O	FT	-	TRACED1, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, DCMI_D8, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPIM_P1_DQS	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-	DFSDM1_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-	DFSDM1_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM1_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM1_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM1_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM1_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN	-	SPI1_MOSI	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port G	PG0	-	-	-	-	-	OCTOSPIM_P2_IO4	-	-
	PG1	-	-	-	-	-	OCTOSPIM_P2_IO5	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPIM_P1_DQS	I2C3_SMBA	-	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	OCTOSPIM_P2_DQS	DFSDM1_CKOUT	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	OCTOSPIM_P2_IO6	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	OCTOSPIM_P2_IO7	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPIM_P1_IO5	-	-	SPI3_MOSI	USART1_CTS_NSS
	PG12	-	LPTIM1_ETR	-	-	-	OCTOSPIM_P2_NCS	SPI3_NSS	USART1_RTS_DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	OCTOSPIM_P2_DQS	-	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port C	PC0	LPUART1_RX	-	-	-	-	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	-	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	TSC_G4_IO1	DCMI_D0	LCD_R0	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_ D123DIR	TSC_G4_IO2	DCMI_D1	LCD_R1	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00- 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

6.3.4 Embedded voltage reference

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 53* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 53. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		7	9	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	9.1	9.8	µs
			Wakeup clock HSI16 = 16 MHz	8.5	9.0	
		Range 2	Wakeup clock MSI = 24 MHz	18.8	19.7	
			Wakeup clock HSI16 = 16 MHz	17.6	18.3	
			Wakeup clock MSI = 4 MHz	23.9	25.7	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	1.9	2.5	
			Wakeup clock HSI16 = 16 MHz	2.6	2.9	
		Range 2	Wakeup clock MSI = 24 MHz	2.6	3.1	
			Wakeup clock HSI16 = 16 MHz	2.6	3.0	
			Wakeup clock MSI = 4 MHz	10.0	11.5	

6.3.8 Internal clock source characteristics

The parameters given in *Table 60* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 60. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

High-speed internal 48 MHz (HSI48) RC oscillator

Table 62. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

The maximum value of R_{AIN} can be found in *Table 83: Maximum ADC RAIN*.

Table 83. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

Figure 41. ADC accuracy characteristics

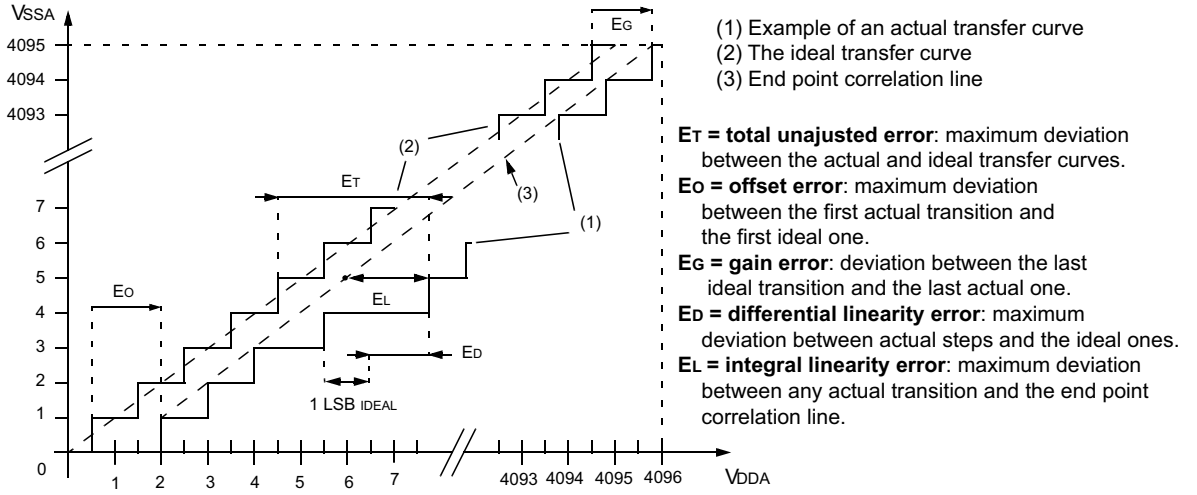
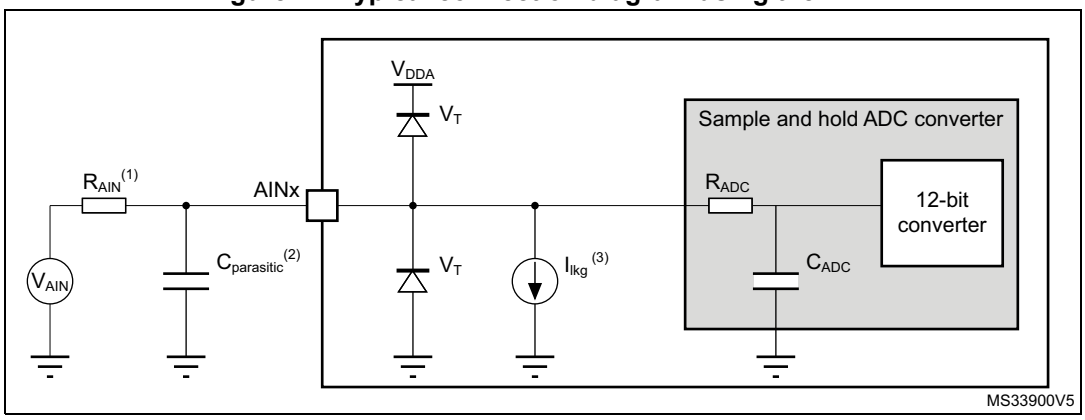


Figure 42. Typical connection diagram using the ADC



1. Refer to *Table 82: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 76: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 76: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 26: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.23 Voltage reference buffer characteristics

Table 90. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.046(3)	2.048	2.049(3)	
			V_{RS} = 1	2.498(3)	2.5	2.502(3)	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < TJ < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(4)		-	300	350	µs
		CL = 1.1 µF(4)		-	500	650	
		CL = 1.5 µF(4)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5)	-	-	-	8	-	mA

6.3.33 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 123* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 21*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Figure 68. DCMI timing diagram

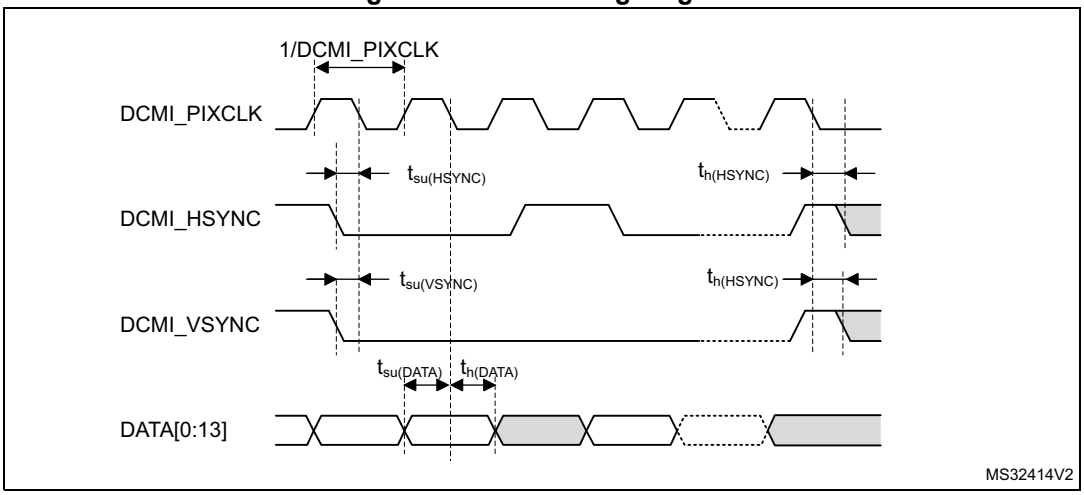


Table 123. DCMI characteristics(1)

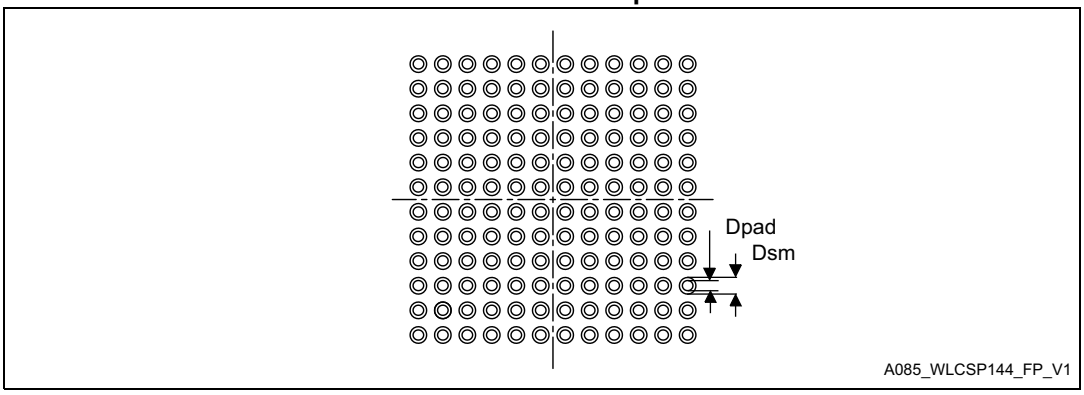
Symbol	Parameter	Condition	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	1.71 < VDD < 3.6 Voltage range V1	-	48	MHz
		1.71 < VDD < 3.6 Voltage range V2	-	10	
D_{pixel}	Pixel clock input duty cycle	-	30	70	%

Table 132. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[2]	-	-	0.0010	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	5.22	5.24	5.26	0.205	0.206	0.207
E	5.22	5.24	5.26	0.205	0.206	0.207
e	-	0.40	-	-	0.016	-
e1	-	4.40	-	-	0.173	-
e2	-	4.40	-	-	0.173	-
F	-	0.420[3]	-	-	0.0165	-
G	-	0.420[4]	-	-	0.0165	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. A3 value is guaranteed by technology design value.
3. This value is calculated from over value D and e1.
4. This value is calculated from over value E and e2.

Figure 83. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, recommended footprint



1. Dimensions are expressed in millimeters.