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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 77 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 640K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 14x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r9vit6 |

# Contents

- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited:
  - In single bank mode, two areas can be selected with 128-bit granularity.
  - In dual bank mode, one area per bank can be selected with 64-bit granularity.

  An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

## 3.5 Embedded SRAM

The STM32L4R5xx, STM32L4R7xx and STM32L4R9xx devices feature 640 Kbytes of embedded SRAM. This SRAM is split into three blocks:

- 192 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x1000 0000 with hardware parity check (SRAM2).
  This memory is also mapped at address 0x2003 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the ICode/DCode buses for maximum performance.
  These 64 Kbytes SRAM can also be retained in Standby mode.
  The SRAM2 can be write-protected with 1 Kbyte granularity.
- 384 Kbytes mapped at address 0x2004 0000 - (SRAM3).

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

### 3.10.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from $V_{DD}$ when there is no external battery and when an external supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when $V_{DD}$ is not present. An internal VBAT battery charging circuit is embedded and can be activated when $V_{DD}$ is present.

*Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.*

## 3.11 Interconnect matrix

Several peripherals have direct connections between them, which allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, Low-power run and Sleep, Stop 0, Stop 1 and Stop 2 modes. See *Table 6* for more details.

**Table 6. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx peripherals interconnect matrix**

| Interconnect source | Interconnect destination | Interconnect action | Run | Sleep | Low-power run | Low-power sleep | Stop 0 / Stop 1 | Stop 2 |
|---|---|---|---|---|---|---|---|---|
| TIMx | TIMx | Timers synchronization or chaining | Y | Y | Y | Y | - | - |
| | ADC<br>DACx<br>DFSDM1 | Conversion triggers | Y | Y | Y | Y | - | - |
| | DMA | Memory to memory transfer trigger | Y | Y | Y | Y | - | - |
| | COMPx | Comparator output blanking | Y | Y | Y | Y | - | - |
| COMPx | TIM1, 8<br>TIM2, 3 | Timer input channel, trigger, break from analog signals comparison | Y | Y | Y | Y | - | - |
| | LPTIMERx | Low-power timer triggered by analog signals comparison | Y | Y | Y | Y | Y | Y (1) |
| ADCx | TIM1, 8 | Timer triggered by analog watchdog | Y | Y | Y | Y | - | - |
| RTC | TIM16 | Timer input channel from RTC events | Y | Y | Y | Y | - | - |
| | LPTIMERx | Low-power timer triggered by RTC alarms or tampers | Y | Y | Y | Y | Y | Y (1) |
| All clocks sources (internal and external) | TIM2<br>TIM15, 16, 17 | Clock source used as input channel for RC measurement and trimming | Y | Y | Y | Y | - | - |

## 3.19 Analog-to-digital converter (ADC)

The device embeds a successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

### 3.19.1 Temperature sensor

The temperature sensor (TS) generates a voltage $V_{TS}$ that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 10. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1, TIM8 | 16-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | 3 |
| General-purpose | TIM2, TIM5 | 32-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM3, TIM4 | 16-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 |
| General-purpose | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### 3.30.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.30.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

### Figure 15. STM32L4R9xx UFBGA144 ballout(1)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | PE0 | PB9 | PH3-BOOT0 | PB4 | VDDIO2 | VSS | PD3 | PC11 | PA14 | VDD | VSS |
| B | VBAT | VDD | PE3 | PB8 | PB5 | PB3 | PD6 | PD1 | PA15 | PA13 | PA12 | PA11 |
| C | VSS | PE5 | PE2 | PE1 | PB7 | PG13 | PD4 | PD0 | PC10 | PA10 | VDDUSB | PC9 |
| D | PC14-OSC32_IN | PC15-OSC32_OUT | PE4 | PE6 | PB6 | PG12 | PD5 | PD2 | PC12 | PA9 | PA8 | PC6 |
| E | PF2 | PF1 | PF0 | PC13 | PF3 | PG10 | PD7 | PG8 | PC7 | PC8 | PG7 | VDDIO2 |
| F | PF8 | PF6 | PF4 | PF5 | PF7 | PG9 | PG3 | PG5 | PG6 | PG4 | VSS | PG2 |
| G | VDD | VSS | PF10 | PF9 | PF12 | PE7 | PD15 | PD14 | PD12 | PD13 | PD11 | VDD |
| H | PH0-OSC_IN | PH1-OSC_OUT | PC0 | PC2 | PB2 | PF15 | PE11 | PD10 | PD9 | PD8 | DSI_D1P | DSI_D1N |
| J | NRST | PC1 | PC3 | PA6 | PB1 | PF13 | PE9 | PE13 | PB15 | VSSDSI | DSI_CKP | DSI_CKN |
| K | VSSA/VREF- | VREF+ | PA0 | PA4 | PC5 | PF11 | PE8 | PE15 | PB11 | PB14 | DSI_D0P | DSI_D0N |
| L | VDDA | PA1 | PA2 | PA5 | PC4 | VSS | PG0 | PE10 | PB10 | PB12 | VDD | VCAPDSI |
| M | VSS | VDD | PA3 | PA7 | PB0 | VDD | PF14 | PG1 | PE12 | PE14 | PB13 | VSS |

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1. The above figure shows the package top view.

### Figure 16. STM32L4R9xx WLCSP144 ballout(1)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | PA14 | PA15 | PD0 | PD5 | VDD | PG12 | VDDIO2 | PB7 | PE0 | PE1 | VSS |
| B | VDD | VDDUSB | PA13 | PC12 | PD2 | VSS | PG10 | PB3 | PH3-BOOT0 | PB9 | PE2 | VDD |
| C | PA11 | PA12 | PC10 | PC11 | PD1 | PD4 | PG9 | PB4 | PB6 | PB8 | PE3 | PE4 |
| D | PC8 | PC9 | PA8 | PA9 | PA10 | PD3 | PD7 | PG13 | PE5 | PE6 | PC13 | VSS |
| E | PG7 | PG8 | VDDIO2 | PC6 | PG6 | PC7 | PD6 | PB5 | PF0 | VBAT | PC14-OSC32_IN | PC15-OSC32_OUT |
| F | PD15 | PG2 | PD14 | PD12 | PG3 | PG4 | PG5 | PF1 | PF5 | PF4 | PF3 | PF2 |
| G | VSS | VDD | PD13 | PD11 | PD10 | PE9 | PF14 | PA5 | PF7 | PF6 | VSS | VDD |
| H | PD9 | PD8 | PB14 | PB13 | PE14 | PE8 | PB1 | PA2 | PC2 | PF10 | NRST | PH0-OSC_IN |
| J | DSI_D1N | DSI_D1P | PB15 | PB12 | PE13 | PF15 | PB2 | PA6 | PA0 | PC3 | PC0 | PH1-OSC_OUT |
| K | DSI_CKP | DSI_CKN | VSSDSI | PE15 | PE10 | PG0 | PF11 | PC5 | PA4 | PA1 | VSSA/VREF- | PC1 |
| L | DSI_D0P | DSI_D0N | VCAPDSI | PB10 | PE11 | PG1 | VDD | PF12 | PC4 | PA3 | VREF+ | VDDA |
| M | VDD | VDD | VSS | PB11 | PE12 | PE7 | PF13 | VSS | PB0 | PA7 | VDD | VSS |

MSv42219V2

1. The above figure shows the package top view

**Table 15. STM32L4Rxxx pin definitions (continued)**

| Pin number | | | | | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4R5xxx, STM32L4R7xxx | | | | | | | | STM32L4R9xxx | | | | | | | | | | | |
| LQFP100 | BGA132_SMPS | BGA132 | LQFP144_SMPS | LQFP144 | WLCSP144 | UFBGA169_SMPS | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144_SMPS | WLCSP144 | UFBGA169 | | | | | | |
| - | M4 | M4 | - | - | - | N4 | N4 | - | - | - | - | - | - | OPAMP2_VINM | I | TT | - | - | - |
| 32 | J5 | J5 | 43 | 43 | M10 | L4 | L4 | 30 | 40 | M4 | M10 | M10 | M4 | PA7 | I/O | FT_fla | - | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, OCTOSPIM_P1_IO2, TIM17_CH1, EVENTOUT | OPAMP2_VINM, ADC1_IN12 |
| 33 | K5 | K5 | 44 | 44 | L9 | H5 | H5 | 31 | 41 | L5 | L9 | L9 | K4 | PC4 | I/O | FT_a | - | USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT | COMP1_INM, ADC1_IN13 |
| 34 | L5 | L5 | 45 | 45 | K8 | J5 | J5 | - | - | K5 | K8 | K8 | - | PC5 | I/O | FT_a | - | SAI1_D3, USART3_RX, EVENTOUT | COMP1_INP, ADC1_IN14, WKUP5 |
| 35 | M5 | M5 | 46 | 46 | M9 | K5 | K5 | 32 | 42 | M5 | M9 | M9 | N4 | PB0 | I/O | TT_la | - | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT | OPAMP2_VOUT, ADC1_IN15 |

Table 15. STM32L4Rxxx pin definitions (continued)

| Pin number | | | | | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4R5xxx, STM32L4R7xxx | | | | | | | | STM32L4R9xxx | | | | | | | | | | | |
| LQFP100 | BGA132_SMPS | BGA132 | LQFP144_SMPS | LQFP144 | WLCSP144 | UFBGA169_SMPS | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144_SMPS | WLCSP144 | UFBGA169 | | | | | | |
| 42 | M9 | M9 | 64 | 64 | L5 | N8 | N8 | 39 | 60 | H7 | L5 | L5 | N8 | PE11 | I/O | FT | - | TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, OCTOSPIM_P1_NCS, LCD_G4, FMC_D8, EVENTOUT | - |
| 43 | L9 | L9 | 65 | 65 | M5 | M8 | M8 | 40 | 61 | M9 | M5 | M5 | M8 | PE12 | I/O | FT | - | TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, OCTOSPIM_1_IO0, LCD_G5, FMC_D9, EVENTOUT | - |
| 44 | M10 | M10 | 66 | 66 | J5 | L8 | L8 | 41 | 62 | J8 | J5 | J5 | L8 | PE13 | I/O | FT | - | TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, OCTOSPIM_P1_IO1, LCD_G6, FMC_D10, EVENTOUT | - |

**Table 15. STM32L4Rxxx pin definitions (continued)**

| Pin number | | | | | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4R5xxx, STM32L4R7xxx | | | | | | | | STM32L4R9xxx | | | | | | | | | | | |
| LQFP100 | BGA132_SMPS | BGA132 | LQFP144_SMPS | LQFP144 | WLCSP144 | UFBGA169_SMPS | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144_SMPS | WLCSP144 | UFBGA169 | | | | | | |
| - | - | - | - | - | - | A2 | A2 | - | - | - | - | - | A2 | PH2 | I/O | FT | - | OCTOSPIM_P1_IO4, EVENTOUT | - |
| - | - | - | - | - | - | B2 | B2 | - | - | - | - | - | B2 | PI7 | I/O | FT | - | TIM8_CH3, DCMI_D7, EVENTOUT | - |
| - | - | - | - | - | - | B1 | B1 | - | - | - | - | - | B1 | PI9 | I/O | FT | - | OCTOSPIM_P2_IO2, CAN1_RX, EVENTOUT | - |
| - | - | - | - | - | - | A1 | A1 | - | - | - | - | - | A1 | PI10 | I/O | FT | - | OCTOSPIM_P2_IO1, EVENTOUT | - |

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0432 reference manual.
3. NC (not-connected) balls must be left unconnected. However, non connected (NC) GPIOS are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low-power modes.
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses[(1)] (continued)

| Bus | Boundary address | Size (bytes) | Peripheral |
|---|---|---|---|
| APB2 | 0x4001 1C00 - 0x4001 1FFF | 1 KB | FIREWALL |
| | 0x4001 0800- 0x4001 1BFF | 5 KB | Reserved |
| | 0x4001 0400 - 0x4001 07FF | 1 KB | EXTI |
| | 0x4001 0200 - 0x4001 03FF | 1 KB | COMP |
| | 0x4001 0030 - 0x4001 01FF | 1 KB | VREFBUF |
| | 0x4001 0000 - 0x4001 002F | 1 KB | SYSCFG |
| APB1 | 0x4000 9800 - 0x4000 FFFF | 26 KB | Reserved |
| | 0x4000 9400 - 0x4000 97FF | 1 KB | LPTIM2 |
| | 0x4000 8C00 - 0x4000 93FF | 3 KB | Reserved |
| | 0x4000 8400 - 0x4000 87FF | 1 KB | I2C4 |
| | 0x4000 8000 - 0x4000 83FF | 1 KB | LPUART1 |
| | 0x4000 7C00 - 0x4000 7FFF | 1 KB | LPTIM1 |
| | 0x4000 7800 - 0x4000 7BFF | 1 KB | OPAMP |
| | 0x4000 7400 - 0x4000 77FF | 1 KB | DAC1 |
| | 0x4000 7000 - 0x4000 73FF | 1 KB | PWR |
| | 0x4000 6800 - 0x4000 6FFF | 2 KB | Reserved |
| | 0x4000 6400 - 0x4000 67FF | 1 KB | CAN1 |
| | 0x4000 6000 - 0x4000 63FF | 1 KB | CRS |
| | 0x4000 5C00- 0x4000 5FFF | 1 KB | I2C3 |
| | 0x4000 5800 - 0x4000 5BFF | 1 KB | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | 1 KB | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | 1 KB | UART5 |
| | 0x4000 4C00 - 0x4000 4FFF | 1 KB | UART4 |
| | 0x4000 4800 - 0x4000 4BFF | 1 KB | USART3 |
| | 0x4000 4400 - 0x4000 47FF | 1 KB | USART2 |
| | 0x4000 4000 - 0x4000 43FF | 1 KB | Reserved |
| | 0x4000 3C00 - 0x4000 3FFF | 1 KB | SPI3 |
| | 0x4000 3800 - 0x4000 3BFF | 1 KB | SPI2 |
| | 0x4000 3400 - 0x4000 37FF | 1 KB | Reserved |
| | 0x4000 3000 - 0x4000 33FF | 1 KB | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 KB | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 KB | RTC |
| | 0x4000 1800 - 0x4000 23FF | 4 KB | Reserved |

### 6.3.4 Embedded voltage reference

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 25. Embedded internal voltage reference**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +130 °C | 1.182 | 1.212 | 1.232 | V |
| $t_{S\_vrefint}$ (1) | ADC sampling time when reading the internal reference voltage | - | 4(2) | - | - | µs |
| $t_{start\_vrefint}$ | Start time of reference voltage buffer when ADC is enable | - | - | 8 | 12(2) | µs |
| $I_{DD}(V_{REFINTBUF})$ | $V_{REFINT}$ buffer consumption from $V_{DD}$ when converted by ADC | - | - | 12.5 | 20(2) | µA |
| $\Delta V_{REFINT}$ | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V | - | 5 | 7.5(2) | mV |
| $T_{Coeff}$ | Average temperature coefficient | –40°C < $T_A$ < +130°C | - | 30 | 50(2) | ppm/°C |
| $A_{Coeff}$ | Long term stability | 1000 hours, T = 25°C | - | 300 | 1000(2) | ppm |
| $V_{DDCoeff}$ | Average voltage coefficient | 3.0 V < $V_{DD}$ < 3.6 V | - | 250 | 1200(2) | ppm/V |
| $V_{REFINT\_DIV1}$ | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$ | 1/2 reference voltage | | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$ | 3/4 reference voltage | | 74 | 75 | 76 | |

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

**Table 40. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1**

| Symbol | Parameter | Conditions | | Code | TYP | Unit | TYP | Unit |
|---|---|---|---|---|---|---|---|---|
| | | - | Voltage scaling | | 25°C | | 25°C | |
| $I_{DD}$ (Run) | Supply current in Run mode | $f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable | Range2 $f_{HCLK}$=26 MHz | Reduced code(1) | 3.35 | mA | 129 | µA/MHz |
| | | | | Coremark | 3.10 | | 119 | |
| | | | | Dhrystone2.1 | 3.65 | | 140 | |
| | | | | Fibonacci | 3.20 | | 123 | |
| | | | | While(1) | 2.85 | | 110 | |
| | | | Range 1 Normal Mode $f_{HCLK}$= 80 MHz | Reduced code(1) | 11.0 | mA | 138 | µA/MHz |
| | | | | Coremark | 10.5 | | 131 | |
| | | | | Dhrystone2.1 | 12.5 | | 156 | |
| | | | | Fibonacci | 10.5 | | 131 | |
| | | | | While(1) | 9.40 | | 118 | |
| | | | Range 1 Boost Mode $f_{HCLK}$= 120 MHz | Reduced code(1) | 18.0 | mA | 150 | µA/MHz |
| | | | | Coremark | 16.5 | | 138 | |
| | | | | Dhrystone2.1 | 19.5 | | 163 | |
| | | | | Fibonacci | 17.5 | | 146 | |
| | | | | While(1) | 15.0 | | 125 | |
| $I_{DD}$(LPRun) | Supply current in Low-power run | $f_{HCLK}$ = $f_{MSI}$ = 2MHz all pripherals disable | | Reduced code(1) | 435 | µA | 218 | µA/MHz |
| | | | | Coremark | 395 | | 198 | |
| | | | | Dhrystone2.1 | 470 | | 235 | |
| | | | | Fibonacci | 425 | | 213 | |
| | | | | While(1) | 455 | | 228 | |

1. Reduced code used for characterization results provided in *Table 26*, *Table 30*, *Table 34*.

**Table 47. Current consumption in Stop 1 mode**

| Symbol | Parameter | Conditions | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | VDD | 25°C | 55°C | 85°C | 105°C | 125°C | 25°C | 55°C | 85°C | 105°C | 125°C | |
| IDD (Stop 1) | Supply current in Stop 1 mode, RTC disabled | - | 1.8 V | 120 | 430 | 1400 | 2750 | 5050 | 280 | 1100 | 3300 | 6500 | 13000 | µA |
| | | | 2.4 V | 120 | 430 | 1400 | 2750 | 5100 | 280 | 1100 | 3300 | 6500 | 13000 | |
| | | | 3 V | 125 | 430 | 1400 | 2750 | 5100 | 280 | 1100 | 3300 | 6500 | 13000 | |
| | | | 3.6 V | 120 | 430 | 1400 | 2750 | 5150 | 280 | 1100 | 3300 | 6600 | 13000(2) | |
| IDD (Stop 1 with RTC) | Supply current in STOP 1 mode, RTC enabled | RTC clocked by LSI | 1.8 V | 120 | 430 | 1400 | 2700 | 5050 | 280 | 1100 | 3300 | 6500 | 13000 | |
| | | | 2.4 V | 125 | 430 | 1400 | 2750 | 5100 | 280 | 1100 | 3300 | 6500 | 13000 | |
| | | | 3 V | 125 | 430 | 1400 | 2750 | 5100 | 280 | 1100 | 3300 | 6600 | 13000 | |
| | | | 3.6 V | 125 | 435 | 1400 | 2750 | 5150 | 280 | 1100 | 3300 | 6600 | 13000 | |
| | | RTC clocked by LSE bypassed at 32768 Hz | 1.8 V | 120 | 430 | 1400 | 2750 | 5050 | 300 | 1100 | 3500 | 6900 | 13000 | |
| | | | 2.4 V | 120 | 435 | 1400 | 2750 | 5100 | 300 | 1100 | 3500 | 6900 | 13000 | |
| | | | 3 V | 125 | 435 | 1400 | 2750 | 5100 | 320 | 1100 | 3500 | 6900 | 13000 | |
| | | | 3.6 V | 125 | 435 | 1400 | 2750 | 5150 | 320 | 1100 | 3500 | 6900 | 13000 | |
| | | RTC clocked by LSE quartz(3) in low drive mode | 1.8 V | 120 | 420 | 1350 | 2700 | - | 300 | 1100 | 3400 | 6800 | - | |
| | | | 2.4 V | 120 | 420 | 1350 | 2700 | - | 300 | 1100 | 3400 | 6800 | - | |
| | | | 3 V | 120 | 420 | 1350 | 2700 | - | 300 | 1100 | 3400 | 6800 | - | |
| | | | 3.6 V | 120 | 425 | 1350 | 2700 | - | 300 | 1100 | 3400 | 6800 | - | |
| IDD (wakeup from Stop 1) | Supply current during wakeup from Stop 1 mode | Wakeup clock is MSI = 48 MHz, voltage Range 1(4) | 3 V | 2.10 | - | - | - | - | - | - | - | - | - | mA |
| | | Wakeup clock is MSI = 4 MHz, voltage Range 2(4) | 3 V | 0.70 | - | - | - | - | - | - | - | - | - | |
| | | Wakeup clock is HSI = 16 MHz, voltage Range 1(4) | 3 V | 1.50 | - | - | - | - | - | - | - | - | - | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*

### 6.3.7 External clock source characteristics

#### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

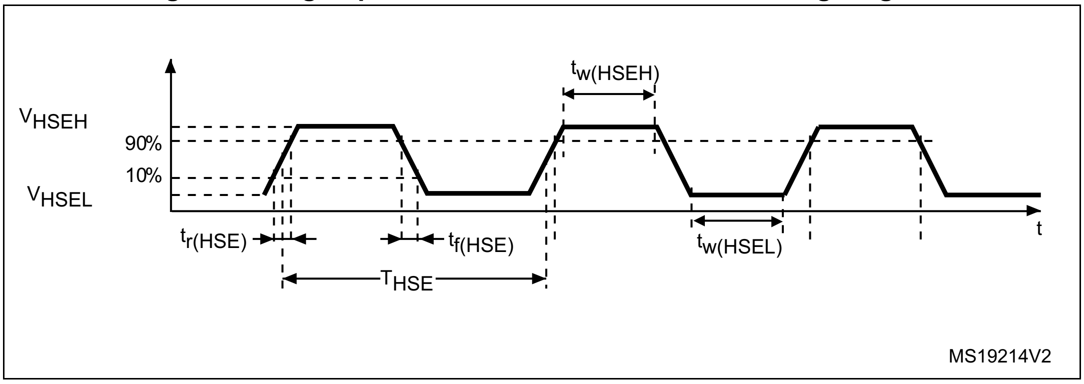
The external clock signal has to respect the I/O characteristics in *Section 6.3.17*. However, the recommended clock input waveform is shown in *Figure 29: High-speed external clock source AC timing diagram*.

**Table 56. High-speed external user clock characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency | Voltage scaling Range 1 | - | 8 | 48 | MHz |
| | | Voltage scaling Range 2 | - | 8 | 26 | |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | - | 0.7 $V_{DDIOx}$ | - | $V_{DDIOx}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | - | $V_{SS}$ | - | 0.3 $V_{DDIOx}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | Voltage scaling Range 1 | 7 | - | - | ns |
| | | Voltage scaling Range 2 | 18 | - | - | |

1. Guaranteed by design.

**Figure 29. High-speed external clock source AC timing diagram**



### 6.3.9 PLL characteristics

The parameters given in *Table 64* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 64. PLL, PLLSAI1, PLLSAI2 characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL\_IN}$ | PLL input clock(2) | - | 2.66 | - | 16 | MHz |
| | PLL input clock duty cycle | - | 45 | - | 55 | % |
| $f_{PLL\_P\_OUT}$ | PLL multiplier output clock P | Voltage scaling Range 1 Normal mode | 2.0645 | - | 80 | MHz |
| | | Voltage scaling Range 1 Boost mode | 2.0645 | - | 120 | |
| | | Voltage scaling Range 2 | 2.0645 | - | 26 | |
| $f_{PLL\_Q\_OUT}$ | PLL multiplier output clock Q | Voltage scaling Range 1 Normal mode | 8 | - | 80 | |
| | | Voltage scaling Range 1 Boost mode | 8 | - | 120 | |
| | | Voltage scaling Range 2 | 8 | - | 26 | |
| $f_{PLL\_R\_OUT}$ | PLL multiplier output clock R | Voltage scaling Range 1 Normal mode | 8 | - | 80 | |
| | | Voltage scaling Range 1 Boost mode | 8 | - | 120 | |
| | | Voltage scaling Range 2 | 8 | - | 26 | |
| $f_{VCO\_OUT}$ | PLL VCO output | Voltage scaling Range 1 | 64 | - | 344 | |
| | | Voltage scaling Range 2 | 64 | - | 128 | |
| $t_{LOCK}$ | PLL lock time | - | - | 15 | 40 | μs |
| Jitter | RMS cycle-to-cycle jitter | System clock 80 MHz | - | 40 | - | ±ps |
| | RMS period jitter | | - | 30 | - | |
| $I_{DD}(PLL)$ | PLL power consumption on $V_{DD}$(1) | VCO freq = 64 MHz | - | 150 | 200 | μA |
| | | VCO freq = 96 MHz | - | 200 | 260 | |
| | | VCO freq = 192 MHz | - | 300 | 380 | |
| | | VCO freq = 344 MHz | - | 520 | 650 | |

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

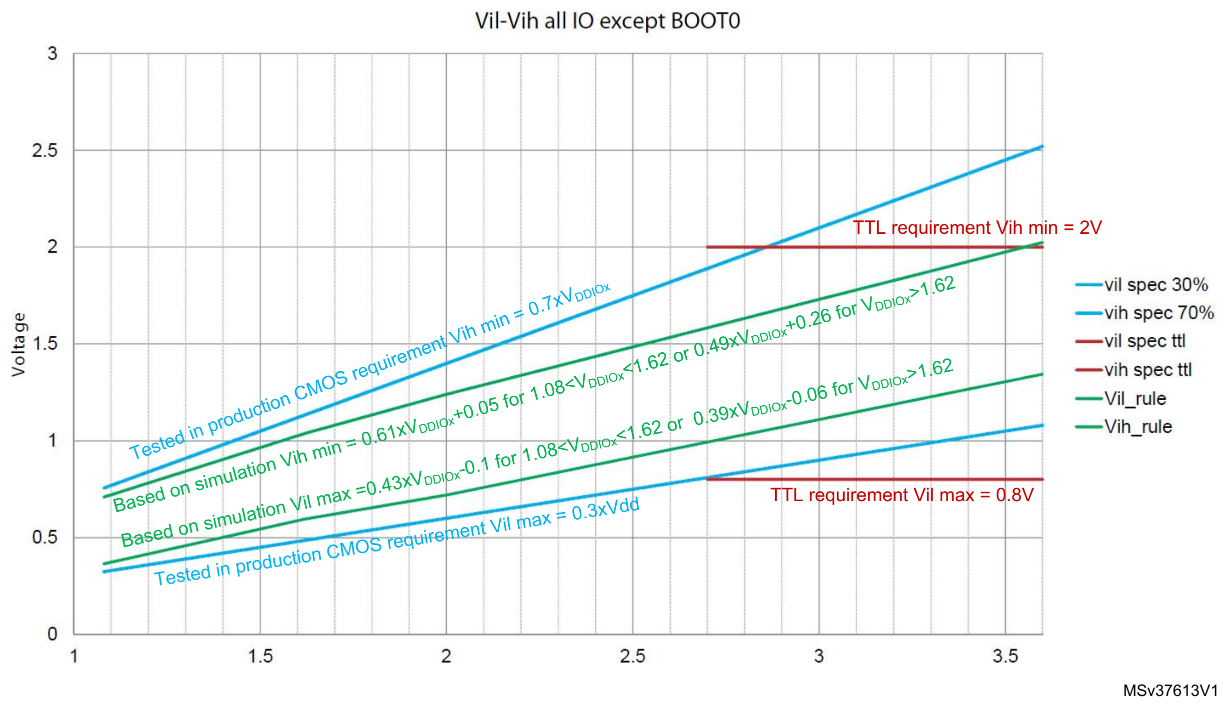
### 6.3.10 MIPI D-PHY characteristics

The parameters given in *Table 65* and *Table 66* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22*.

1. Refer to *Figure 38: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. Max($V_{DDXXX}$) is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table.*
5. All TX_xx IO except FT_lu, FT_u, PB2 and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:
   $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where $V_{IN}$ is applied on the pad] $_x$ $I_{lkg}$(Max).
7. To sustain a voltage higher than MIN($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$, $V_{LCD}$) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to $I_{bias}$ in *Table 92: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 38* for standard I/Os, and in *Figure 38* for 5 V tolerant I/Os.

**Figure 38. I/O input characteristics**




## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed $V_{OL}/V_{OH}$).

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when $V_{DDA}$ < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA}$ < 2.4V). It is disable when $V_{DDA} \geq 2.4$ V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0.
4. Slow channels are: all ADC inputs except the fast channels.

**Figure 49. USB OTG timings – definition of data signal rise and fall time**

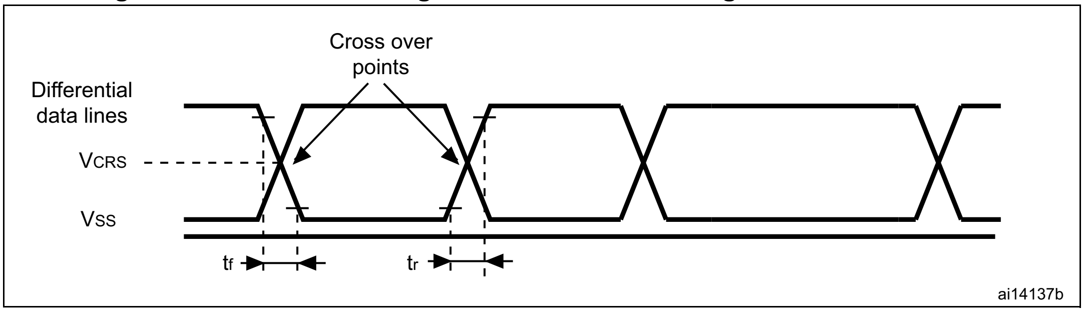



**Table 104. USB OTG electrical characteristics(1)**

| Driver characteristics | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_{rLS}$ | Rise time in LS(2) | $C_L$ = 200 to 600 pF | 75 | 300 | ns |
| $t_{fLS}$ | Fall time in LS(2) | | | | |
| $t_{rfmLS}$ | Rise/ fall time matching in LS | $t_r$ / $t_f$ | 80 | 125 | % |
| $t_{rFS}$ | Rise time in FS(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{fFS}$ | Fall time in FS(2) | $C_L$ = 50 pF | | | |
| $t_{rfmFS}$ | Rise/ fall time matching in FS | $t_r$ / $t_f$ | 90 | 111 | % |
| $V_{CRS}$ | Output signal crossover voltage (LS/FS) | - | 1.3 | 2.0 | V |
| $Z_{DRV}$ | Output driver impedance(3) | Driving high or low | 28 | 44 | Ω |

1. Guaranteed by design
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

**Table 105. USB BCD DC electrical characteristics(1)**

| Driver characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{DD(USBBCD)}$ | Primary detection mode consumption | - | - | - | 300 | µA |
| | Secondary detection mode consumption | - | - | - | | |
| RDAT_LKG | Data line leakage resistance | - | 300 | - | - | kΩ |
| VDAT_LKG | Data line leakage voltage | - | 0.0 | - | 3.6 | V |
| RDCP_DAT | Dedicated charging port resistance across D+/D- | - | - | - | 200 | Ω |
| VLGC_HI | Logic high | - | 2.0 | - | 3.6 | V |
| VLGC_LOW | Logic low | - | - | - | 0.8 | V |

**Figure 65. OctoSPI Hyperbus read**

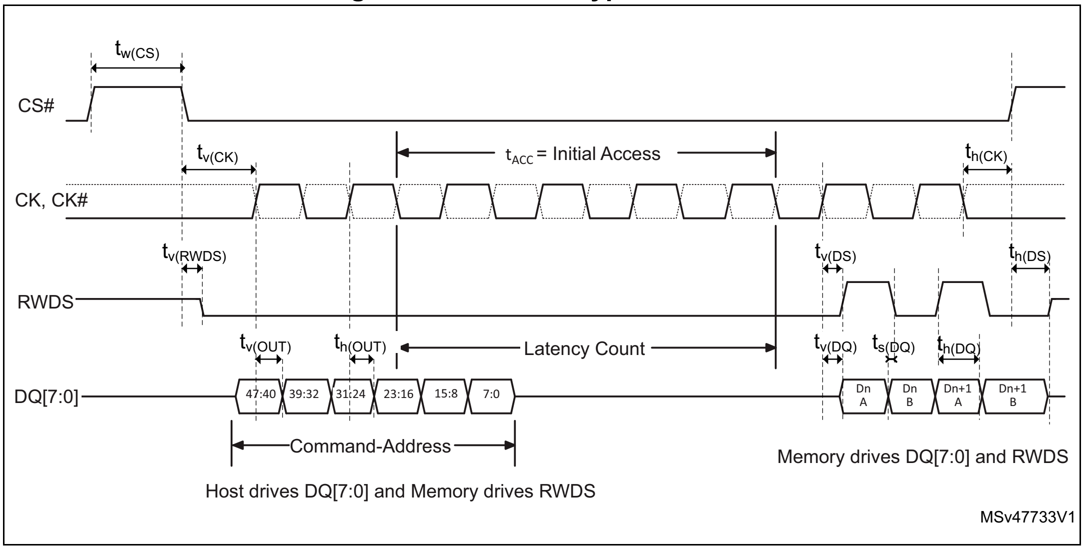
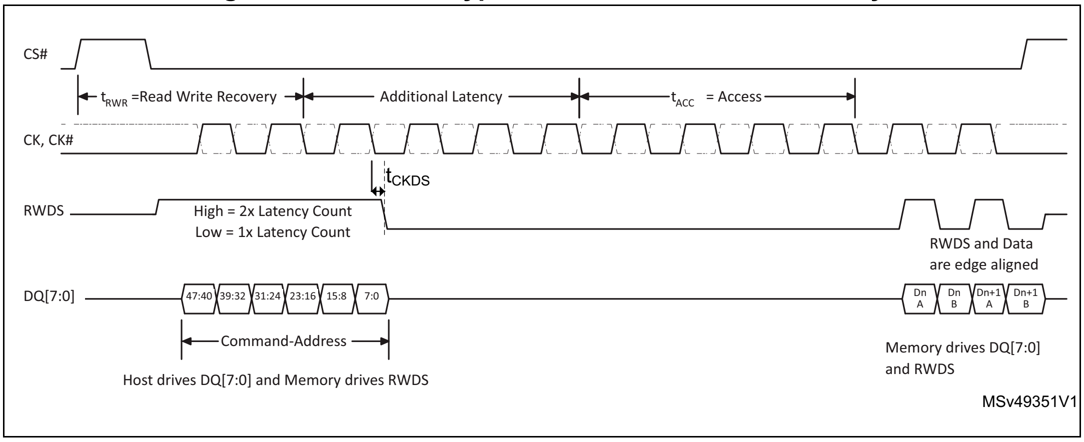



**Figure 66. OctoSPI Hyperbus read with double latency**

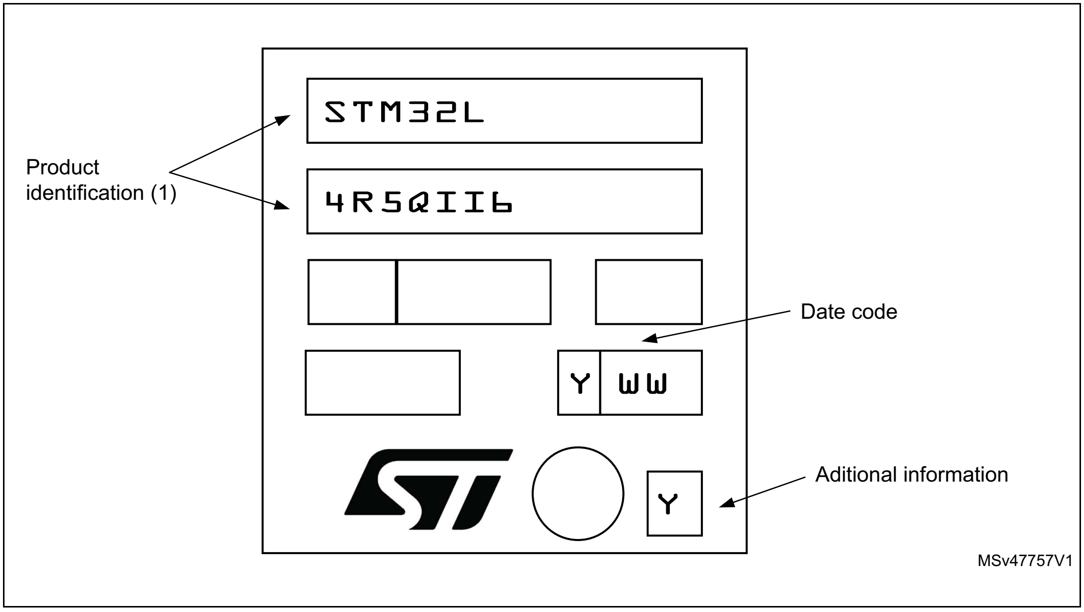


### UFBGA132 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 87. UFBGA132 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.