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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	112
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r9zgj6

The main features of the firewall are the following:

- Three segments can be protected and defined thanks to the firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segment are configurable:
  - Code segment: up to 2048 Kbytes with granularity of 256 bytes
  - Non-volatile data segment: up to 2048 Kbytes with granularity of 256 bytes
  - Volatile data segment: up to 192 Kbytes of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.8 Boot modes

At startup, a BOOT0 pin and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty-check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed and if the boot selection is configured to boot from main Flash.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB OTG FS in device mode through the DFU (device firmware upgrade).

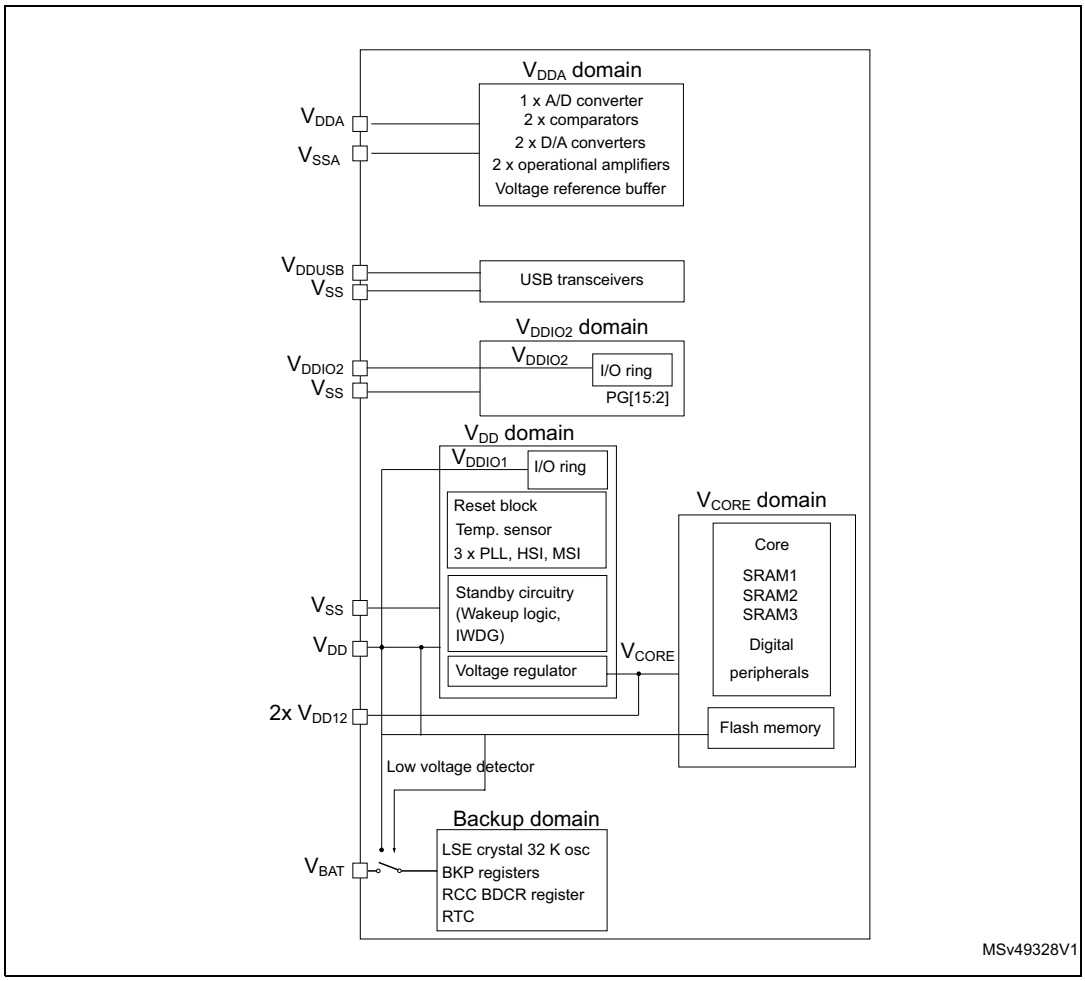
3.9 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

Figure 4. STM32L4R5xxxP and STM32L4R7xxxP with external SMPS power supply overview



retained in Standby mode, supplied by the low-power regulator (standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2, SRAM3 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 8. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.19.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 9. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.19.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18. As the V_{BAT} voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.20 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	J6	J6	93	93	E2	H9	H9	-	97	E8	E2	E2	F10	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	94	94	D12	F13	F13	-	-	F11	D12	D12	F13	VSS	S	-	-	-	-
-	-	-	95	95	E3	F12	F12	-	-	E12	E3	E3	F12	VDDIO 2	S	-	-	-	-
63	E12	E12	96	96	E4	F11	F11	65	98	D12	E4	E4	F11	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, SDMMC1_D0DIR, TSC_G4_IO1, DCMI_D0, LCD_R0, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
64	E11	E11	97	97	E6	G12	G12	66	99	E9	E6	E6	G11	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, SDMMC1_D123DIR, TSC_G4_IO2, DCMI_D1, LCD_R1, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
65	E10	E10	98	98	D1	G10	G10	67	100	E10	D1	D1	F9	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, DCMI_D2, SDMMC1_D0, EVENTOUT	-
66	D12	D12	99	99	D2	G9	G9	68	101	C12	D2	D2	G13	PC9	I/O	FT_fl	-	TRACED0, TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3, I2C3_SDA, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, SAI2_EXTCLK, EVENTOUT	-
67	D11	D11	100	100	D3	G8	G8	69	102	D11	D3	D3	E11	PA8	I/O	FT_f	-	MCO, TIM1_CH1, SAI1_CK2, USART1_CK, OTG_FS_SOF, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	-	-	-	-	-	D11	D11	-	-	-	-	-	C11	PH9	I/O	FT	-	I2C3_SMBA, OCTOSPIM_P2_IO4, DCMI_D0, EVENTOUT	-
-	-	-	-	-	-	B13	B13	-	-	-	-	-	B13	PH12	I/O	FT	-	TIM5_CH3, OCTOSPIM_P2_IO7, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	A13	A13	-	-	-	-	-	A13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-
-	-	-	-	-	-	B12	B12	-	-	-	-	-	B12	PH15	I/O	FT	-	TIM8_CH3N, OCTOSPIM_P2_IO6, DCMI_D11, EVENTOUT	-
-	-	-	-	-	-	A12	A12	-	-	-	-	-	A12	PI0	I/O	FT	-	TIM5_CH4, OCTOSPIM_P1_IO5, SPI2_NSS, DCMI_D13, EVENTOUT	-
-	-	-	-	-	-	C11	C11	-	-	-	-	-	-	PI8	I/O	FT	-	OCTOSPIM_P2_NCS, DCMI_D12, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
79	C10	C10	112	112	C4	E9	E9	81	114	A9	C4	C4	E9	PC11	I/O	FT	-	DCMI_D2, OCTOSPIM_P1_NCS, SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, DCMI_D4, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
80	B10	B10	113	113	B4	F8	F8	82	115	D9	B4	B4	F8	PC12	I/O	FT	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, DCMI_D9, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
81	C9	C9	114	114	A4	B8	B8	83	116	C8	A4	A4	B8	PD0	I/O	FT	-	SPI2_NSS, DFSDM1_DATIN7, CAN1_RX, LCD_B4, FMC_D2, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
82	B9	B9	115	115	C5	C8	C8	84	117	B8	C5	C5	C8	PD1	I/O	FT	-	SPI2_SCK, DFSDM1_CKIN7, CAN1_TX, LCD_B5, FMC_D3, EVENTOUT	-
83	C8	C8	116	116	B5	D8	D8	85	118	D8	B5	B5	D8	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, DCMI_D11, SDMMC1_CMD, EVENTOUT	-
84	B8	B8	117	117	D6	E8	E8	86	119	A8	D6	D6	E8	PD3	I/O	FT	-	SPI2_SCK, DCMI_D5, SPI2_MISO, DFSDM1_DATIN0, USART2_CTS_NSS, OCTOSPIM_P2_NCS, LCD_CLK, FMC_CLK, EVENTOUT	-
85	B7	B7	118	118	C6	C7	C7	87	120	C7	C6	C6	C7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, OCTOSPIM_P1_IO4, FMC_NOE, EVENTOUT	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port C	PC0	LPUART1_RX	-	-	-	-	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	-	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	TSC_G4_IO1	DCMI_D0	LCD_R0	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_ D123DIR	TSC_G4_IO2	DCMI_D1	LCD_R1	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

6.3.4 Embedded voltage reference

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 46. Current consumption in Stop 2 mode, SRAM3 enabled

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	3.90	15.0	59.5	140	310	13.0	52.0	210	480	1100	µA
			2.4 V	3.95	15.0	60.0	140	310	14.0	53.0	210	480	1100	
			3 V	3.95	15.0	60.5	145	315	14.0	53.0	210	480	1100	
			3.6 V	3.95	15.0	61.5	145	320	14.0	54.0	210	490	1100	
IDD(Stop 2 with RTC)	Supply current in STOP 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	4.10	15.0	60.5	140	310	11.0	53.0	210	480	1100	
			2.4 V	4.25	15.5	60.5	145	315	12.0	54.0	210	480	1100	
			3 V	4.50	15.5	61.5	145	320	12.0	54.0	210	480	1100	
			3.6 V	4.70	16.0	62.5	145	325	12.0	56.0	220	490	1100(2)	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	4.35	15.5	61.0	140	310	9.50	39.0	160	350	780	
			2.4 V	4.50	15.5	61.0	145	315	9.60	39.0	160	370	790	
			3 V	4.70	16.0	62.0	145	320	9.90	40.0	160	370	800	
			3.6 V	4.80	16.5	63.0	145	325	10.0	42.0	160	370	820	
		RTC clocked by LSE quartz in low drive mode	1.8 V	4.30	15.5	63.5	150	-	9.40	39.0	160	380	-	
			2.4 V	4.40	16.0	64.0	150	-	9.50	40.0	160	380	-	
			3 V	4.45	16.0	64.5	150	-	9.60	40.0	170	380	-	
			3.6 V	4.85	16.5	65.5	155	-	11.0	42.0	170	390	-	
IDD(wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(3)	3 V	3.80	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(3)	3 V	1.30	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(3)	3 V	2.95	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*.

Table 53. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	30.7	47.8	µs
			Wakeup clock MSI = 4 MHz	40.4	55.6	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	32.1	49.1	
			Wakeup clock MSI = 4 MHz	41.5	55.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	265.0	339.4	

1. Guaranteed by characterization results.

Table 54. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low- power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 55. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by characterization results.

Table 61. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD}=2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD}=2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	-5	-	1	
				V_{DD}=2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(6)}$	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	%
			T_A= -40 to 125 °C		-	2	4	
P_USB Jitter(MSI)(6)	Period jitter for USB clock(4)	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI)(6)	Medium term jitter for USB clock(5)	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI)(6)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(6)	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(6)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 110. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-0.5	$4T_{HCLK}$+1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK}$-0.5	$2T_{HCLK}$+1	
$t_{w(NOE)}$	FMC_NOE low time	T_{HCLK}-0.5	T_{HCLK}+0.5	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	T_{HCLK}-1	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1.5	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}	T_{HCLK}+1.5	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	T_{HCLK}-3	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}+14	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	14	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 111. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$-0.5	$9T_{HCLK}$+ 1	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{HCLK}$-0.5	$6T_{HCLK}$+1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+12	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+11	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 115. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK}- 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	RxT_{HCLK}/2 +1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Table 125. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tISU	Input setup time HS	-	1.5	-	-	ns
tIHD	Input hold time HS	-	2	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tOV	Output valid time HS	-	-	5	6.5	ns
tOH	Output hold time HS	-	4	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	-	1.5	-	-	ns
tIHD	Input hold time SD	-	2	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	-	-	1	2.5	ns
tOHD	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. For SD 1.8 V support, an external voltage converter is needed.

Table 126. Dynamics characteristics: eMMC characteristics at VDD = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	52	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp = 52 MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp = 52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
tISU	Input setup time HS	-	0.5	-	-	ns
tIH	Input hold time HS	-	4.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
tOV	Output valid time HS	-	-	6	7.4	ns
tOH	Output hold time HS	-	4	-	-	

1. Guaranteed by characterization results.
2. Cload = 20 pF.

Table 133. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, recommended PCB design rules

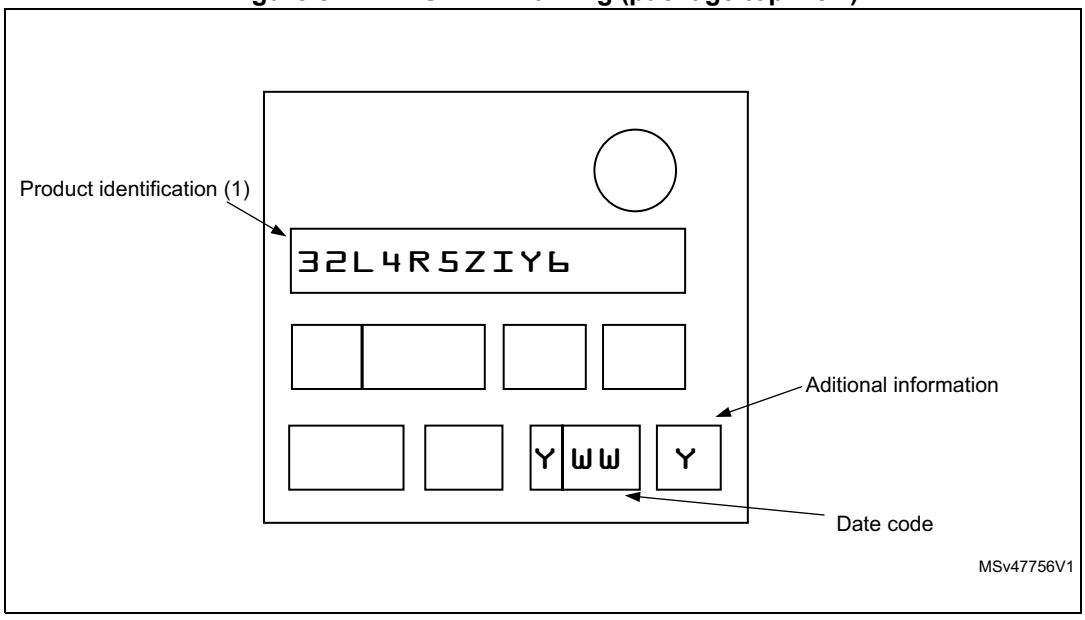
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

WLCSP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

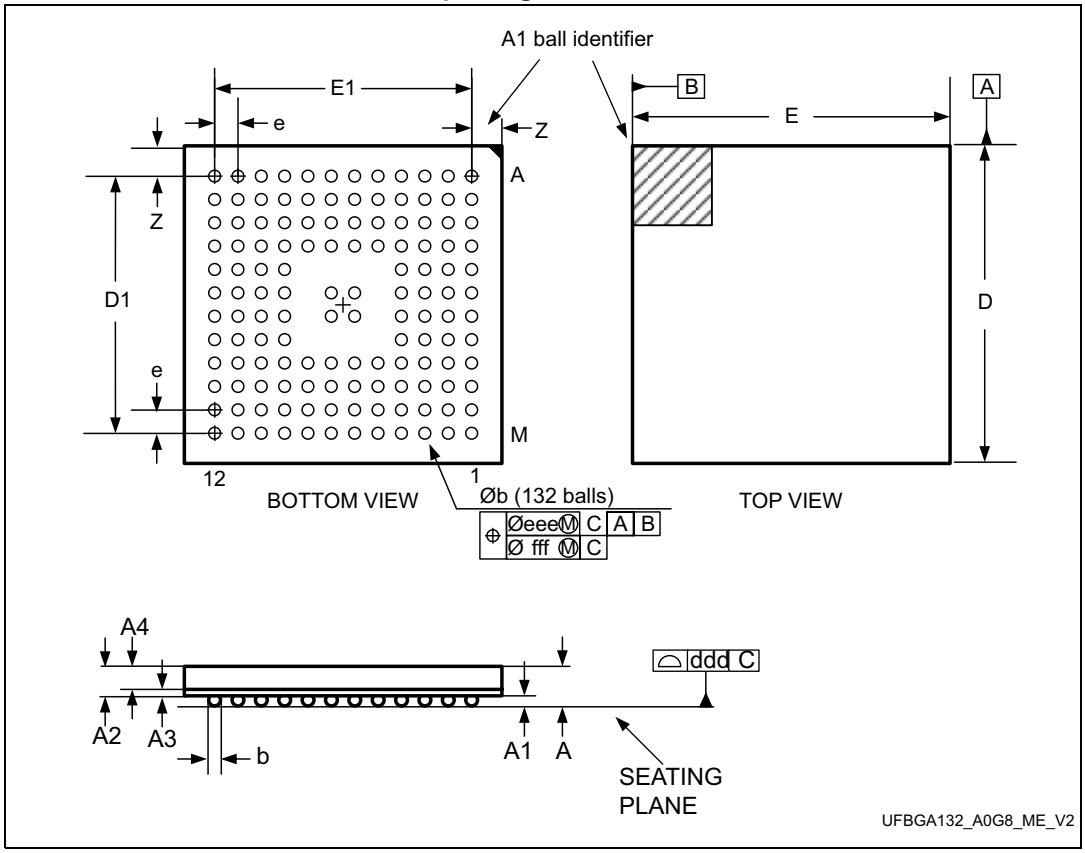
Figure 84. WLCSP144 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 UFBGA132 package information

Figure 85. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 134. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-