Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	112
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA, WLCSP
Supplier Device Package	144-WLCSP (5.24x5.24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r9zgy6tr

  - 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC, low-power sample and hold
  - 2x operational amplifiers with built-in PGA
  - 2x ultra-low-power comparators
- 20x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2x SAIs (serial audio interface)
  - 4x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 6x USARTs (ISO 7816, LIN, IrDA, modem)
  - 3x SPIs (5x SPIs with the dual OctoSPI)
  - CAN (2.0B Active) and SDMMC
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- 8- to 14-bit camera interface up to 32 MHz (black and white) or 10 MHz (color)
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell (ETM)

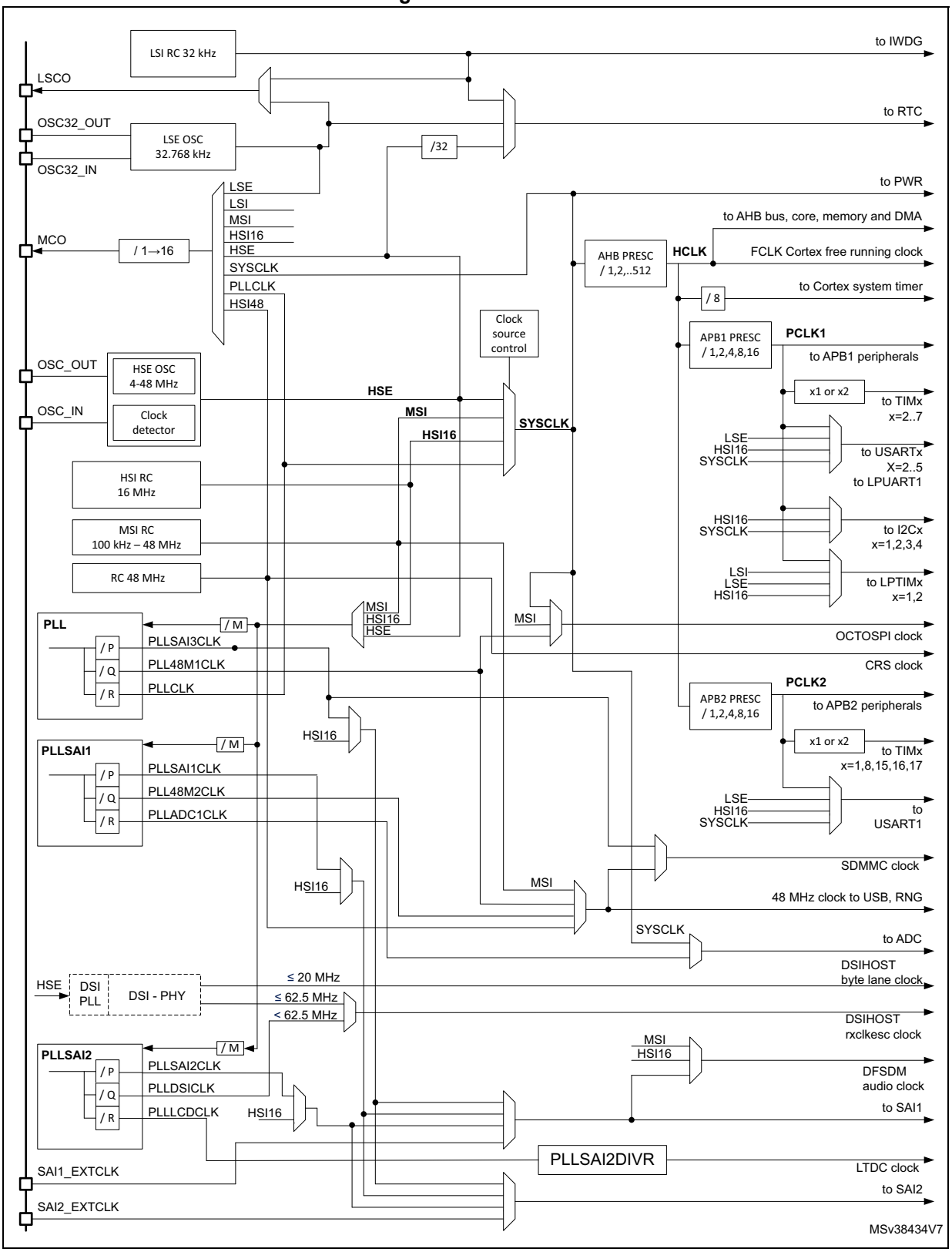
Table 1. Device summary

Reference	Part numbers
STM32L4R5xx	STM32L4R5VI, STM32L4R5QI, STM32L4R5ZI, STM32L4R5AI, STM32L4R5AG, STM32L4R5QG, STM32L4R5VG, STM32L4R5ZG
STM32L4R7xx	STM32L4R7VI, STM32L4R7ZI, STM32L4R7AI
STM32L4R9xx	STM32L4R9VI, STM32L4R9ZI, STM32L4R9AI, STM32L4R9AG, STM32L4R9VG, STM32L4R9ZG

Table 4. STM32L4R5xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Stop 0[5]	Range 1 Range 2	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]

Figure 7. Clock tree



3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.14 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are both software programmable (4 levels: very high, high, medium, low) or hardware programmable in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

3.27 Digital filter for sigma-delta modulators (DFSDM)

The STM32L4Rxxx devices embed one DFSDM with four digital filters modules and eight external input serial channels (transceivers) or alternately eight internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to the microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs).

The DFSDM can also interface the PDM (pulse density modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators) and the DFSDM digital filter modules perform digital processing according to the user's selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various SD modulator(s)
  - Configurable Manchester coded 1 wire interface support
  - PDM (pulse density modulation) microphone input support
  - Maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - Clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16-bit input resolution):
  - Internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - Integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - Software trigger
  - Internal timers
  - External events
  - Start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - Low value and high-value data threshold registers
  - Dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from final output data or from selected input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - Up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - Monitoring continuously each input serial channel

3.39 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume.

The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

The major features are:

- Combined Rx and Tx FIFO size of 1.25 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- One bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- Eight host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- Software configurable to OTG 1.3 and OTG 2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery charging specification revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

The synchronization for this oscillator can also be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.40 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.41 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named flexible memory controller (FMC).

3.44.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L4Rxxx devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

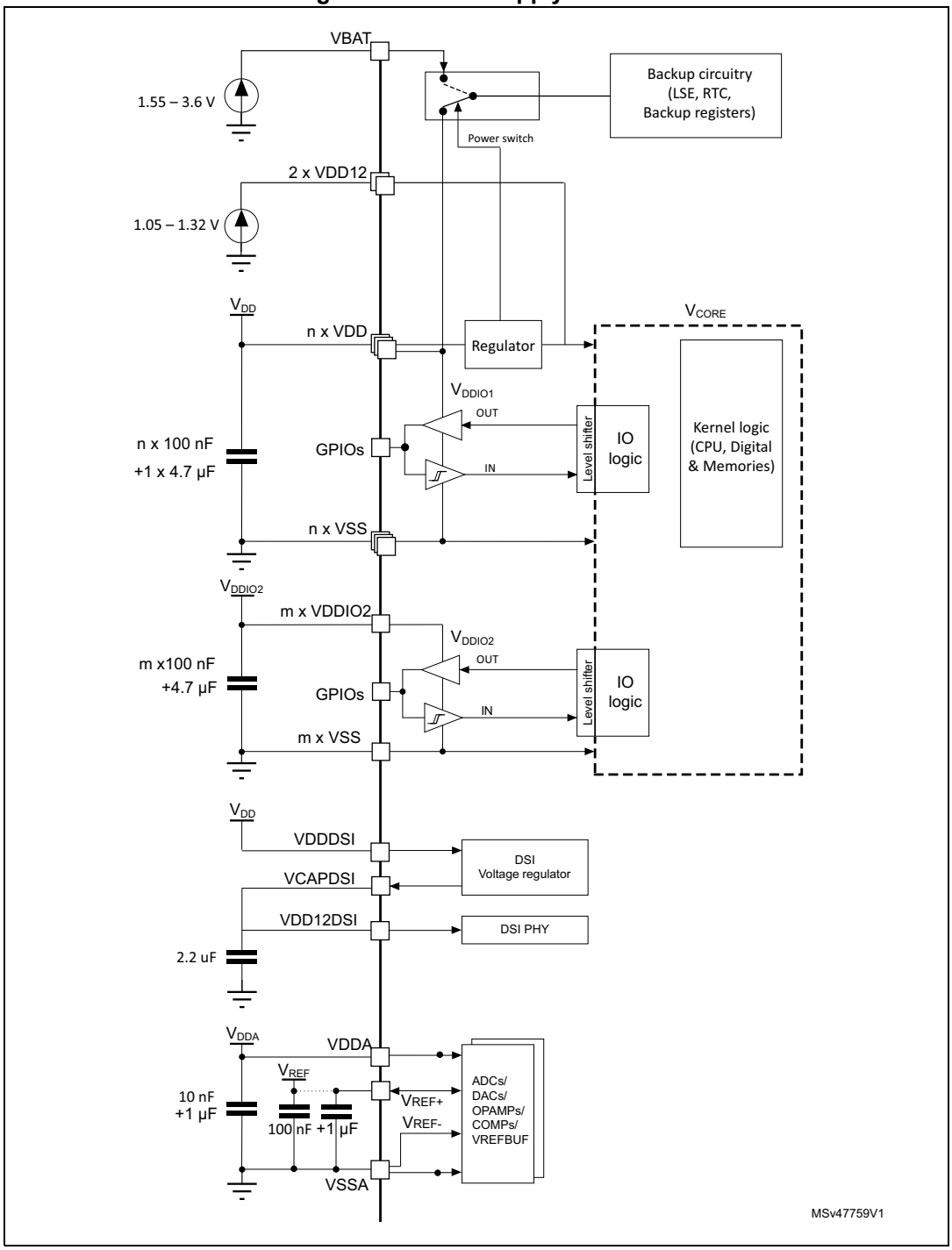
The Embedded Trace Macrocell operates with third party debugger software tools.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	J6	J6	93	93	E2	H9	H9	-	97	E8	E2	E2	F10	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	94	94	D12	F13	F13	-	-	F11	D12	D12	F13	VSS	S	-	-	-	-
-	-	-	95	95	E3	F12	F12	-	-	E12	E3	E3	F12	VDDIO 2	S	-	-	-	-
63	E12	E12	96	96	E4	F11	F11	65	98	D12	E4	E4	F11	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, SDMMC1_D0DIR, TSC_G4_IO1, DCMI_D0, LCD_R0, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
64	E11	E11	97	97	E6	G12	G12	66	99	E9	E6	E6	G11	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, SDMMC1_D123DIR, TSC_G4_IO2, DCMI_D1, LCD_R1, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-

6.1.6 Power supply scheme

Figure 26. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 30. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	4.00	4.40	5.55	7.20	10.0	4.60	5.5	7.5	11.0	17.0	mA
				16 MHz	2.65	3.05	4.15	5.80	8.75	3.10	4.0	6.0	9.3	16.0	
				8 MHz	1.50	1.85	2.90	4.45	7.25	1.80	2.6	4.6	7.9	14.0	
				4 MHz	0.875	1.25	2.35	3.95	6.90	1.20	1.9	3.9	7.2	14.0	
				2 MHz	0.565	0.925	2.05	3.65	6.55	0.77	1.6	3.6	6.8	13.0	
				1 MHz	0.405	0.770	1.90	3.50	6.40	0.60	1.4	3.4	6.7	13.0	
				100 KHz	0.265	0.635	1.75	3.35	6.25	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.5	19.5	21.0	23.5	27.0	21.00	23.0	26.0	30.0	38.0	
			Range 1 Normal Mode	80 MHz	13.0	13.5	15.5	17.5	21.0	15.00	17.0	19.0	23.0	30.0	
				72 MHz	12.0	12.5	14.0	16.0	20.0	14.00	15.0	18.0	22.0	29.0	
				64 MHz	10.5	11.0	12.5	15.0	18.5	12.00	14.0	16.0	20.0	28.0	
				48 MHz	8.75	9.30	11.0	13.0	16.5	9.80	12.0	14.0	18.0	25.0	
				32 MHz	6.20	6.70	8.20	10.0	14.0	7.00	8.2	11.0	15.0	22.0	
				24 MHz	4.70	5.20	6.70	10.5	12.5	5.40	6.5	9.0	13.0	20.0	
				16 MHz	3.35	3.85	5.25	7.30	11.0	3.90	4.9	7.4	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	595	1000	2300	4150	7350	810.00	1700	4100	7800	15000	µA
				1 MHz	370	800	2100	3950	7150	560.00	1500	3900	7600	14000	
				400 KHz	245	705	2000	3850	7050	420.00	1400	3800	7500	14000	
				100 KHz	230	655	1950	3800	7000	400.00	1400	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 32. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	4.10	4.50	5.60	7.20	10.00	4.7	5.6	7.6	11.0	17.0	mA
				16 MHz	2.75	3.10	4.25	5.85	8.70	3.2	4.1	6.1	9.4	16.0	
				8 MHz	1.25	1.90	2.95	4.55	7.35	1.7	2.7	4.7	8.0	14.0	
				4 MHz	0.91	1.25	2.35	3.90	6.75	1.2	2.0	4.0	7.3	14.0	
				2 MHz	0.59	0.94	2.00	3.60	6.40	0.8	1.6	3.6	6.9	13.0	
				1 MHz	0.42	0.77	1.85	3.40	6.25	0.6	1.4	3.4	6.7	13.0	
				100 KHz	0.27	0.63	1.70	3.25	6.10	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	17.00	18.00	19.50	21.50	25.50	19.0	21.0	24.0	28.0	36.0	
			Range 1 Normal Mode	80 MHz	13.00	13.50	15.00	17.00	20.50	15.0	16.0	19.0	23.0	30.0	
				72 MHz	11.50	12.00	14.00	16.00	19.50	13.0	15.0	18.0	22.0	29.0	
				64 MHz	10.50	11.00	12.50	14.50	18.00	12.0	13.0	16.0	20.0	27.0	
				48 MHz	9.00	9.50	11.00	13.00	16.50	11.0	12.0	15.0	19.0	26.0	
				32 MHz	6.45	6.95	8.40	10.50	14.00	7.3	8.5	12.0	16.0	23.0	
				24 MHz	4.90	5.40	6.85	8.80	12.50	5.6	6.7	9.3	14.0	21.0	
				16 MHz	3.55	4.00	5.40	7.40	11.00	4.1	5.2	7.7	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	590	1000	2300	4050	7200	800.0	1800	4200	7800	15000	µA
				1 MHz	390	805	2100	3850	7000	580.0	1600	4000	7600	14000	
				400 KHz	245	655	1950	3750	6900	420.0	1400	3800	7500	14000	
				100 KHz	195	610	1900	3700	6850	370.0	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 34. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.75	4.85	6.45	9.30	4.70	5.6	7.6	11.0	17.0	mA
				16 MHz	2.20	2.55	3.65	5.20	8.10	3.20	4.1	6.1	9.4	16.0	
				8 MHz	1.20	1.55	2.65	4.25	7.10	1.70	2.7	4.7	8.0	14.0	
				4 MHz	0.74	1.10	2.15	3.75	6.60	1.20	2.0	4.0	7.3	14.0	
				2 MHz	0.49	0.85	1.95	3.50	6.35	0.79	1.6	3.6	6.9	13.0	
				1 MHz	0.37	0.73	1.80	3.40	6.20	0.61	1.4	3.4	6.7	13.0	
				100 KHz	0.26	0.62	1.70	3.25	6.10	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.00	18.50	20.00	22.50	26.50	19.00	21.0	24.0	28.0	36.0(2)	
			Range 1 Normal Mode	80 MHz	11.00	11.50	13.50	15.50	19.00	15.00	16.0	19.0	23.0	30.0(2)	
				72 MHz	10.00	10.50	12.00	14.00	18.00	13.00	15.0	18.0	22.0	29.0	
				64 MHz	9.10	9.60	11.00	13.00	16.50	12.00	13.0	16.0	20.0	27.0	
				48 MHz	7.20	7.70	9.20	11.00	14.50	11.00	12.0	15.0	19.0	26.0	
				32 MHz	4.90	5.40	6.85	8.80	12.50	7.30	8.5	12.0	16.0	23.0	
				24 MHz	3.75	4.25	5.65	7.65	11.00	5.60	6.7	9.3	14.0	21.0	
				16 MHz	2.60	3.10	4.50	6.45	9.90	4.10	5.2	7.7	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable FLASH in power-down		2 MHz	435	885	2150	3950	7100	800	1800	4200	7800	15000	µA
				1 MHz	300	745	2000	3800	6950	580	1600	4000	7600	14000	
				400 KHz	225	655	1900	3700	6850	420	1400	3800	7500	14000	
				100 KHz	180	620	1900	3650	6800	370	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 46. Current consumption in Stop 2 mode, SRAM3 enabled

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	3.90	15.0	59.5	140	310	13.0	52.0	210	480	1100	µA
			2.4 V	3.95	15.0	60.0	140	310	14.0	53.0	210	480	1100	
			3 V	3.95	15.0	60.5	145	315	14.0	53.0	210	480	1100	
			3.6 V	3.95	15.0	61.5	145	320	14.0	54.0	210	490	1100	
IDD(Stop 2 with RTC)	Supply current in STOP 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	4.10	15.0	60.5	140	310	11.0	53.0	210	480	1100	
			2.4 V	4.25	15.5	60.5	145	315	12.0	54.0	210	480	1100	
			3 V	4.50	15.5	61.5	145	320	12.0	54.0	210	480	1100	
			3.6 V	4.70	16.0	62.5	145	325	12.0	56.0	220	490	1100(2)	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	4.35	15.5	61.0	140	310	9.50	39.0	160	350	780	
			2.4 V	4.50	15.5	61.0	145	315	9.60	39.0	160	370	790	
			3 V	4.70	16.0	62.0	145	320	9.90	40.0	160	370	800	
			3.6 V	4.80	16.5	63.0	145	325	10.0	42.0	160	370	820	
		RTC clocked by LSE quartz in low drive mode	1.8 V	4.30	15.5	63.5	150	-	9.40	39.0	160	380	-	
			2.4 V	4.40	16.0	64.0	150	-	9.50	40.0	160	380	-	
			3 V	4.45	16.0	64.5	150	-	9.60	40.0	170	380	-	
			3.6 V	4.85	16.5	65.5	155	-	11.0	42.0	170	390	-	
IDD(wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(3)	3 V	3.80	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(3)	3 V	1.30	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(3)	3 V	2.95	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 53: Low-power mode wakeup timings*.

Table 53. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	12.6	14.5	µs
			Wakeup clock HSI16 = 16 MHz	12.2	14.0	
		Range 2	Wakeup clock MSI = 24 MHz	22.1	24.1	
			Wakeup clock HSI16 = 16 MHz	21.3	23.3	
			Wakeup clock MSI = 4 MHz	25.1	27.1	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.3	7.0	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
		Range 2	Wakeup clock MSI = 24 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
			Wakeup clock MSI = 4 MHz	10.9	12.6	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	20.4	22.4	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			16.8	19.0	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	13.1	14.8	µs
			Wakeup clock HSI16 = 16 MHz	12.6	14.4	
		Range 2	Wakeup clock MSI = 24 MHz	22.6	24.6	
			Wakeup clock HSI16 = 16 MHz	21.7	23.7	
			Wakeup clock MSI = 4 MHz	25.8	27.9	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
		Range 2	Wakeup clock MSI = 24 MHz	6.4	8.0	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
			Wakeup clock MSI = 4 MHz	11.9	13.6	

Figure 51. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

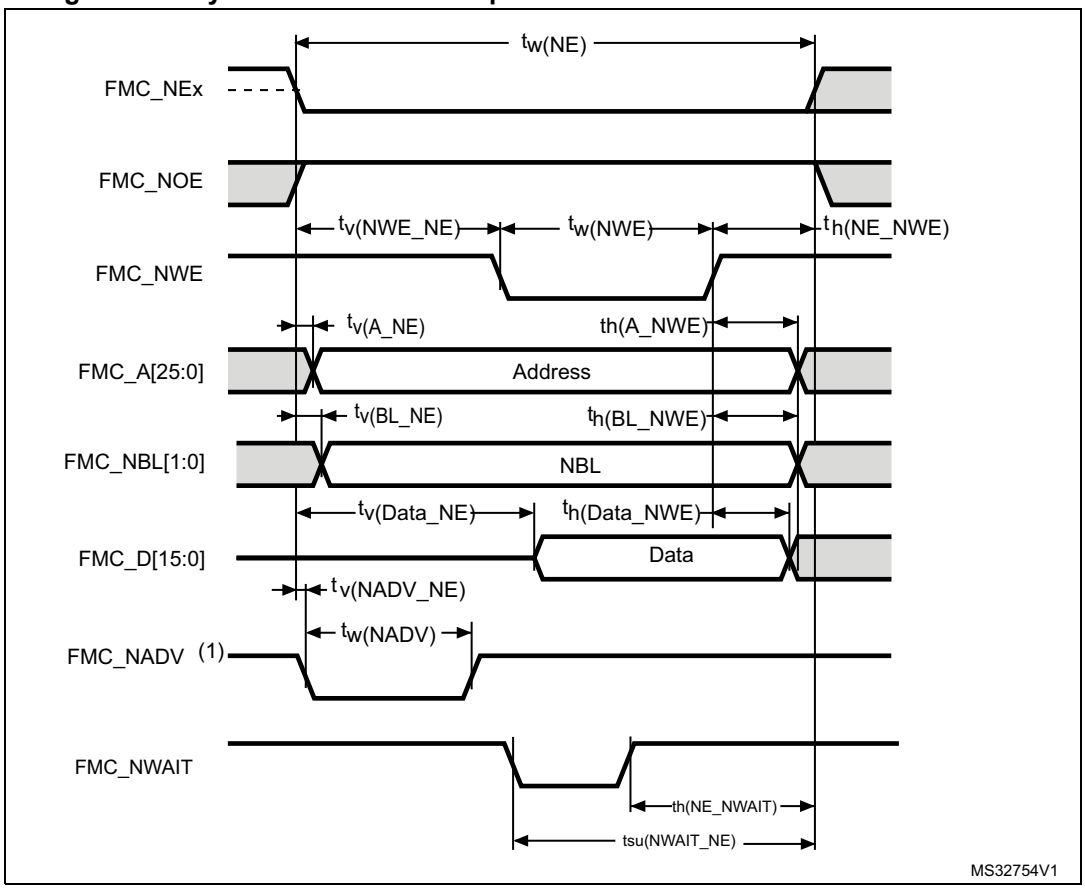


Table 108. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-0.5	$4T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{HCLK}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$2T_{HCLK}$-1	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	T_{HCLK}	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$2T_{HCLK}$-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK}+3	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$2T_{HCLK}$+1	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+1.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 120. OctoSPI(1) characteristics in SDR mode(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(QCK)	OctoSPI clock frequency	1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	58	MHz
		2.7 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	86	
		1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 15 pF	-	-	66	
		1.71 V < V_{DD}< 3.6 V Voltage Range 2 C_{LOAD} = 20 pF	-	-	26	
$t_{w(CKH)}$	OctoSPI clock high and low time	Prescaler = 0	$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$			$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	0.5	-	-	
		Voltage Range 2	0	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	7.75	-	-	
		Voltage Range 2	10.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	2	3.5	
		Voltage Range 2	-	4	5.5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.

6.3.33 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 123* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 21*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Figure 68. DCMI timing diagram

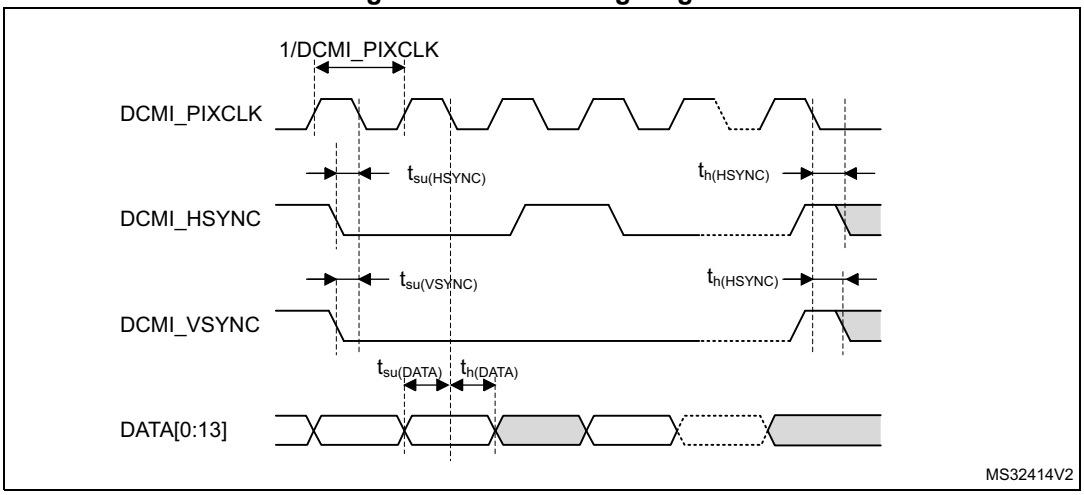


Table 123. DCMI characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	1.71 < VDD < 3.6 Voltage range V1	-	48	MHz
		1.71 < VDD < 3.6 Voltage range V2	-	10	
D_{pixel}	Pixel clock input duty cycle	-	30	70	%

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 124. LTDC characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CLK} D_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V	-	83	MHz
		1.71 V < V_{DD} < 3.6 V	-	50	
	LTDC clock output duty cycle	-	45	55	%
tw(CLKH) tw(CLKL)	Clock high time Clock low time	-	tw(CLK)/2-0.5	tw(CLK)/2+0.5	-
t_v(DATA)	Data output valid time	-	-	6	
t_h(DATA)	Data output hold time	-	0	-	
t_v(HSYNC) t_v(VSYNC) t_v(DE)	HSYNC/VSYNC/DE output valid time	-	-	3	
t_h(HSYNC) t_h(VSYNC) t_h(DE)	HSYNC/VSYNC/DE output hold time	-	0	-	

1. Guaranteed by characterization results.

6.3.35 SD/SDIO/MMC card host interfaces (SDMMC)

Unless otherwise specified, the parameters given in Table xx for SDIO are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in *Table 22: General operating conditions* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD} Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 125. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	66	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp = 52 MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp = 52 MHz	8.5	9.5	-	

Table 125. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tISU	Input setup time HS	-	1.5	-	-	ns
tIHD	Input hold time HS	-	2	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tOV	Output valid time HS	-	-	5	6.5	ns
tOH	Output hold time HS	-	4	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	-	1.5	-	-	ns
tIHD	Input hold time SD	-	2	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	-	-	1	2.5	ns
tOHD	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. For SD 1.8 V support, an external voltage converter is needed.

Table 126. Dynamics characteristics: eMMC characteristics at VDD = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	52	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp = 52 MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp = 52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
tISU	Input setup time HS	-	0.5	-	-	ns
tIH	Input hold time HS	-	4.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
tOV	Output valid time HS	-	-	6	7.4	ns
tOH	Output hold time HS	-	4	-	-	

1. Guaranteed by characterization results.
2. Cload = 20 pF.